# Microelectronic Substrates for Optoelectronic Packages

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*Electronic systems with the increased functionality and speed required in today's advanced applications are placing a performance burden on the interconnection and packaging technologies that standard electrical "wiring" approaches simply cannot support. Engineering staff at APL recognized this trend several years ago, and in a collaborative effort with The Johns Hopkins University Department of Electrical and Computer Engineering, APL has been developing various microelectronic packages that support both electrical and optical signals and facilitate the translation between them. Work has begun to fabricate microelectronic substrates that use integrated optical waveguides to raise the level of the total system's performance as needed. This report will present some of the current technology for optoelectronic packages, an overview of the process technologies being developed industry-wide to meet the need, and details on related work within the Research and Technology Development Center and the Engineering, Design, and Fabrication Branch of the Technical Services Department here at APL.*

## INTRODUCTION

Electronics and photonics are converging at a rapidly increasing rate. Therefore, work is being undertaken by the research community to develop optical interconnects and various concepts, including free-space connections,[1] embedded fibers,[2] and guided wave connections,[3] that have been demonstrated in recent years. The communications industry embraced photonics many years ago, and this trend is spreading to electronic stalwarts such as computer processing, data storage, and sensor systems. Electronic packages with integrated photonic elements, referred to as optoelectronic integrated circuits (OEICs), will eventually be the norm and offer great potential advantages in

performance, size, and cost. In 2005, the Massachusetts Institute of Technology's Microphotonics Center led an industry consortium that established a communications technology road map.[4] Among their conclusions was the assertion that both optical backplanes incorporated into the manufacturing of printed wiring boards (PWBs)[5] and optical interconnects integrated into microelectronic substrates will be a market need within the next 5 years. Industries affected by this technology include computer, automotive, aerospace, security, military, and medical. In short, APL needs experience with OEICs now in order to be able to effectively design and evaluate their applications. The MIT report offered several hybridization levels, which are shown in Table 1.

Our efforts at APL are focused on levels 2 and 3. Level 1 consists of multiple, individually packaged devices interconnected in a module. Level 2 consists of multiple chips in a package with each die being primarily either electrical or optical in nature. The chip itself has been hybridized in level 3 to accommodate mixed signals. This hybridization occurs most often during back-end processing that is done after the fabrication of the chip has been completed. Level 4 is similar to a system on a chip for OEICs. The relative cost is for a mature production process capability that does not exist yet for all levels.

Level 2 interconnections have advanced to the point where optical signals, in addition to electrical signals, are accommodated over a wide range of frequencies and bandwidths. In some cases, like with the work done at the Packaging Research Center of the Georgia Institute of Technology, all of the signals are integrated by a single system-on-a-package (SOP) substrate.[6] The possibilities for the SOP substrate material include FR4 (standard PWB material), polymer, ceramic, and silicon. The goal is to embed optoelectronic interconnections and interfaces within an electrical interconnection substrate. APL has developed unique system packages utilizing both ceramic and silicon that accommodate micro-sized, discrete optical elements such as lenses and diffraction gratings. One such application, which we refer to as a die-level optical interferometer, is presented in detail later in this article. We also have created processes that utilize waveguides for building integrated optical elements.

Optical waveguides for optical interconnections require large core sizes (cross-sectional areas) to facilitate high coupling efficiency between the vertical cavity surface-emitting laser (VCSEL) and the waveguide or between a multimode fiber and the waveguide. They also need to be thermally stable to 200°C in order to withstand the soldering processes that are used in assembling the waveguide structures.[7] There are half a dozen or so material systems that have been used to build integrated optical elements for OEICs. The silicon-based materials include silica ($SiO_2$), silicon nitride ($Si_3N_4$), silicon oxynitride ($SiO_xN_y$), and of course silicon itself, and they are relatively easy to integrate with silicon-based integrated circuits (ICs). These materials support low propagation losses on the order of 0.1 dB/cm, but the waveguides are often planar and thin, making them difficult to couple into, and there exists only a small range of possible refractive indices for waveguide formation. Other material systems such as gallium arsenide (GaAs), indium phosphide (InP), and lithium niobate ($LiNbO_3$) all exhibit higher propagation losses (from 0.5 up to 3.0 dB/cm) and suffer from a limited range of refractive indices. Polymer systems including polyimides, olefins, acrylates, and polycarbonates have processes compatible with most ICs, support low propagation losses similar to that of silicon-based systems, and have the widest range of possible refractive indices. Polymers also display a strong thermo-optic effect and can be doped to become electro-optically active.[8] At APL, we have worked with titanium in-diffused $LiNbO_3$, the silicon-based materials system, and various polymers in an effort to support OEIC hybridization levels 2 and 3. Our most promising results to date have been with polymers, and our work with integrating these waveguides also is presented in this article.

## LEVEL 2 OEIC: DIE-LEVEL OPTICAL INTERFEROMETER

A highly sensitive, die-level optical interferometer could offer a unique method for measuring nanoscale physical distances with applications throughout the optoelectronics industry. By definition, interferometry is the technique of superimposing two or more waves to detect the differences between them. An interferometer built on this principle can be used for optical metrology,

**Table 1. Electronic and photonic hybrids.**

| Hybridization level | Complexity | Cost | Size |
|---|---|---|---|
| Level 1: Splicing packages/chips | Low | High | High |
| Level 2: Chip-to-chip attach | Medium | Medium | Medium |
| Level 3: Hybrid integration | Medium | Medium | Low |
| Level 4: Heteroepitaxy | High | Low | Low |

which is a highly precise, noncontact method for measuring distances. To build a micro-sized, self-contained, die-level optical interferometer would require a light source, optical elements such as lenses and mirrors, a sensing device, and a level 2 OEIC package that could accommodate both electrical and optical components. Once realized, this die-level optical interferometer could revolutionize the application and performance capabilities of many microelectromechanical systems (MEMS), which often require accurate physical measurements.

Researchers at both The Johns Hopkins University (JHU) and APL have been working with MEMS devices in an effort to leverage some of their unique properties for sensing and/or actuator applications. A MEMS device uses micrometer-sized physical elements that display both electrical and mechanical properties that are functions of each other. Thus, a single feature within the device, such as a microbeam made out of polysilicon and anchored at only one end of the beam, can be used for both its ability to mechanically deflect and its ability to conduct an electrical charge. Interdigitated beams or "fingers" can be designed to sense some physical property, such as an acceleration vector, or they can be used as tiny "electric motors" that can drive some other part of the device. Many of these MEMS devices rely on the accurate measurement of a micro-sized mechanical displacement. In the case of a MEMS accelerometer, the amount of deflection of the finger structures correlates to the acceleration. Our goal was to meet this measurement challenge by creating the die-level optical interferometer.

Measuring mechanical displacement in MEMS devices through capacitive readout techniques is the current industry standard. This approach is limited by the need to overcome the parasitic capacitance, which often requires altering the mechanical structure. In some accelerometers, 75% of the surface area is occupied by sense and drive finger geometries. Optical interferometry offers a highly sensitive method for optical detection of mechanical deformation with MEMS devices but can be difficult to employ. To enable MEMS optical detection techniques, the MEMS devices must change reflectivity when they move. These reflectivity changes can come from a simple mechanism, such as reflective coatings that are masked and unmasked by the MEMS motion, or they can be created by more complex mechanisms, such as subwavelength gratings.[9] Beam deflection is another popular approach for optical detection. This method monitors the motion of a beam reflected off of the MEMS device. Thus, it is possible to build the MEMS such that there is a "mirror" surface that reflects light as a function of motion. The next challenge for optical sensing is the architecture of the optical interferometer itself.

Peregrine Semiconductor's ultra-thin silicon (UTSi)-on-sapphire complementary metal-oxide semiconductor (CMOS) process provides a transparent substrate that allows for a unique advantage to MEMS sensing in silicon on sapphire (SOS). In short, the light path can include the substrate when designing optoelectronic systems. Beyond that, the active silicon layer thickness of only 100 nm enables the design of hybrid, compact, and array-able die-level optical interferometers.[10–12] An optical standing wave can be created by taking a coherent light beam and reflecting it back onto itself. When the wave is reflected, it undergoes a phase shift of $\pi$. The position of the reflector in this system determines the phase relation between the incoming and reflected light waves. The phase relation between the two waves determines the magnitude of the electric field at a given point and hence the light intensity. Now consider a detector that is thinner than the wavelength of the light being used to produce the standing wave. It is possible for such a detector to sample the intensity of the standing wave contained inside of it. Standing-wave detectors have been presented as a method to build interferometers and displacement sensors.[13] A 100-nm-thick PIN diode fabricated in the UTSi-on-sapphire technology can act as a standing-wave detector and be used to build an interferometer.

The various components of our die-level optical interferometer are shown in Fig. 1. It is a typical Fabry–Perot design in which the interference is caused by the changing path length between two beams in an optical cavity (in this case between the MEMS structure and the substrate). The VCSEL diode is our light source and was procured from Emcore configured in a $1 \times 4$ array. The micro-lens was supplied by MEMS Optical, which used its patented grayscale imaging technique to etch the desired profile into fused silica. We diced the micro-lens substrates down into $1 \times 4$ arrays to match the VCSEL die. As previously mentioned, our UTSi-on-sapphire design was fabricated by Peregrine Semiconductor. The package substrate itself is a low-temperature co-fired ceramic (LTCC) design that was built at APL, and all of the assembly was done at either APL or JHU. To date,

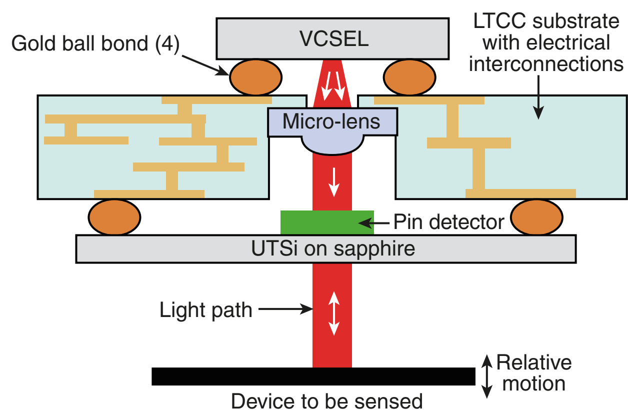


**Figure 1.** Optoelectronic package of a die-level optical interferometer with a collimated light source.

the LTCC substrate with all of the electrical interconnections has been successfully fabricated (a cross-section of which is shown in Fig. 2). The substrate also includes the cavity, which serves as a recessed mounting location for the micro-lens and a pathway for the light.

The VCSEL die has been flip-chip-bonded to the LTCC substrate, which verified the integrity of the "ceramic ledge" that sets the VCSEL to micro-lens distance at 100 μm. The VCSEL is shown in Fig. 3, and the micro-lenses are shown in Fig. 4. Future work will involve a new UTSi-on-sapphire design that includes a PIN diode with the I/O to accommodate flip-chip bonding to the backside of the LTCC substrate.

The process used to attach the VCSEL die to the ceramic optical package is commonly known as "flip-chip bonding to gold stud bumps." Gold balls (stud bumps) are first thermosonically attached to the thick-film metallization on the substrate by using a programmable automatic wire-bonding machine. The gold wire is cut just above the top of the gold ball, leaving only the ball, which could have been placed on either the substrate or the VCSEL die. We chose to place it on the substrate because the substrate, being larger, is easier to hold during the bonding process. The next step is to flip-chip-bond the substrate and VCSEL die together

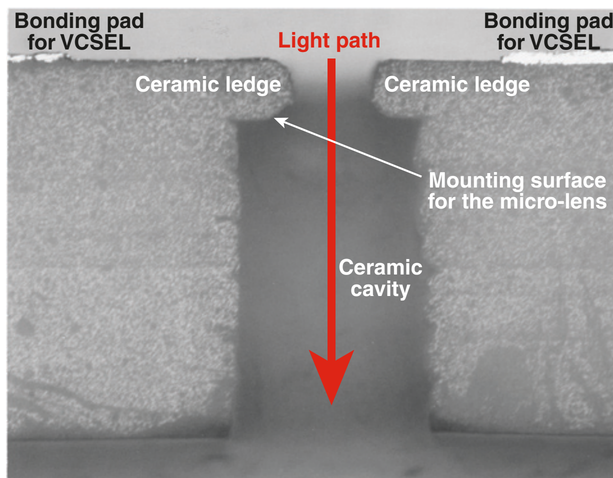


**Figure 2.** Photograph of a cross-section of the LTCC substrate.

**Figure 3.** Photograph of VCSEL (1 × 4 array).

**Figure 4.** Photograph of micro-lens arrays.

with a flip-chip-bonding machine. A calibrated optical system in the flip-chip bonder is used to align the gold balls to the bonding pads on the surface of the VCSEL die. The VCSEL die is lowered, facing down, toward the gold balls until contact is made. The flip-chip-bonding machine applies a pre-set constant force on the back of the VCSEL die while a heated work holder and a heated chip holder are activated to heat the devices to form a thermocompression bond from the tops of the gold balls on the substrate to the gold bonding pads on the VCSEL die.

## LEVEL 3 OEIC: INTEGRATED WAVEGUIDES

By definition, to achieve true level 3 OEICs, the package itself must include integrated optical components such as waveguides, switches, lenses, and mirrors. Recently, polymer waveguides have been successfully demonstrated in SU-8 (trademark of MicroChem Corp).[14] SU-8 has been widely used in MEMS applications as a negative tone photoresist because of high-aspect-ratio imaging with a nearly vertical sidewall. It is thermally stable and has good controllability of the film thickness from tens of micrometers up to several hundred micrometers.[15] The soft-baked SU-8 film can be used to make angled patterns through tilted exposure or grayscale lithography and can be exposed in hard contact with the mask to improve the fidelity of the pattern. We have worked with SU-8 for several years at APL with varying degrees of success.

One drawback of the integrated SOS-based Fabry–Perot interferometer similar to our die-level optical interferometer is the need to place the VCSEL immediately over the SOS (or UTSi-on-sapphire)

photodiode. This limits the technique to hybrid construction, in which the optical source and MEMS components are bonded to opposite sides of the sapphire substrate. It also makes it difficult to assemble more than one sensor on the same chip. It is envisioned that a more integrated solution would be similar to that illustrated schematically in Fig. 5. In the scheme in Fig. 5, both the mechanical structure and the photodiode are integrated into the SOS substrate. The VCSEL, together with any necessary collimating optics, is mounted on the front side of the wafer, and the light is controlled by the polymer waveguide. The latter would be part of the final package assembly. This concept would allow the use of commercially available 4 VCSEL chips; therefore, up to four MEMS subsystems in a single package would be possible. A similar approach could be used to build a Mach–Zehnder interferometer, as illustrated in Fig. 6. With the Mach–Zehnder design, the interference results from a small phase shift caused by a small change in optical path length in one of two collimated beams from a coherent light source.

Initial work on developing the necessary SU-8 polymer waveguides was based on delineating the waveguides by using an NOA61 epoxy bottom cladding layer on glass substrates.[16] The first waveguides had sloped side walls and a loss of ~0.3 dB/mm. Square-sided waveguides were produced by filtering the illumination to restrict the SU-8 exposure to wavelengths >340 nm. Cross-sections of high-aspect-ratio waveguides created with either the unfiltered or the filtered exposure are shown in Fig. 7. The filtering technique reduced the loss down to 0.15 dB/mm, as shown in Fig. 8, but resulted in poor adhesion between the SU-8 and the NOA61 layers because of additional film stresses.

The adhesion between the SU-8 and the bottom cladding or substrate was improved somewhat by using a double-exposure system that used both filtered and unfiltered illumination, although problems remained because of stresses caused by the differential thermal coefficient mismatch between the polymers and the substrate. Attempts to improve this mismatch by using epoxy-clad FR4 substrates[17] proved inconclusive. Many different test structures were fabricated using these SU-8 waveguides to determine their capabilities, one of which is shown in Fig. 9.

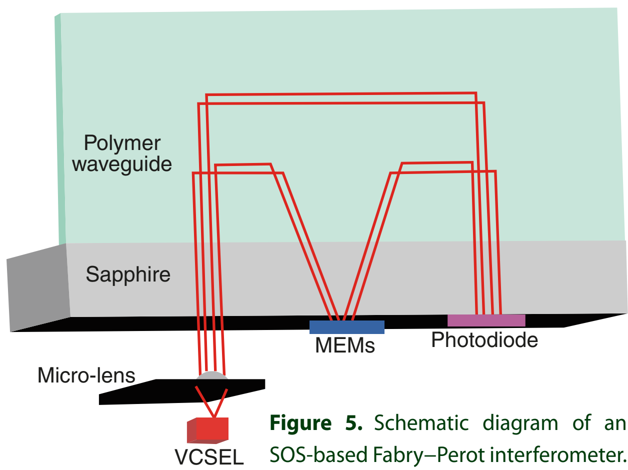


**Figure 5.** Schematic diagram of an SOS-based Fabry–Perot interferometer.

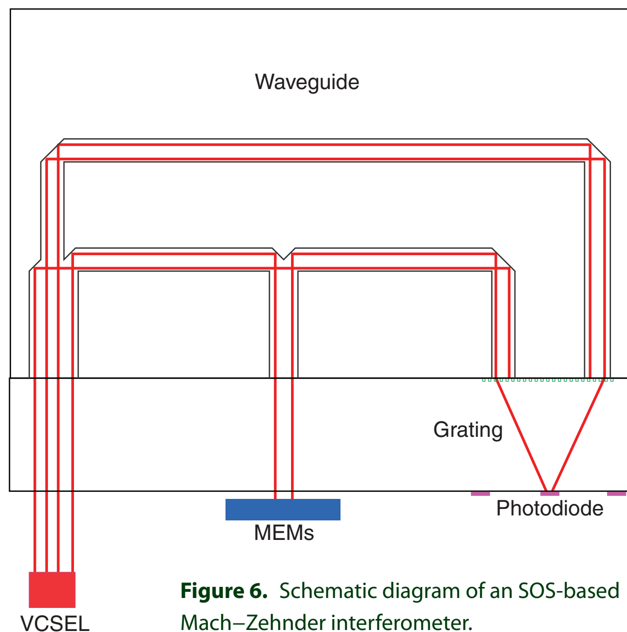


**Figure 6.** Schematic diagram of an SOS-based Mach–Zehnder interferometer.

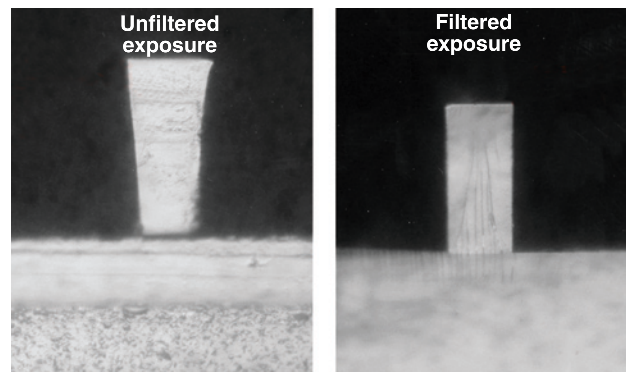


**Figure 7.** Photographs of SU-8 waveguide cross-sections.

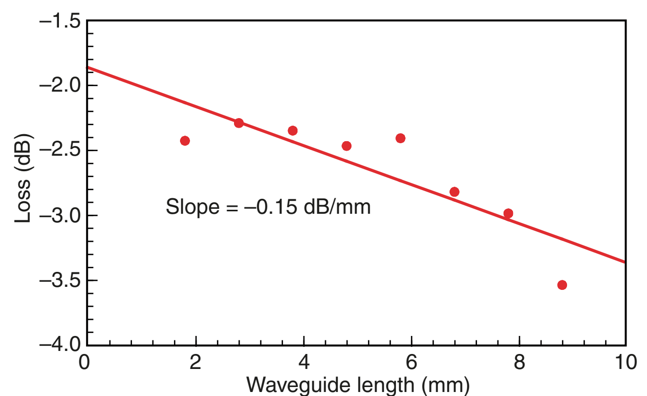


**Figure 8.** Measured propagation losses in SU-8 waveguides.

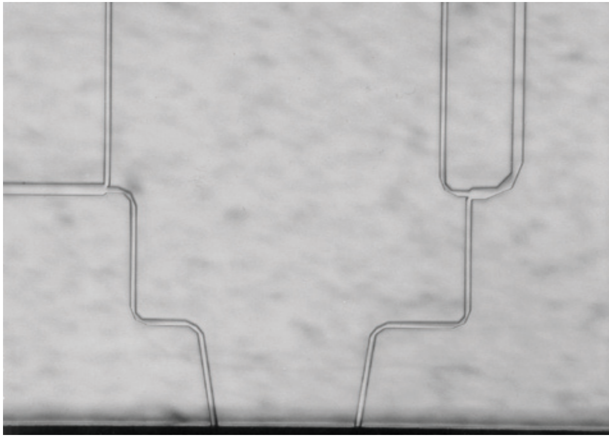

**Figure 9.** Photograph of an SU-8 waveguide test structure.

## CONCLUSION

It is 2008, and OEICs are becoming more prevalent in a wider range of applications. Electronics still dominates the computing and data-storage functions, but photonics with the dual capabilities of high speed and broad bandwidth is needed for signal transfer and some routine manipulations. APL is developing unique packaging approaches to accommodate the integration of both optical and electrical devices. We have designed and are building a die-level optical interferometer with the light source, a collimating lens, and the detector packaged as a single unit. We also have developed processes for building polymer waveguides and are characterizing them for integration with various MEMS sensors.

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