Reliable Miniature Electronic and Optical Interconnects for Low-Volume Applications

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At some level, all integrated circuit devices, passive devices, and optoelectronic devices must be interconnected together to function as a highly integrated electronic or optoelectronic system. As silicon-based device technologies have continued to evolve, the number of chip-level and package-level interconnections has increased dramatically while chip sizes have remained relatively constant. This dramatic increase in interconnection density has been enabled through the adoption of area array packages such as ball grid arrays and chip-scale packages. To accommodate these area array packages, today's printed wiring board fabrication techniques are featuring 100-μm (2-mil) lines and spaces as well as 0.25-mm-diameter (10-mil) blind and buried vias, both of which are necessary for high interconnection densities. Although the technology for wiring chips to packages and packages to boards for high-volume applications is relatively mature, it becomes increasingly ambitious to implement that technology for low-volume electronic applications. The nature of APL's wide range of innovative, miniature electronic development activities necessitates the use of high-density interconnection methods. This article focuses on APL's ongoing activity to develop high-density interconnection methods for use with low-volume, noncommercial electronic applications.

INTRODUCTION

Reliable, cost-effective miniaturized electronics systems are a key to APL's future business plans as they relate to military, homeland security, and space systems applications. The low volume and rapid turnaround requirements for some miniature electronic systems designed at APL preclude the up-front planning required

to both design and purchase devices that are manufactured specifically for ultra-miniaturized electronic systems. In addition, preparing commercially available integrated circuits (ICs) for extreme miniaturization can be quite costly. Back-end wafer processing for high-density applications such as die-thinning and solder-bumping IC bond pads add additional cost to the devices and typically require that the customer purchase at least one entire wafer. For the majority of devices, these back-end services are not even available. To meet the diverse requirements of APL sponsors, state-of-the-art techniques and innovative new solutions are being developed that address the need to provide cost-effective, high-density, miniature electronic packaging solutions.

MINIATURE ELECTRONIC PACKAGING TECHNOLOGIES

Currently, wafer-scale integration offers the highest available density in two-dimensional electronic packaging. In fact, an ever-increasing level of on-chip integration has postponed the widespread adoption of multichip packaging methods. The increased functionality available on a single IC chip has resulted in significant decreases in electronic system volume without the use of more advanced substrate and packaging technologies. However, in many applications where highly integrated devices are not available or packaged devices are too large for ultra-miniature applications, direct chip attachment techniques are still required.

Direct chip attachment assemblies involving more than one active device are often referred to either as multichip modules (MCMs) or as chip-on-board (COB) assemblies. The label MCM is typically reserved for multilayer thin-film circuits on silicon, multilayer thick film on ceramic, or thick film on multilayer cofired ceramic. The label COB refers to unpackaged ICs mounted directly onto printed wiring boards (PWBs). A newer designation, chip-on-flex (COF), refers specifically to bare ICs mounted on thin, flexible polyimide PWBs. APL has been consistently fabricating MCMs for space and medical applications since the late 1970s.[1] In recent years, APL has fabricated COB assemblies for both space and national defense programs. Currently, APL is moving more toward COF assemblies for their reduced size as well as the ability to conform these circuits to three-dimensional geometries.

There are two primary methods for interconnecting unpackaged ICs to the underlying circuit board: wire bonding and flip-chip bonding. Wire bonding is the traditional method for electrically wiring ICs to either packages or circuit boards. In this method, the backside of the IC die is first solder- or epoxy-attached to the substrate or package. In this case, a gold wire is first bonded to a pad on the IC and then to a pad on the underlying substrate. This is repeated for each IC bond pad. These wires electrically connect the device to the metal traces on the substrate or to the package leads. The wire-bonding process is depicted in Fig. 1. Flip-chip bonding involves the direct attachment of the top side of the IC die to the underlying substrate via a small bump contact. The substrate must have a pad layout that mirrors the pad layout for the chip so that when a die is positioned over the substrate and brought into contact with the substrate, a bond between chip and substrate can be formed. The flip-chip interconnection technique is illustrated in Fig. 2.

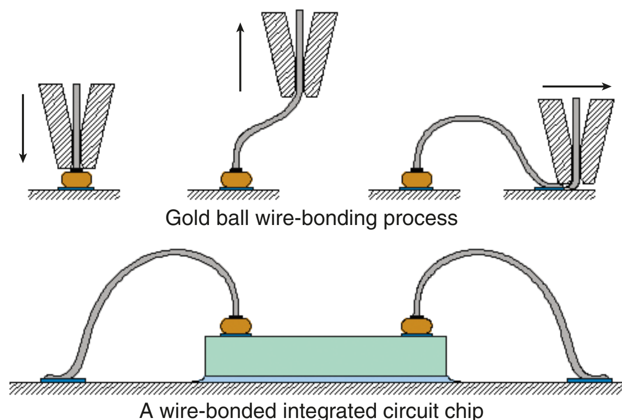

Figure 1. A gold ball wire-bonding process (upper) and a wire-bonded integrated circuit chip (lower).

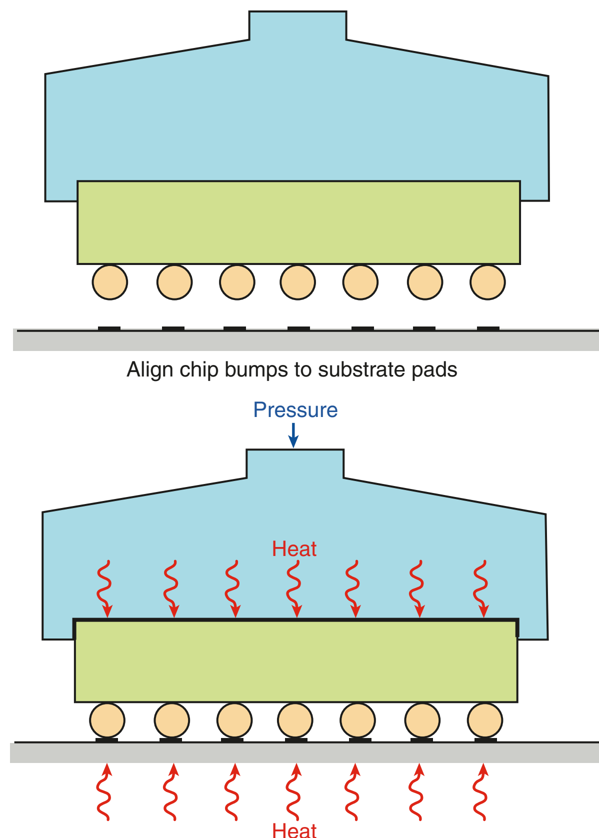

Figure 2. Flip-chip bonding process.

A small tradeoff in density for convenience can be gained with the use of chip-scale packages (CSPs) and ball grid arrays (BGAs). The CSP is typically used to package medium-scale IC devices (such as an operational amplifier and transistor arrays, etc.). CSPs are typically not more than 10% larger than the IC itself and offer a slightly smaller footprint than the BGA package. The leads are typically 100-μm-diameter solder balls that are located around the periphery of the package or in an area array. Large-scale ICs with higher numbers of inputs and outputs (signal processors, gate arrays, etc.) are more likely packaged in the larger BGAs. These packages also have ≥100-μm-diameter solder balls; however, they are arranged as an array to accommodate the increased number of inputs and outputs. Examples of CSPs and BGAs are shown in Fig. 3.

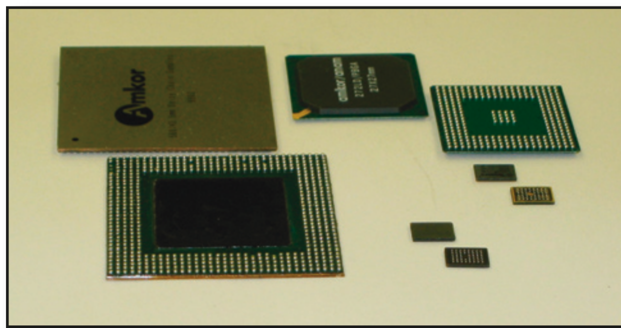

Figure 3. Examples of BGAs, microBGAs, and CSPs.

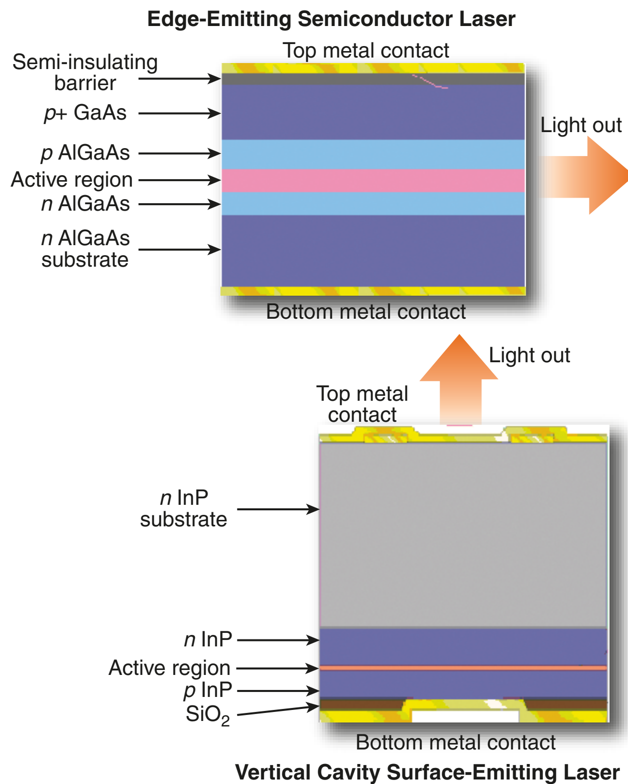

Figure 4. Differences between the EEL and VCSEL.

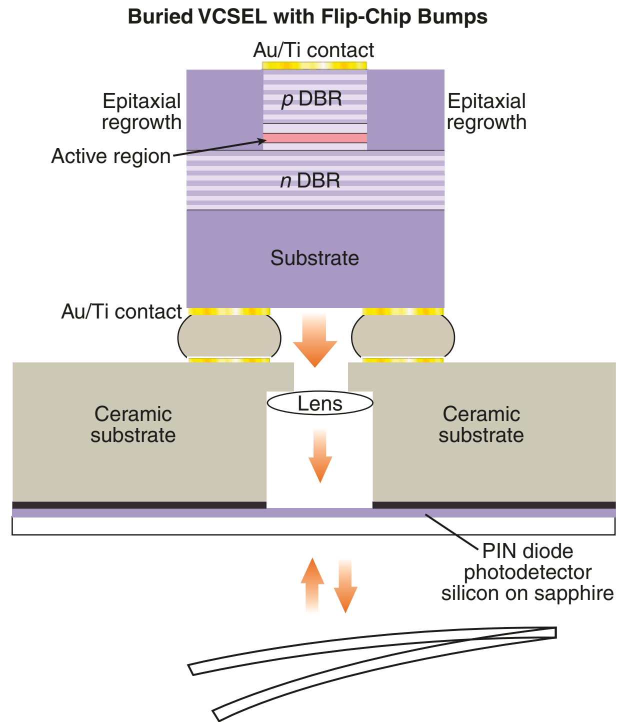

Figure 5. Flip-chip-mounted VCSEL used with a silicon-on-sapphire (SOS) PIN diode for motion detection. DBR, distributed Bragg reflector.

The technology for interconnecting highly integrated optoelectronic systems is at the present time relatively immature compared with that for electronic systems. Traditional interconnection schemes involved complex alignment of embedded optical fibers (usually in V-grooves etched in silicon) to edge-emitting laser (EEL) devices in that same silicon. With the advent of the vertical-cavity surface-emitting lasers (VCSELs), interconnection options have increased. The differences between VCSELs and EELs are illustrated in Fig. 4. VCSELs, along with thin-film optoelectronic components such as waveguides and coupling gratings, have facilitated the use of both photodetectors and photoemitters that are embedded directly into the substrate. With advancements in embedded waveguide techniques, flip-chip attachment of VCSELs is rapidly becoming the preferred interconnection method. A flip-chip style of VCSEL is depicted in Fig. 5 for a microelectromechanical motion-sensor application fabricated at APL.[2]

LOW-VOLUME, HIGH-DENSITY INTERCONNECT TECHNOLOGIES

Wire Bonding

In high-volume commercial applications, the principal die-level interconnection method used for high-density circuits is still the gold wire bond. There are two types of wire bonds, the ball bond and the

wedge bond. Both the ball bond and the wedge bond are welded to the aluminum metal bond pad on the IC by using ultrasonic energy and heat. This process is referred to as thermosonic gold wire bonding. Gold wedge bonding typically takes up less space on a bond pad; however, it has less flexibility than does the gold ball bond when bonding die with complex pad layouts or when bonding to substrates with irregular pad arrangements. For high input/output (I/O) density ICs, 18-μm-diameter (0.7-mil) gold wire is now the standard. With this thinner wire, gold ball bonds can easily be used on devices with 50-μm pads and 50-μm pad spacings.

Thermosonic gold wire bonding represents the most viable low-volume, high-density die-level interconnection technique. The technology is available to the occasional user in the form of a low-cost manual machine. For the frequent user, programmable automatic versions are available for only a modest capital investment. Thermosonic gold wire bonding is used for COB circuits and to a large extent for MCMs and COF assemblies. When wire-bonded assemblies are not placed in a package, the die and wire bonds are usually coated with an epoxy encapsulant to protect the tiny gold wires from mechanical damage while providing the IC some corrosion protection as well.

The limitations to wire bonding come to the fore in ultra-miniature applications where the substrate pad fanout (which grows with increasing I/O count) limits the number of die that can be colocated within a given substrate area. In addition, the height of the epoxy-encapsulated bond wires increases the overall thickness of the assembly. For high-speed applications, the lead inductance of bond wires often limits the maximum wire length allowed. There are instances where the front side of an IC chip must face the substrates, most notably in the cases of some optoelectronic devices. Wire bonding is impossible in these cases. All of the above limitations can be mitigated by using flip-chip technology.

Flip-Chip Bonding Process

The flip-chip bonding process requires a flip-chip bonder, which is a highly specialized tool. Unlike wire bonding, this bonding process is a "gang bonding": one where all of the device interconnections are made at once. Flip-chip bonders have various capabilities selected for maximizing the bonder's utility in a particular fabrication scenario. APL currently uses a low-volume research instrument that will essentially accommodate most if not all flip-chip modes of operation. Flip-chip bonders have a bottom heating chuck for vacuum-holding the substrate and an upper heated vacuum chuck for holding the chip to be attached. There is a split-prism optical system that allows the operator to align the bumps on the chip to the pads on the substrate. After the alignment process is completed and the temperature attains the desired value, the two chucks bring the substrate into contact with the bumped chip. The contact pressure is monitored via a pressure sensor or by a displacement sensor, depending on whether the bumps are to be welded or reflowed.

Flip-chip attachment is not new. IBM was making ICs with small solder bumps on IC bond pads as far back as the early 1960s.[3] Their process was called the controlled collapse chip connection or C4. Essentially, the IC with solder-bumped pads was mounted front-side down onto a ceramic or silicon substrate with corresponding pads and then heated until the solder reflowed, producing the necessary electrical connections. There were several reasons for the slow development of this early flip-chip technology. The initial reason had to do with the inherent unreliability of the process; as chips got bigger and the bond pads remained at the periphery, stresses on the small solder bumps became large. As the number of device I/Os increased, the cost of bare die testing went up as well. With the arrival of inexpensive, reliable plastic packaging combined with the ease of testing packaged ICs, flip-chip technology remained a relatively obscure technology. The increased use of the area grid array packages such as BGAs and CSPs reduced package sizes, further postponing the need for the end user to adopt flip-chip technology. Today there are few widespread commercial applications that require flip-chip assembly, and thus there is essentially no supply of unpackaged ICs available with solder bumps. This leaves the prospective flip-chip user two options: (*i*) purchase an entire wafer and have it bumped (often, the option to purchase an entire wafer is not available) or (*ii*) develop an alternative, lower-cost method that can use diced, unpackaged off-the-shelf IC chips. APL has taken the latter option to investigate innovative, cost-effective techniques to bump single-chip devices or wafers when available.

Low-Volume, Low-Cost Flip-Chip Technologies

Recently, one prime goal of the electronics packaging industry has been the adaptation of available bare, off-the-shelf ICs to flip-chip applications. In response to this need, several low-cost methods have been developed for applying conductive bumps to IC bond pads and, in turn, using standard flip-chip equipment to bond them to substrates. The most useful methods for implementing this goal are the wire-bond stud-bump approach and the electroless under-bump metallization (UBM) process.

Gold and Platinum Wire Stud Bumping

The stud-bump process is now incorporated in most automatic wire-bonding equipment. The technique for making the stud bump, basically a single-ended wire bond, is depicted in Fig. 6. After the bond is made and the wire is broken, a special tool is used to tamp down the bump so that the tops of all of the bumps are

coplanar. An optical micrograph of an array of gold ball stud bumps is illustrated in Fig. 7. The gold ball wire-bond stud bump is a suitable interconnection when both the device pads and the substrate pads are composed of gold. In that case, in a process called thermocompression flip-chip bonding, after alignment of the die to the substrate, the flip-chip bonder briefly heats both the lower and the upper chuck to ≈300°C. After thermal equilibrium is reached, the die is lowered toward the substrate. As the gold bumps contact the corresponding gold pads on the substrate, the applied pressure from the upper chuck is permitted to rise to a programmed set point. This set point equals the amount of pressure required to weld the gold bumps to the gold pads. The required bonding times and pressure are inversely related to temperature. Depending on the mismatch between the coefficients of thermal expansion (CTEs) of the die and the substrate, an underfill adhesive may be required to relieve stresses at the interconnections. The underfill adhesive serves to bond the chip to the substrate while simultaneously encapsulating the gold bumps. Both reliability studies and finite element analyses have shown that the use of underfill materials can significantly improve the reliability of the flip-chip interconnection.

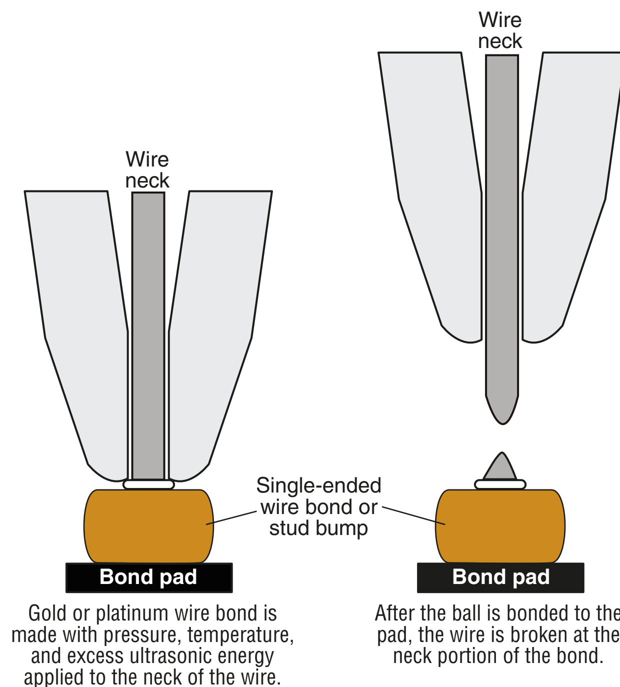

Figure 6. Process for making single-ended wire-bond stud bumps.

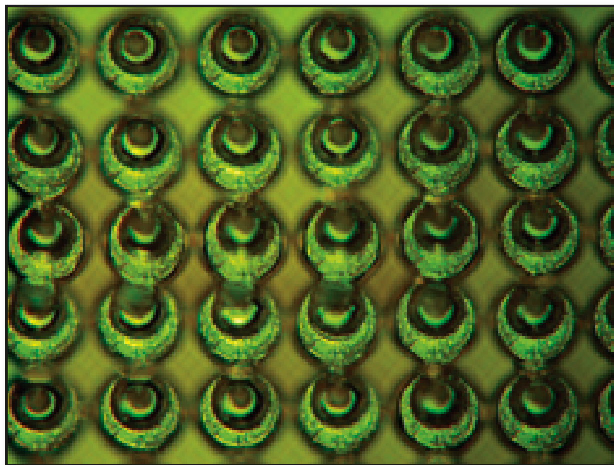

Figure 7. Array of single-ended gold wire stud bumps.

When using the gold stud-bump technique, thermocompression flip-chip bonding is only suitable when the stud bumps are made to gold pads. Most silicon ICs have aluminum pads and are not suitable for thermocompression bonding because of the rapid formation of aluminum–gold intermetallics at bonding temperatures. The most detrimental form of these intermetallics is Au_2Al (known in the industry as "purple plague"), which is present at >150°C and forms rapidly at temperatures of ≈300°C.

One solution to the purple plague problem is to use platinum bonding wire to form the stud-bump interconnection, which requires a different process than that used with the gold stud bump. In this process, the platinum wire is bonded directly to the aluminum bond pad. Because platinum is a harder metal than gold, it usually requires higher bonding temperatures and lower ultrasonic energy to prevent work hardening. Furthermore, because platinum, unlike gold, can be soldered with low-temperature solder alloys, the stud bump can be directly soldered to the substrate, which requires that the substrate have solder already applied to its pads. The best method for applying solder to the pad is via solder plating. In air, flux is typically required to ensure that the solder wets the platinum stud bump. To keep flux residues from contaminating the IC, the best approach is to use fluxless soldering. Fluxless soldering requires a steady stream of gas (typically nitrogen) to flow over the work area while the solder is reflowing. During the bonding process, the bonder maintains a steady pressure on the die while the temperature is ramped up to the reflow temperature. Reflow temperatures are typically >200°C for a short time and thus tend not to produce significant intermetallic growth at the platinum–aluminum interface.

There is another process whereby purple plague can be avoided when using gold stud bumps on aluminum pads. The bump-to-substrate electrical connection is made by using an anisotropically conductive adhesive (i.e., an adhesive with microscopically small, electrically conductive particles designed and introduced into the epoxy matrix at a density such that electrical conduction will occur only along one axis). The adhesive is placed everywhere underneath the die. When the chip is aligned with the substrate bonding pads, the flip-chip bonder brings the gold bumps into contact with the conductive particles. With pressure and heat applied, the

adhesive within the conductive particle matrix cures while the gold bumps are making electrical contact (via the conductive particles) to the substrate pad metallization. When the epoxy cures, the material shrinks, pulling the connections closer together and further improving electrical conductivity along the preferred axis. Because pressure is applied only in the *z* direction and pressure is required to facilitate the electrical connection, there is no conductive path between the adjacent gold bumps. A cross-sectional micrograph of a chip attached to a flexible substrate in this manner is depicted in Fig. 8. APL is currently evaluating this technique for a NASA sponsor.

UBM and Thermocompression Bonding

Another bump technology for flip-chip bonding first requires a UBM step. One such UBM process requires treating the bare aluminum pad with a zincating solution that improves the adhesion of the next metal layer, which is deposited by electroless plating of nickel followed by a thin layer of electroless gold. Because the nickel film can induce much stress, considerable care must be shown to avoid cracking the pad passivation on the chip. Solder can then be screen-printed onto the pads (if they are big enough), or a transfer approach can be used to place individual solder spheres onto the UBM. Once the solder is located on the device pads, it can be reflowed to the UBM. After the chip has solder bumps applied to its pads, it can then be placed by using a flip-chip bonder and soldered to an underlying substrate or package. This UBM process is currently being investigated at APL concerning the viability of plating single unpackaged IC chips.

The more interesting application of the UBM process is coupling it with the gold stud bump. In this case, the gold stud bump or single-ended wire bond is made to the electroless gold portion of the UBM on the IC bonding pads. Because the gold is in contact with the nickel and not the aluminum, there are no detrimental intermetallic compounds formed when using thermocompression flip-chip bonding to interconnect the die to the substrate.

Indium Bump Plating for Optoelectronic Detectors

As part of an indium phosphide (InP) particle detector array fabricated for an external sponsor, APL developed an indium bump electroplating process.[4] Indium bumps are an excellent flip-chip bump material for optoelectronic materials such as InP semiconductors because they can be cold-bonded (i.e., bonded at room temperature). The desirable properties of InP semiconductor detectors can be degraded when heated to temperatures typically used for flip-chip bonding. The detector had a requirement for bonding an InP detector with a large array (64 × 64) of small indium bumps (26 μm wide by 38 μm long by 23 μm high) to an application-specific integrated circuit (ASIC) signal processing readout chip. Figure 9 shows a scanning electron microscope (SEM) micrograph of indium bumps on a simulated detector chip. A special flip-chip underfill process had to be developed because the cold-welded indium bumps had almost zero strength after bonding. The underfill process required the use of an adhesive that was placed on the bottom ASIC device after alignment but before bonding. The two chips were brought together, and pressure was applied to squeeze out the adhesive between the indium bumps. After cold-welding the bumps, the temperature was raised high enough to cure the adhesive but not so high as to affect the properties of the InP detector. Figure 10 is a photograph of the InP detector bonded to a glass substrate.

Flip-Chip Bonding of Thinned ICs to Flex Circuits

Currently, APL is actively pursuing the development of ultra-thin flexible electronic assemblies that are

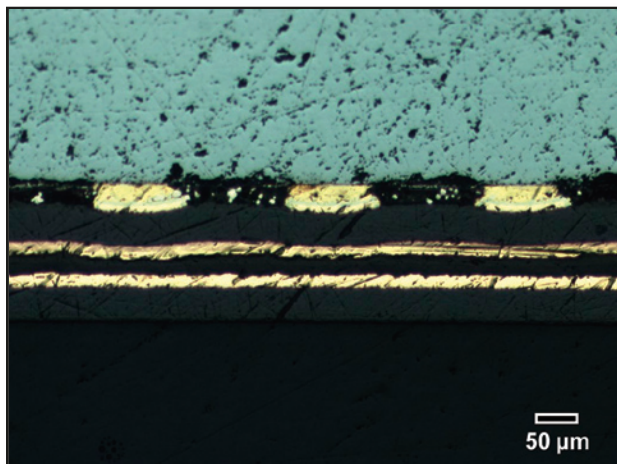

Figure 8. Flip chip with gold stud bumps bonded to gold-plated flex substrate by using anisotropic conductive adhesive.

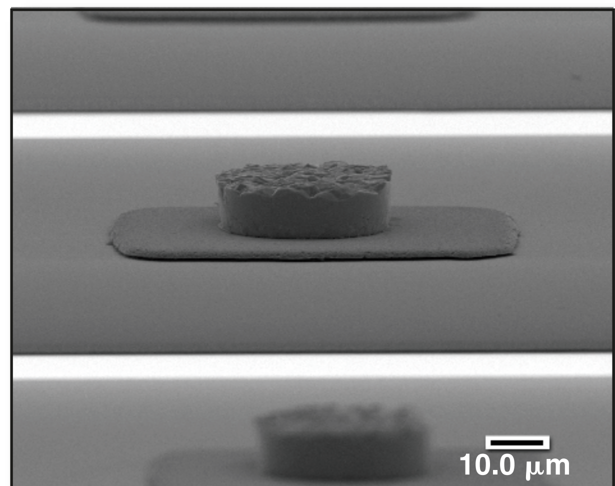

Figure 9. SEM photomicrograph of indium stud bump on InP detector array.

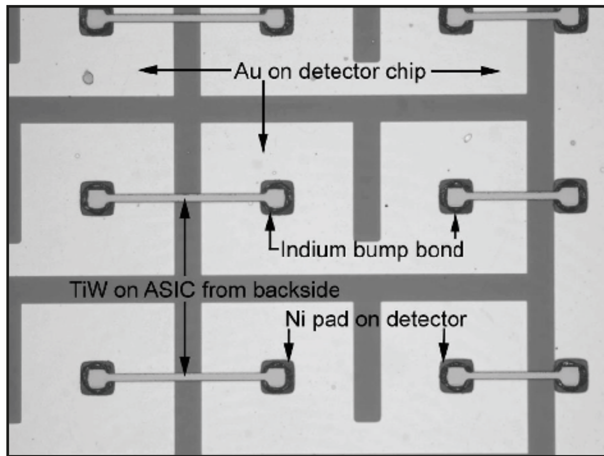

Figure 10. Photograph of InP detector bonded to a glass substrate.

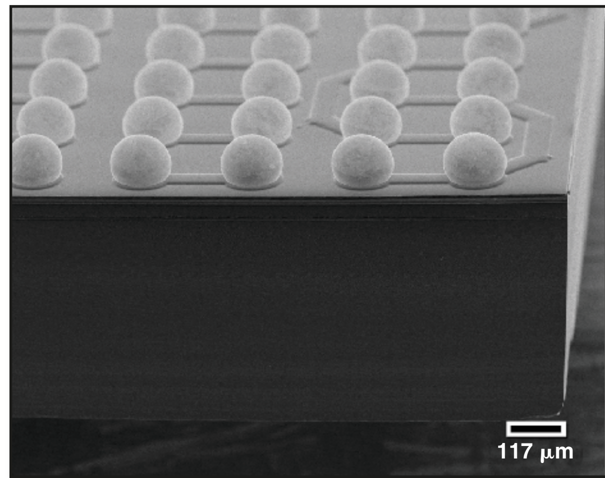

Figure 12. SEM photomicrograph of a solder ball array with 50 μm of silicon on the handle before flip-chip attachment. The handle is chemically dissolved away after the solder reflow process is completed.

≤0.25 mm in thickness, including all active and passive components. Circuits of this thickness or thinner can be formed around cylindrical objects to form a type of smart skin with the potential for significant data-processing capability. Achieving these thickness dimensions requires that ICs be thinned to a thickness of ≈2 mils (0.05 mm). Multilayer flexible wiring board material must be used to keep the board both flexible and under 6 mils (0.15 mm) thick. Thinned ICs mounted to the substrate must then be flip-chip-attached to remain within the desired thickness range. A picture of the test assembly used to develop this process with thinned die and a flexible circuit wiring board is illustrated in Fig. 11. The test assembly featured an array of 1368 solder connections. All of the solder joints were daisy-chained together to ensure that all connections were soldered after assembly and to test for failures that occurred during subsequent temperature cycling. An SEM micrograph of the array of solder bumps on the chip is shown in Fig. 12 along with the handle used to process the device. Handle is the term used for silicon blank that is adhesively attached to the die to aid in the die-thinning and flip-chip attachment processes.

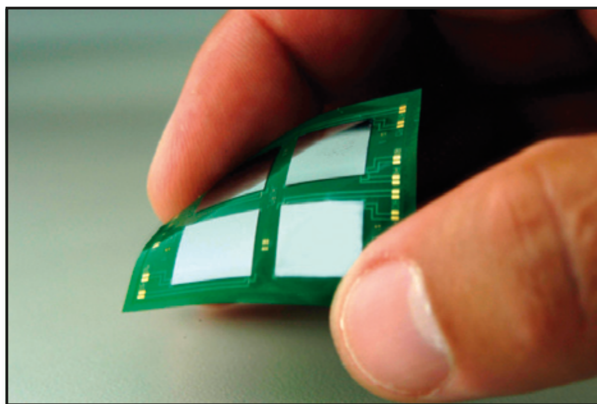

Figure 11. Ultra-thin silicon on a flexible circuit board. The chips and flex board are each 50 μm thick, and each chip contains 1368 solder bumps.

RELIABILITY OF FLIP-CHIP AND AREA ARRAY SOLDERED INTERCONNECTS

Low-Cycle Fatigue Analysis Method for Soldered Interconnections

Many flip-chip interconnects require the use of an underfill epoxy because of the CTE mismatch between the silicon and most conventional substrate materials. For most tin–lead soldered interconnections, a large CTE mismatch coupled with a large thermal excursion (i.e., large strains) will result in a short fatigue life, with fatigue life representing the number of temperature cycles to failure. For the flip-chip solder joint, fatigue failures are exacerbated by the fact that this joint is a smaller one, so that once crack propagation is initiated, it will not take long for the crack to propagate through the joint.

Temperature cycle testing is a common accelerated life testing approach to evaluate the quality and service life of a soldered interconnection. Many military and NASA standards require temperature cycling to screen for bad solder connections. Engelmaier[5] derived a thermal fatigue model for eutectic tin–lead solder based on the Coffin–Manson equation of the following form:

$$N_f = \frac{1}{2}\left[\frac{\Delta\gamma}{2\varepsilon_f}\right]^{1/\beta}, \quad (1)$$

where N_f is the number of cycles to failure, ε_f is the fatigue ductility coefficient, β is the fatigue ductility exponent, and $\Delta\gamma$ is the equivalent plastic strain per cycle.

Engelmaier concluded from solder fatigue data from Wild[6] that a reasonable correlation of his model to these data could be found if the fatigue ductility exponent could be represented by the following equation:

$$\beta = -0.442 - 6 \times 10^{-4}\, T_s + 1.74 \times 10^{-2} \ln(1 + \nu), \quad (2)$$

where T_s is the mean cyclic solder-joint temperature and ν is the cyclic frequency (cycles per day). The fatigue ductility coefficient was given by:

$$2\varepsilon_f \approx 0.65. \quad (3)$$

For most situations, finding the equivalent plastic shear strain requires the use of the finite element method. This analysis, in turn, requires a time-dependent, nonlinear elastic-plastic analysis based on experimental stress–strain data followed by a creep strain analysis. Creep is the time-dependent material deformation that occurs when a material is subject to a load. The creep analysis estimates the amount of nonrecoverable strain occurring during high-temperature hold periods. The total equivalent plastic strain is the sum of the time-independent plastic strain (otherwise known as primary creep) and the time-dependent creep (secondary creep). The plastic analysis was performed by using a piecewise continuous stress–strain curve constructed from data found in Ref. 7. The creep law and creep strain data for several tin–lead solders used in this analysis can be found in Ref. 8. To correctly use Eq. 1 to estimate fatigue life, the finite element model must be able to simulate the total equivalent plastic strain from the beginning through the end of one complete cycle. A typical cycle might include a ramp from room temperature to an upper temperature limit followed by a period of dwell at this temperature. This would be followed by a ramp to the lower temperature limit and a dwell at this lower temperature. The cycle then would conclude with a ramp back to room temperature. The accumulated equivalent plastic strain over this cycle would be the plastic strain used in Eq. 1.

Analysis of Fatigue Life for Temperature-Cycled Ultra-Thin Flip-Chip Circuits

The finite element model and the Engelmaier fatigue equation were used to compare the reliability of the temperature-cycled solder joints for several candidate underfill epoxies recommended for underfilling the ultra-thin assemblies discussed above. The underfill adhesive occupies the space between the chip and the underlying substrate and, in most cases, serves to reduce the strain on the solder joints. The candidate epoxies must both be flexible to allow for bending and provide strain relief for the array of tiny solder joints. The results of these analyses were compared with actual test data from temperature-cycling studies performed on the ultra-thin assemblies. The temperature cycle used to test the reliability of these ultra-thin flip-chip assemblies involved an upper temperature of 125°C and a lower temperature of −40°C. The ramp time between the upper and lower temperatures was 15 min, with 15-min dwell times at each extreme allowing for ≈24 temperature cycles per day. Because all of the 1368 solder joints were daisy-chained together on the test assemblies, the failure of a single solder joint would produce an open circuit. The continuity of the solder-joint chain was monitored via automated testing equipment. The number of cycles to failure was noted to occur on that cycle when an open circuit in the daisy-chain was detected.

Finite element analyses were performed to estimate the accumulated equivalent strain for one complete cycle for the conditions discussed above. A one-quarter symmetry model was used for the analyses and is depicted in Fig. 13. The mesh for the finite element model was relatively coarse throughout most of the model but was densest in the area near the corner solder joint farthest from the neutral axis. Because of the large number of solder joints (342) to be modeled and the computational demands of this nonlinear, time-dependent analysis, the mesh was coarser than is desirable for accurately estimating solder-joint fatigue life. However, the model was deemed suitable for selecting that underfill epoxy that would provide the most strain relief for the encapsulated solder joints. The analyses were divided into two distinct cases: one with an underfill epoxy and one without (baseline). An example of an equivalent plastic strain contour plot for the solder joint farthest from the neutral axis is depicted in Fig. 14. In all cases, the equivalent plastic strains in the solder joint were largest near the silicon substrate.

Four different underfill epoxies were evaluated by using finite element method techniques. The properties of these epoxies are presented in Table 1 along with the estimated and actual number of cycles to failure for each material. Epoxy 1 was a commercially available material that was recommended for underfilling flip-chip devices. It was initially compared with specimens that had no underfill epoxy. After temperature cycling baseline assemblies with no underfill and those underfilled with epoxy 1, it was interesting to note that the underfilled assemblies failed sooner than did those assemblies without underfill. Three additional epoxies were selected and analyzed by using finite element methods. Although the analysis data could not be directly correlated to actual cycles to failure, the analyses did point to those underfill materials that would perform better. The analysis indicated that epoxy 4 would significantly improve the fatigue life of the soldered interconnection over the

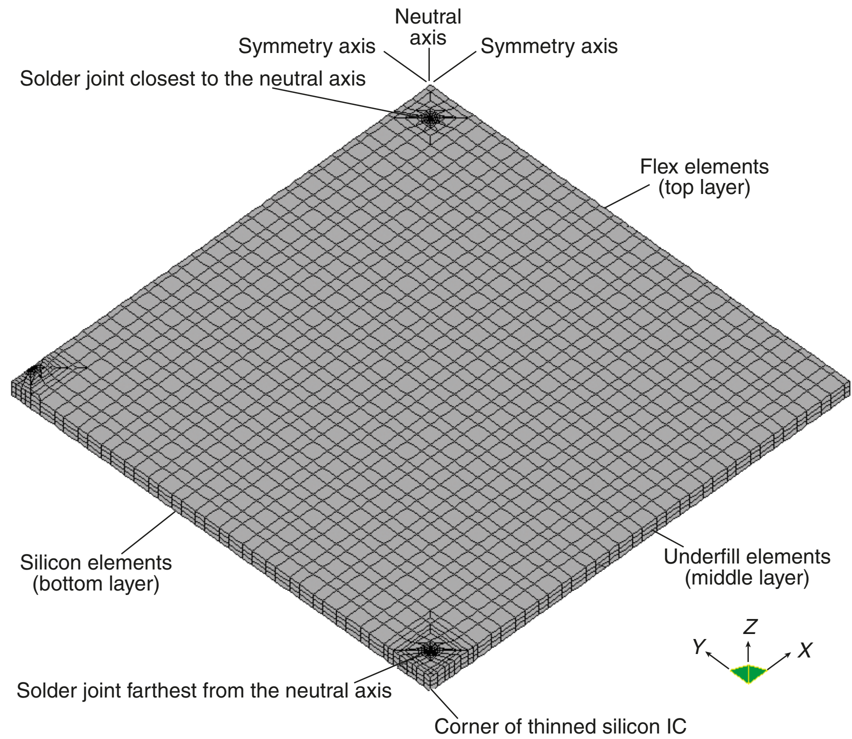

Figure 13. Finite element model used to estimate the equivalent plastic strain on solder joints for ultra-thin silicon bonded to flex circuit resulting from temperature cycling from –40°C to 120°C.

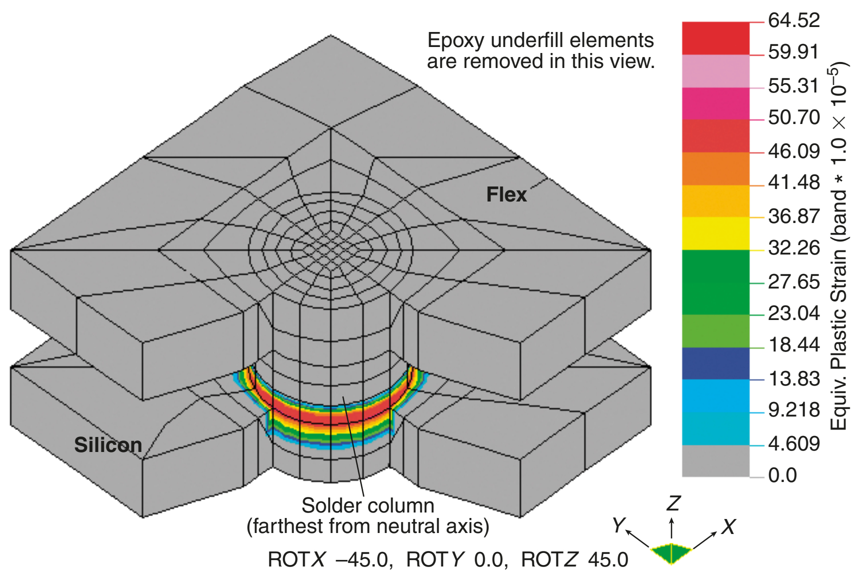

Figure 14. Cumulative equivalent plastic strain for the solder joint farthest from the neutral axis for one complete temperature cycle. Plastic strain then was used to estimate the cycle life (N_f) of the solder joint.

Table 1. Underfill epoxy material properties and projected cycles to failure.

Properties	No underfill	Underfill epoxy 1	Underfill epoxy 2	Underfill epoxy 3	Underfill epoxy 4
Young's modulus (GPa)		0.26	5.6	3.56	5.0
CTE (ppm)		40/94*	45	36	30
T_g (°C)		0	140	126	163
Equivalent plastic strain		1.97×10^{-2}	8.19×10^{-3}	2.42×10^{-3}	1.70×10^{-3}
Estimated N_f	≈310	≈1,500	≈11,500	≈190,000	≈424,000
Actual N_f	1,260	1,032	Not tested	Not tested	>4,000

*Below glass transition temperature (T_g)/above T_g.

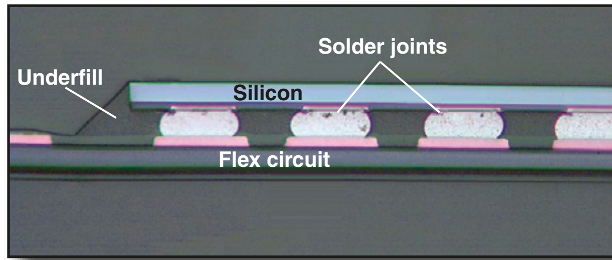

Figure 15. Cross-sectional view of an underfilled ultra-thin assembly before temperature cycling.

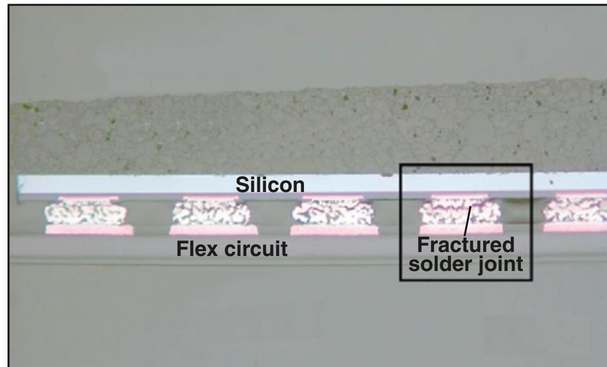

Figure 16. Cross-sectional view of an ultra-thin underfilled flip-chip assembly after 1080 temperature cycles between –40°C and 125°C.

original underfill material selected. As a result, when assemblies that used underfill epoxy 4 were tested, the number of cycles exceeded 4000 before the testing was ended without a recorded failure.

The results of the analysis indicate that an underfill epoxy with a lower CTE will perform better than one with a higher CTE independent of the material stiffness. Figure 15 represents a cross-sectional view of one of the ultra-thin assemblies underfilled with epoxy 1 before temperature cycling. Figure 16 shows a cross-sectional view of the same epoxy after temperature cycling. In this figure, one solder joint is highlighted that is exhibiting a crack that had propagated through the entire joint, producing an open circuit. It is interesting to note that this fracture in the solder occurs closest to the silicon substrate, the location of the largest equivalent plastic strains as predicted by the finite element analyses.

SUMMARY

Innovation and skill in fabricating miniature electronic systems has always been a mainstay of APL. The demand for even smaller, lighter, and thinner electronics systems is proving to be the entrée to new and challenging business opportunities with the Department of Defense and NASA. The requirements of miniaturization are directing APL's efforts to developing innovative new techniques, particularly in the areas of single-chip bumping and ultra-thin flexible circuit technology. Electronic assemblies that utilize flip-chip technology offer the highest circuit density short of full wafer-scale integration. Single-chip bumping will be critical for fabricating ultra-miniature circuitry because commercial manufacturers have little financial incentive to address the needs of fast-turnaround programs that require limited quantities of prebumped IC chips. APL has successfully used the gold stud-bump method in conjunction with an anisotropically conductive epoxy to bump and interconnect a commercially available bare IC die. The electroless UBM plating process is currently being evaluated on single chips in order to facilitate the thermocompression flip-chip bonding of conventional aluminum metallized ICs. Indium bump plating of InP detector arrays and the flip-chip attachment of a VCSEL have demonstrated APL's capability in fabricating substrate-level integrated optoelectronic systems.

The most recent advancement in miniaturization involves the ultra-thin, silicon-on-flex technology. Metallized and patterned thin silicon (≈50 μm) substrates have been successfully flip-chip-attached to thin flex substrates (≈50 μm), underfilled with epoxy, and temperature cycled between 125°C and −40°C for >4000 cycles without a failure. The use of the finite element method was demonstrated as a useful aid in the selection of an underfill adhesive to improve system reliability.

APL has demonstrated the ability to use skill and innovation to develop several low-cost approaches to single-chip bumping and flip-chip attachment for use in thin and ultra-thin microelectronic assemblies. Numerous APL sponsors can benefit from these developments, particularly in those areas where miniaturization offers a distinct advantage.

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