Technology Advances and Globalization in Electronic and Electro-Optical Packaging

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*S*emiconductor technology and integrated optical device technology, coupled with modern, miniaturized packaging, form the backbone of today's high-performance electronic and electro-optical systems. This article explores some current and future electronic and electro-optical device technologies and their impacts on APL. It also explores the ramifications and impact of globalization on the accessibility of this technology to APL. In a similar vein, the article describes the latest trends in packaging and how packaging is essential to the development of high-performance systems. Packaging has been fully globalized for many years, and thus the question is not when globalization will occur but rather how to best exploit the global packaging technology and keep critical access for APL. The packaging discussion also focuses on important APL advances in optical waveguides and transitions as well as on advanced flexible-integrated-circuit assemblies.

INTRODUCTION

Electronic packaging and electro-optical packaging are enabling technologies for the world's electronic and integrated circuit (IC) industries. IC technology and semiconductor devices of all types (e.g., basic logic to light-emitting diodes and lasers) are appearing in the marketplace, and the growth and importance of electronics technology are expanding without bounds. Moore's Law[1,2] still holds (and promises to hold for the foreseeable future), and the world's marketplace is filled with not only new devices and products but also new materials (e.g., silicon carbide,[3] organic semiconductors,[4] etc.).

Given this diverse and rapidly expanding semiconductor technology, the challenges for electronic and electro-optical packaging are rapidly increasing, forcing major changes in packaging methods and materials. Packaging is defined as the methodology for connecting and interfacing the IC or semiconductor device technology with a system and, ultimately, the physical world. Inherent in the packaging concept is the preservation of IC performance while satisfying the interface requirements with a structure that is reliable and meets the constraints of size, cost, and environmental operability. In today's

electronic world, devices must be portable and equipped with wireless connectivity. Along with portability and wireless connectivity go several other system-level factors (e.g., small size, low weight, low power, low cost, high functionality, ease of use, and reliability). These system-level drivers pervade electronic products from personal computers and cellular telephones to military-fielded hardware, biomedical instrumentation, and space-flight hardware. Small, lightweight, low-cost, highly functional, reliable, and connected electronic products are crucial to all current and future electronic and electro-optical system applications.

In a recent article,[5] I discussed the major shifts in electronic devices and packaging. Current and future trends were presented along with the impacts of the trends on APL and its investments for the future. In the present article, these and other trends in electronic and electro-optical packaging are discussed in greater detail, including the impact of globalization on APL's ability to have access to technology at the needed level of detail.

SEMICONDUCTOR AND OPTICAL DEVICES

Current IC technology continues to evolve from its initial beginnings in 1958.[6] Moore's Law for devices, as mentioned above, is continuing to hold: the number of active devices (transistors) on a single chip has been doubling approximately every 2 years.[2] Today, commercial ICs exist with $>10^8$ devices in chip areas <100 mm^2. For example, the Intel Pentium D dual-core processor debuted in 2005 with 230 million transistors based on 90-nm technology. Ninety-nanometer (90-nm) technology refers to the effective length of the channel (the distance between the source and the drain) in metal-oxide-semiconductor (MOS) devices. A representative cross-section of the standard MOS field-effect transistor (FET) is shown in Fig. 1a. This basic structure has existed since the late 1960s, when the self-aligned polysilicon-gate process replaced the initial hard-to-align metal-gate-electrode process.[7] To improve performance, a metal capping layer (as shown in Fig. 1b) was added over the polysilicon in the 1980s. Since that time, most performance improvements have been achieved by reducing the gate length and thinning the gate dielectric (SiO$_2$) to increase the electrode coupling to the channel. Increasing the gate coupling allowed reduced gate voltages and lower-power operation coupled with faster switching speeds (shorter channel). However, thinner standard gate oxides have led to increased leakage currents. In 2006, the Intel Itanium 2 (dual-core) processor launched with 1.72 billion transistors again using 90-nm process technology. Since 2006, Intel has introduced many other device families using both 90-nm and 65-nm technologies. In September 2006, Intel announced a new 45-nm technology using a high-dielectric-constant gate insulator with a composite-metal-capping scheme

as shown in Fig. 1c. Touted as the biggest advancement in transistor technology since the introduction of the polysilicon-gate process with significant enhancements in switching speed and significant reductions in leakage and quiescent power consumption, the new gate structure paves the way for even denser, more efficient ICs. The gate structure in the new Intel process uses hafnium oxide as the gate dielectric. The HfO$_2$ material is typically deposited by using metallo-organic chemical vapor deposition. The electrode for these HfO$_2$ gate dielectrics include sputter-deposited (DC magnetron) tantalum nitride (TaN or Ta$_{1-x}$N$_x$) or tantalum ruthenium and tantalum ruthenium nitride alloys. The exact details of the process used by Intel are proprietary. For example, Intel has a 32-nm technology planned for introduction in 2009 and a 22-nm technology slated for 2011. Given these gate lengths, the number of devices on a fingernail-sized piece of silicon (80 mm^2) could easily reach 100 billion early in the next decade. When IC devices reach these densities, a critical problem is heat generation and removal. Current Pentium chips can have circuit hot spots with heat fluxes higher than those encountered in rocket engines; thus, thermal management is paramount to device function and system reliability. Device packag-
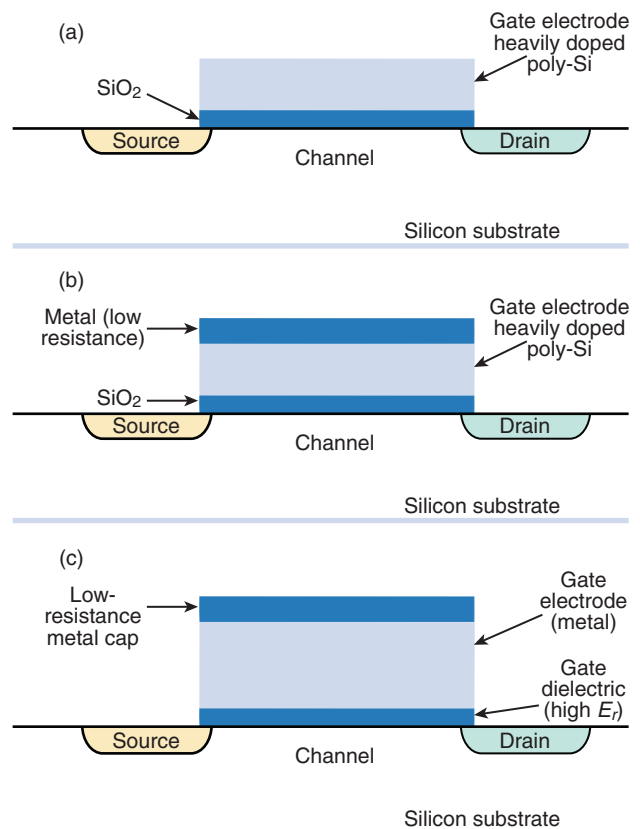

Figure 1. Schematic representations of gate structures on MOS FETs. (a) Polysilicon gate. (b) Polysilicon gate with low-resistance capping layer. (c) Advanced metal gate and high-E_r insulating layer.

ing is crucial to solving this issue. Handling high thermal loads in electronics produces a range of solutions from thermally conductive die-attachment materials to active cooling by using fluids and sprays. Because of the myriad applications for high-heat-dissipating chips at APL, internal efforts have focused on passive cooling approaches such as thermally conductive materials infused with carbon nanotubes (CNTs), diamond heat spreaders, and thermally anisotropic nanowire interposers.[8] The ultimate answers to the heat and density problem are new devices and structures that dissipate less energy but occupy footprints that are the same or smaller than current footprints.

Alternate Materials

In addition to the hafnium-oxide-based gate-electrode structure in Intel's advanced 45-nm technology, other material choices are being made throughout the semiconductor industry. In high-performance devices, the standard aluminum silicon alloy chip metallization is already being replaced by copper, which has much higher electrical conductivity.[9] On-chip inorganic-dielectric layers (SiO_2 and Si_3N_4) between the multilayer metallizations are being replaced by organic materials with lower dielectric constants. Materials such as polyimide, benzocyclobuten, or Teflon-based compounds are routinely being used to increase IC performance. The ultimate performance enhancement would be the use of air or a vacuum as the dielectric material between the metal lines. Topologies and processing methods such as the easy removal of sacrificial spacers would need to be developed, but the potential payoff in enhanced device performance could be significant.

In addition to using organic layers as inorganic dielectric replacements, scientists are working to develop fully organic transistors. These organic structures promise low cost, ease of manufacture with more energy-efficient processes, and better environmental and biological compatibility. In particular, organic thin-film transistors (TFTs) are of interest for a variety of large-production-volume electronics applications, such as displays,[10] sensors,[11] and electronic tags and bar codes.[12] Given the current performance limitations with organic transistors, low cost will be key to their widespread use. Various organic-transistor structures are shown in Fig. 2.

Pentacene is one of the most promising organic materials used for organic-transistor fabrication because it offers higher mobility, a better on/off ratio, improved stability under environmental conditions, and hence greater reliability[13] than other organics tested to date. Pentacene, however, is relatively insoluble, thus rendering the normally solution-based fabrication methods for organic transistors useless. Solution-based processing is the key to low-cost circuit fabrication: it enables high-volume printing, and it eliminates batch-oriented
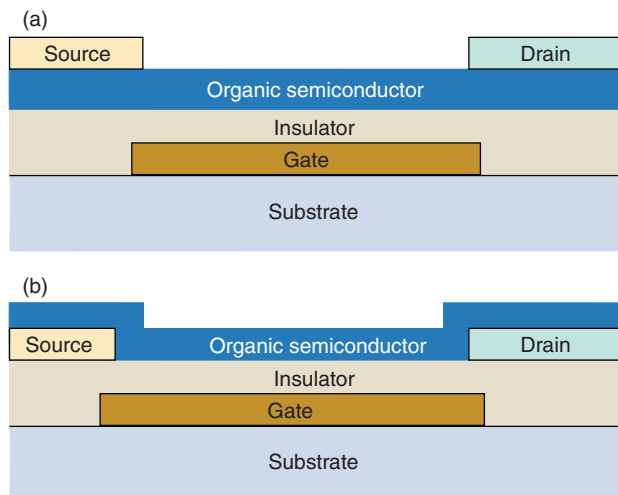

Figure 2. Schematic representation of organic TFT device configurations. (a) Top-contact device with source and drain evaporated onto the organic semiconducting layer. (b) Bottom-contact device with the organic semiconducting layer deposited (printed) onto the prepatterned source and drain electrodes.

lithography, subtractive etching, and vacuum-based film deposition. Recent work[14] with a pentacene precursor (which is soluble) has allowed the fabrication of organic transistors by inkjet printing using a substrate-gated-transistor structure with a pentacene-precursor overprint. After deposition, the pentacene precursor is converted to pentacene by annealing at 120°C or above. Optimization of the annealing process has created demonstration transistors with on/off ratios >10^5 and field-effect mobilities >0.1 cm^2/V•s. Many printed organic transistor mobilities have been in the 0.01 cm^2/V•s range, which is extremely low when compared with mobilities in, for instance, silicon, which range between 500 and 1300 cm^2/V•s. Thus, 0.1 cm^2/V•s is a significant improvement in the organic world. The latest results with pentacene have demonstrated mobilities of >1.0 cm^2/V•s.[13] Although the mobilities with organic TFTs are moving into the useful range, there is still a major problem with their operating voltage, which often exceeds 20 V because of poor capacitive coupling through the relatively thick gate-dielectric layers (inorganic oxides and nitrides or insulating polymers). Gate-dielectric layers are often >100 nm thick to minimize leakage currents.[15]

Recent breakthroughs in gate structures have helped this situation. Particularly interesting is a 2.5-nm-thick gate dielectric produced by molecular self-assembly.[15] Combining these self-assembled monolayer (SAMs) gate dielectrics with a high-mobility organic semiconductor (pentacene) has produced organic TFTs with gate voltages of 2 V or less and leakage currents that are lower than those of their organic counterparts. Such performance suggests that organic TFTs could be used in low-power applications such as portable devices.

In addition to the new gate structure for conventional ICs and the development of workable organic TFTs, other semiconductor materials are needed to address special application requirements. For example, GaAs has been used in high-frequency and high-power applications in place of silicon because of its direct band gap, higher electron mobility, and higher-temperature operation (>200°C). GaAs is semiinsulating, making heat removal more difficult. Thus, high-power GaAs chips are usually thinned to <100 μm thick to reduce thermal resistance and facilitate heat removal. For reference, a standard silicon chip is ≈500 μm thick. However, the thinned GaAs chips are extremely fragile, making handling and assembly operations difficult. The answer to high-temperature, high-power operation may lie in alternate semicondcutors such as silicon carbide and III-nitride-based compounds such as GaN.[16] Recent developments in both silicon carbide and GaN have been reported.[5] Significant progress has been made recently in the reduction of the defect densities in SiC by several orders of magnitude and in the growth of large single crystals. Both of these factors have led to the production of SiC small-scale ICs and individual transistors with reasonable yield at the prototype or preproduction level.

SiC and GaN devices have demonstrated operation in the 300–600°C temperature range. In fact, SiC devices have performed basic switching operations at temperatures exceeding 900°C. Such performance holds promise for solving instrument and control problems in high-temperature applications such as airplanes, spacecraft, automobiles, industrial and power plants, deep-Earth exploration and oil drilling, and, of course, high-power communications systems and radar. This robust high-temperature performance would also provide a measure of security for our electronic and electro-optical systems against the effects of nuclear or other weapons that generate high temperatures. In addition to improvements in the SiC and GaN devices themselves, high-temperature packaging will also be a major challenge to the widespread deployment of SiC or GaN.

Alternate Devices

Although changes to standard IC device structure or materials have been described above, they are basically building on standard metal semiconductor and MOS technology that has been established for more than half a century. Although the density and performance listed above have been outstanding and hold significant promise for even greater future accomplishments, the need for a new device structure will ultimately become paramount. Current MOS FETs, the mainstay electronic device for ICs, have gate lengths <100 nm, and 65-nm gate lengths are somewhat standard in high-performance products. As mentioned above, Intel is starting to produce 45-nm chips, and both 32-nm and 22-nm chip families are planned for the next 4–5 years.

By the middle of the next decade, many researchers believe that the MOS FET, even with Intel's advanced gate structure, will encounter critical technological barriers and even fundamental (i.e., quantum) limitations to any further reduction in size (achieved by scaling critical device parameters). However, decreases in size or scaling fuel the economic engine of the electronics industry, so there is a considerable push to find new devices (materials) that overcome some or most of the problems with the continued scaling of MOS FETs. CNTs are considered by many researchers to be the possible answer.

In a previous article,[5] the fundamental history, structure, operation, and methods of synthesis of CNTs were described. The method of preparation or synthesis and the tube dimensions determine whether a nanotube acts as a metal or a semiconductor. The fact that both metal-like behavior and semiconductor-like behavior can exist in single-walled CNTs gives rise to the potential for an all-carbon-based nanoelectronic technology in which the active devices are semiconducting single-wall CNT transistors and the electrical interconnects are metallic CNTs. Semiconducting, single-walled nanotubes are direct band-gap materials (nominally 1 eV) and can directly absorb and emit light, thus offering promise for a nano-optoelectronics technology based on CNTs. Both n-type and p-type CNT FETs can be produced, thus promising that today's complementary MOS technology can be reproduced at the nanoscale. One-dimensional Schottley-barrier-like devices can be formed at metal/single-walled CNT interfaces. If parameters are right, these devices are ambipolar, displaying N-type behavior (electron conduction) under positive bias and P-type behavior (hole conduction) under negative bias.

Under certain bias conditions, electrons and holes can be simultaneously injected from opposite ends of the CNT, offering great potential for optical light sources.[17] Single-walled CNTs have been resonated while suspended between two electrodes and show potential as ultra-small oscillators or frequency sources.[18]

APL has begun initial work in the area of active nanotube devices. The focus of the research has been lateral CNT field-emission devices (diodes and triodes).[19] Unlike their vertical counterparts, which are used in display technology, the lateral devices offer higher-frequency operation with low power consumption. In addition, device capacitances are very low, and operational current densities can be high (in the amperes/cm^2 range).

Other semiconductor-based technologies include integrated optics[20] and microelectromechanical systems (MEMS). MEMS technology has been around for more than 20 years and, as a somewhat mature technology, has made significant inroads into the commercial world (accelerometers, sensors, actuators, mirror arrays, etc.). The basics of MEMS, APL MEMS development, and the future of MEMS have been described previously in several articles.[21–23]

The field of integrated optics involves optical devices in which light is transmitted in planar waveguides. Planar waveguides are dielectrics that confine the propagating light within a very small structure with a dimension on the order of an optical wavelength. Integrated optical waveguides are typically combined with miniaturized sources (lasers) and detectors to form a functional optical system on a substrate (support layer). The resulting system is called an integrated optical circuit (IOC) in complete analogy with the semiconductor IC. Devices contained within an IOC include lasers, lenses, switches, interferometers, polarizers, modulators, detectors, etc. These IOCs have many uses, including spectrum analysis, analog-to-digital conversion, optical-signal generation, reception sensors, high-bandwidth optical links, and encryption. Optical ICs, in addition to their ultra-small size, have many advantages over conventional bench-top optical systems, including reduced sensitivity to all currents and vibration, low driving voltages, high efficiency, robustness, reproducibility, and economy in large volumes.

Optical ICs, just like their conventional high-frequency electronic counterparts, exist in two basic forms: hybrid and monolithic. Hybrid integrated optic systems consist of planar waveguide substrates containing guides, splitters, branches, gratings, etc., combined with separately fabricated sources, detectors, modulators, and other devices. The hybrid approach requires assembly and various nonstandard forms of interconnect, thus potentially raising cost and sacrificing reliability, because of the increased number of interconnections between dissimilar materials. Hybrids, however, have potential performance advantages because all of the components could be optimized, e.g., by using gallium aluminum arsenide for lasers and silicon for the detectors. Hybrids offer flexibility and cost advantages to institutions like APL that produce low volumes and prototypes.

Monolithic IOCs are basically built on one semiconductor material (e.g., GaAs) that is modified for different components by shaping structures using etching, incorporating dopants, and/or depositing or epitaxially growing additional layers or materials. The most promising materials for monolithic IOCs are the direct band-gap III–V semiconductors such as gallium aluminum arsenide (GaAl)As and indium gallium arsenide phosphide (InGa)(AsP) because, with proper processing, they can be formed into the needed structures (e.g., lasers, modulators, switches, detectors, etc.).

The most fundamental element of an IOC is the channel waveguide. Channel waveguides work like conventional fiber optics, which are used today in long-distance optical communications systems, by trapping light within the material. Channel waveguides are made by deposition and/or etching techniques and are typically made of polymers, silicates, or other light-transmitting materials. The basic requirements for this optical guide

material are that the material is transparent to the wavelength of interest and that the guide's index of refraction be higher than the surrounding material. A typical cross-section of a thin-film optical guide is given in Fig. 3. These waveguides are made by depositing and patterning material on top of a substrate or etching trenches in the substrate and filling them with polymers, silicates, and/or other light-transmitting materials. Guides can be fabricated into several important optical structures, including branches, couplers, interferometers, and guides with integral gratings.

A novel method of guide fabrication has been implemented at APL by using polymers that are electro-optically sensitive. By inducing polarization through the application of an electric field (poling process), the index of refraction of electro-optically active polymers is changed to form channel waveguides. In the APL process,[22,24–26] polyimide is doped with a nonlinear optical chromosphere such as DCM (4-dicyanomethylene-2-methyl-6-p-dimethylaminostyrl-4H-pyran). Poling is accomplished by insertion in a strong electric field as the polymer is heated near its glass-transition temperature. There are several approaches to the fabrication of optical waveguides that use combinations of doped and undoped polymide as well as doped polymide that is either unpoled or poled. Two examples are shown in Fig. 4.
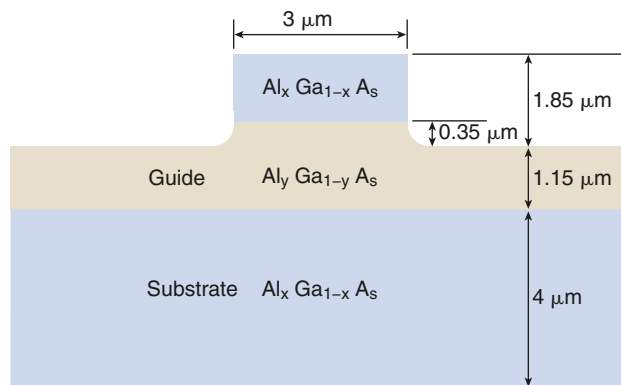

Figure 3. Typical schematic cross-section of a deposited and etched channel waveguide. X is typically 0.24, whereas Y is 0.18. The guide's index of refraction must be higher than that of the medium in which it is embedded.
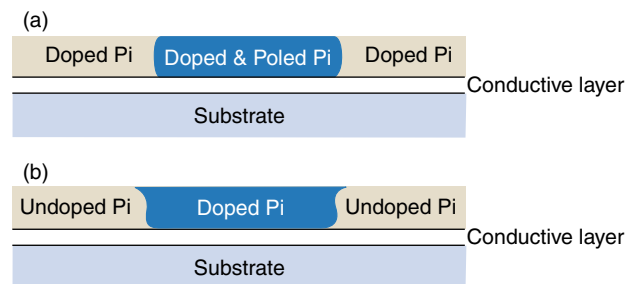

Figure 4. Cross-sections of an optical waveguide formed by using combinations of doped polyimide (unpoled and poled) (a) and undoped and doped polyimide (b).

The first example is shown in Fig. 4a, where doped polyimide is deposited on a substrate that is conductive (metallized) or has a back electrode. Top metal is then deposited and photolithographically patterned to define the guide region. An electric field (up to 1 MV/cm) is applied to the top and bottom metal while the sample is heating to order the chromophores and change the index. Index changes from unpoled to poled polyimide can be >5%, depending on the chromophore doping level and the poling field (the poled polyimide displays the lower index). Once poling is complete, the top metal is removed.

In the second example (Fig. 4b), a layer of undoped polyimide is deposited, patterned (with a channel), and cured on a substrate (metallized or not). Doped polyimide is then deposited and cured in the channel to form the guide. Index changes in the transition from undoped to doped polyimide can be >19%, depending on the chromophore doping level; the greatest change (decrease) occurs at the highest doping level.

In addition to optical guide formation, the use of chromophore-doped polyimide has been investigated for its use a standard circuit dielectric that can support diagnostic testing by using electro-optical probing.[22]

Globalization

Globalization is almost a passé term in the electronics and electro-optics industries. Many aspects of the business have been "globalized" for years, especially in those task areas in which labor-intensive operations are performed (e.g., packaging and testing; see the next section). Asia has dominated the packaging field for at least 25 years, and today it provides ≈80% of the packaged electronic and electro-optical devices or parts sold worldwide. The semiconductor device business has historically been focused in the United States, and even when the major U.S. chip manufacturers lost out to the foundries in Asia (Japan and Taiwan) for the commodity chip products (e.g., memories), the United States still retained design and development of high-end application-specific ICs and microprocessors. Intel and, to a limited extent, Motorola and Advanced Micro Devices (AMD) dominate the microprocessor world. With foundries around the world [Israel, Ireland, China (2009 launch), and the United States], Intel is the leader in advanced microprocessor technology and, until recently, has performed all the advanced design work in the United States. The

center of design work has changed. The Intel Bangalore (India) design center was responsible for the 45-nm HfO_2 gate insulator technology, and it will be the focal point for the more advanced technologies slated for 2009–2011. Thus, the most advanced chip design is no longer being done in the United States.

Advanced device development such as that associated with silicon carbide and CNTs is also a global activity. The latest SiC material breakthroughs have come out of Japan. The CNT was discovered by a Japanese researcher and is being exploited worldwide, as shown in the distribution of nanotube publications (Fig. 5). The United States appears to have a slight lead in the nanotube publications race. Funding for nanotube research is shown in Fig. 6. As shown, the United States, Europe, and Asia are investing significant resources in the development of CNTs.

Optical source and waveguide research and manufacture are also global in nature. Many of the latest advances are coming from Asia, including the latest light-emitting diodes and solid-state lasers. The worldwide electro-optics/photonics market is about $270 billion in today's U.S. dollars and is expected to at least double in the next 10 years.

The globalization of the electronics industry (and I suspect other industries as well) has taken place in a stepwise process over several decades. The globalization process begins this way. First, the manufacturing of volume products is outsourced to regions with an indigenous supply of trainable, low-cost labor. Next, because of the remoteness of the plant locations, the manufacturing operations are required to do basic engineering to improve product yield and reliability. As engineering skills improve,
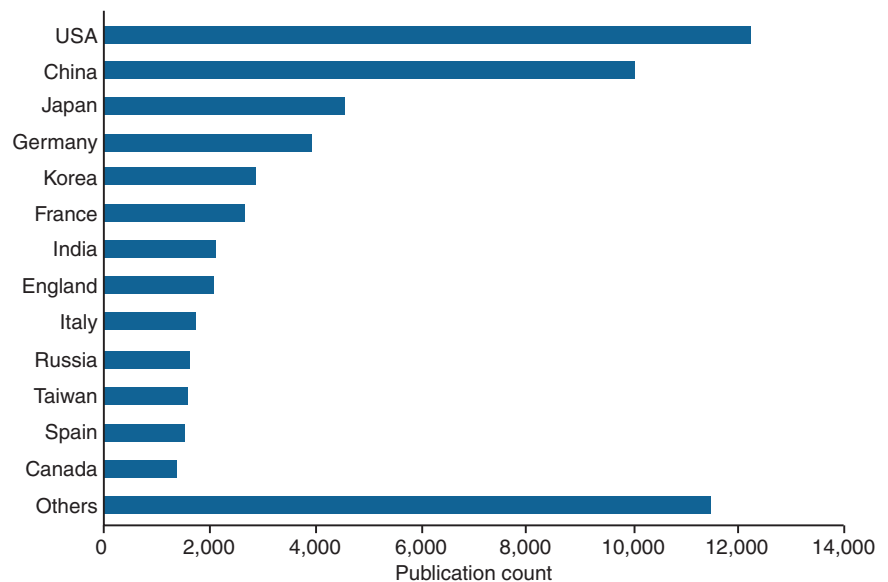

Figure 5. Nanotechnology publications count by country (based on data from the Science Citation Index of 5300 journals for 2007). The "Others" category includes 32 nations with more than 100 and less than 1000 nanotechnology publications.
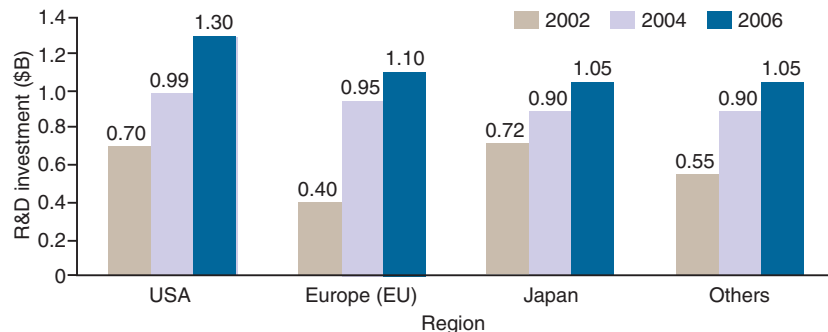
Figure 6. Estimated government nanotechnology research and development investments, expressed in billions of U.S. dollars.

design changes are suggested. These changes result from first-hand knowledge of the process and the testing results. Finally, design skills advance, and eventually the outsourced operation is capable of full design, manufacturing, and testing, and product innovation follows. Research becomes a part of the process to ensure future viability. See, for example, *The World is Flat: A Brief History of the Twenty-First Century* by Thomas L. Friedman.[27]

ELECTRONIC AND ELECTRO-OPTICAL PACKAGING

As the chip (IC) technology and performance grow without bounds (Moore's Law still holds) and new devices such as printable organic transistors and CNTs come on the scene, the world of electronic packaging is facing significant challenges to keep pace. In today's world, the emphasis is on portable systems and the associated factors of small size, low weight, low cost, low power, high functionality, ease of use, and wireless connectivity. These portable, low-cost, highly functional, and reliable systems (portable computers, cellular telephones, digital assistants, music players, etc.) have driven major changes in electronic packaging. These changes encompass all aspects from the size and type of interconnection to major shifts in board materials and package structures.

As the future evolves, increased I/O numbers and density, as well as increased frequency (or clock speed) of operation and larger heat-dissipation requirements, will add further to the already complex packaging world. New devices such as organic and CNT transistors, electro-optical sources, sinks and guides, and microelectromechanical structures will continue to force additional packaging changes.

Even with today's advanced packaging,[5] including stacked components, the packaging efficiency of today's electronic products is extremely low, ranging from ≈10% to 15%. The packaging efficiency is defined as the area of the IC chips to the area of the underlying printed wiring board (PWB). Because the surfaces of PWBs are cluttered with a range of passive components (e.g., resistors capacitors and inductors) and other devices rather than ICs, the packaging efficiencies are inherently low. The full integration of all components except the ICs has the potential to raise the packaging efficiency to greater than 80%. Schematically shown in Fig. 7, this integrated substrate concept requires packaging technology to advance to the point where disparate devices, components, and structures can be embedded in the substrate or board and thus not take up additional board surface layers. The surface area can then be reserved for large, closely packed ICs that are either in a single level or a stacked
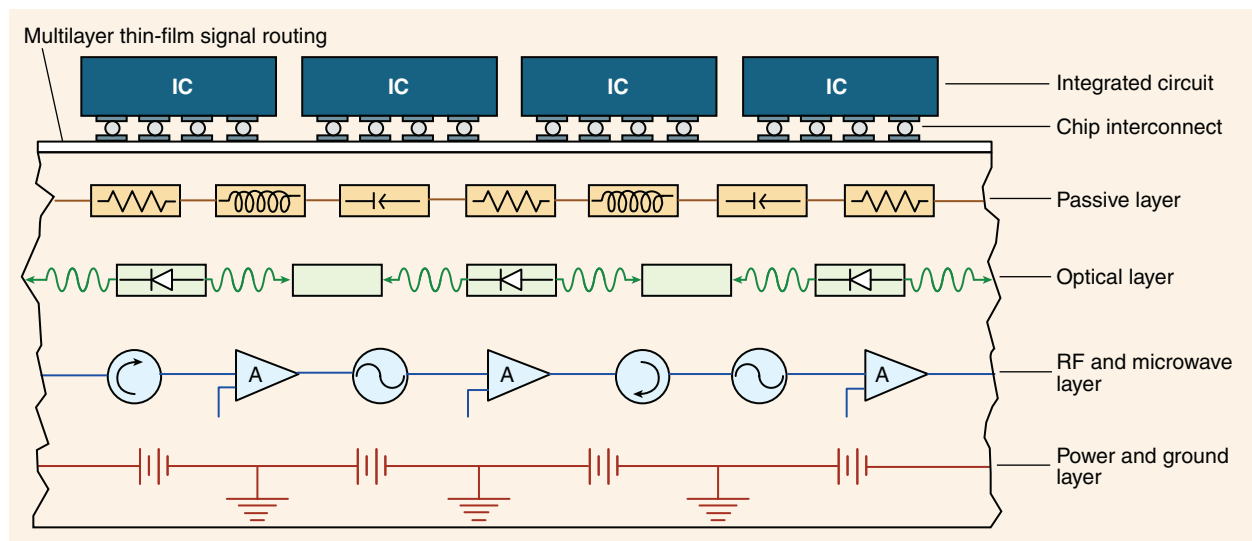

Figure 7. Schematic representation of next-generation integrated substrate technology with embedded RF, microwave, optical, and passive component layers coupled with integral power and ground.

package and are connected by either flip-chip bonding or some other high-density interconnection method.

Interconnection

Flip-chip technology continues to be the rising star in the interconnection world, and, although it is not new, it continues to grow rapidly in the electronic packaging world. A world that was totally dominated by wire bonding just a few years ago is now seeing significant use of flip-chip assembly for high-density, high-performance packaging. Still, despite the inroads made by flip-chip technology, >10[12] wire bonds are made annually.[28] Wire-bonding and flip-chip technologies are shown in Fig. 8. Conventional flip-chip technology is more costly than wire bonding, even in high volume, because of several factors, including the increased IC processing necessary to put the solder balls on the bonding pads, the need for special reflow equipment, and the formation of matching high-resolution (same I/O pitch as the chip) bonding pads on the underlying circuit board. Because of the increased cost, flip-chip technology is used only in applications that require high density and increased speed (frequency) of operation. Wire bonds have frequency-response limitations (loss), which limit their effectiveness to frequencies <10 GHz. The short, wide pillar of the flip-chip solder joint exhibits low signal loss at frequencies >100 GHz. Although high-performance digital circuits are not operating at such clock frequencies (>10 GHz) today, the current rise times of high-performance IC clock signals are 100 ps or less, thus necessitating low-loss signal paths with interconnection bandwidths approaching 35 GHz.

The attachment of bare ICs directly to a circuit board by using wire bonding or flip-chip assembly without an intervening package is on the rise. Such direct-chip attachment (DCA) is faced with several challenges as PWBs evolve from the standard glass-fiber-reinforced

PWBs (rigid boards) to thin, non-rigid board structures (flex boards or flex tapes). Wire bonding on non-rigid structures has been studied extensively at APL,[29] and the studies indicate that by changing bonding parameters [force, temperature, ultrasonic energy, and energy application time (dwell)] and increasing the ultrasonic frequency, strong bonds can be effected.

Flip-chip interconnects are also being used on flexible circuit boards. Although the flip-chip-to-flex-attachment process (solder reflow) is relatively straightforward, some concerns about reliability still remain because of the coefficient of thermal expansion (CTE) mismatch between the rigid semiconductor chip (low CTE) and the unconstrained (no glass-fiber reinforcement) flexible circuit board (high CTE). Large CTE mismatches between chip and circuit board can produce large strains on the solder, leading to fatigue failures. This problem is exacerbated when the chip is large (i.e., when the outermost solder joints are a long distance from the neutral point) and the diameter of the solder ball interconnect is made small to achieve high density (large I/O numbers). One solution to the CTE reliability concerns is the use of underfill, which is an epoxy infused between the chip and the circuit board to fill the space and "glue" the entire surface of the chip to the surface of the underlying board while fully encapsulating the solder joints. The underfill distributes the CTE mismatch forces over the entire surface area of the chip and underlying board, thus minimizing the forces on the individual solder joints and improving reliability. The use of underfill on flip-chip-standard PWB assemblies (rigid boards) has been shown to significantly improve reliability. Underfill for flip-chip-on-flex has been used in volume production with somewhat mixed results. Careful selection of underfill properties for application to flexible circuits is necessary. The standard rigid epoxy underfills prevalent in today's microcircuit industry need to be replaced with low-modulus materials.

APL has taken a different approach to the flexibility issue. Because most of the semiconductor material in an IC chip is needed only for handling during the processing, the use of thinned-die-on-flex (or on multilayer organic thin-film substrates) holds significant promise for solving reliability issues without underfilling.[30] Dies as thin as 25 μm have been attached to 25- to 50-μm-thick flex boards by flip-chip technology. These overall flexible assemblies are <100 μm in total thickness and can be flexed and laminated to curved surfaces with radii as small as 1.5 cm. Examples of such flexing and laminating are
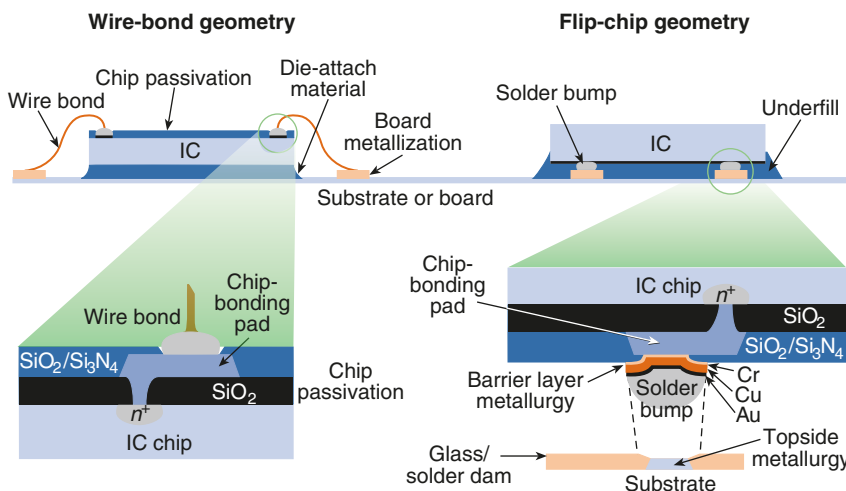

Figure 8. Schematic representation of wire-bond (left) and flip-chip (right) geometry.

shown in Fig. 9. Special handling methods for these thin chips have to be used to avoid damage during assembly.[31,32]

These thinned assemblies have proven extremely reliable, surviving many thousands of stringent thermal cycles (−55°C to +125°C) both with and without underfill. Because the ultimate failure of these parts is solder-joint fatigue, the use of a properly selected underfill (extremely low modules to complement the inherent flexibility) has been shown to extend the fatigue life under these stringent conditions.[29] Figure 10 illustrates Weibull plots (i.e., cumulative failure versus number of thermal cycles) for these thin-film-on-flex assemblies. The ultimate system for flexibility and dense packaging applications will be thinned die on multilayer flex-based-on-thin-film technology. An example of thin-film flex produced at APL is shown in Fig. 11. By using thin-film flex and thinned die, assemblies (chip, interconnect, and substrate) as thin as 30 μm could be produced.[33] This thickness is a little over one-third the thickness of a typical human hair.

Driven by cost and process complexity, APL and others have explored alternatives to conventional flip-chip technology. At APL we have used single-ended ball bonds, produced by automated wire-bonding machines using special gold alloy wire to replace the solder bumps. These special gold ball bonds are placed on standard chip-bonding pads (no need for under-bump metallurgy; see Fig. 8 and Ref. 34), and through machine action, the wire is broken behind the ball. After wire separation, the balls are coined or tamped to achieve a uniform

Figure 10. Weibull reliability data for assemblies with 30-μm-thick die and no underfill. (Left) Failures of die (either chain failed). (Right) Failures of chains.

height above the chip surface. Once formed, these gold "stud bumps" are then glued to mating bond pads on the circuit board by using standard electrically conducting epoxy or an anisotropically conductive adhesive.[35] The details of these stud-bump and glue techniques have been described previously.[5]

Numerous other advanced electrical interconnects have appeared over the years, ranging from laser pantography[36] to solder columns and mechanical spring-like fingers. Such interconnects have also been discussed previously.[5,22]

Electro-optical and optical chip interconnection involves both conventional direct-wired interconnects and, of course, the coupling of light beams to fiber optics or integrated light guides. The direct wiring piece is usually accomplished via wire bonding or flip-chip assembly as described above. The coupling of optical signals into
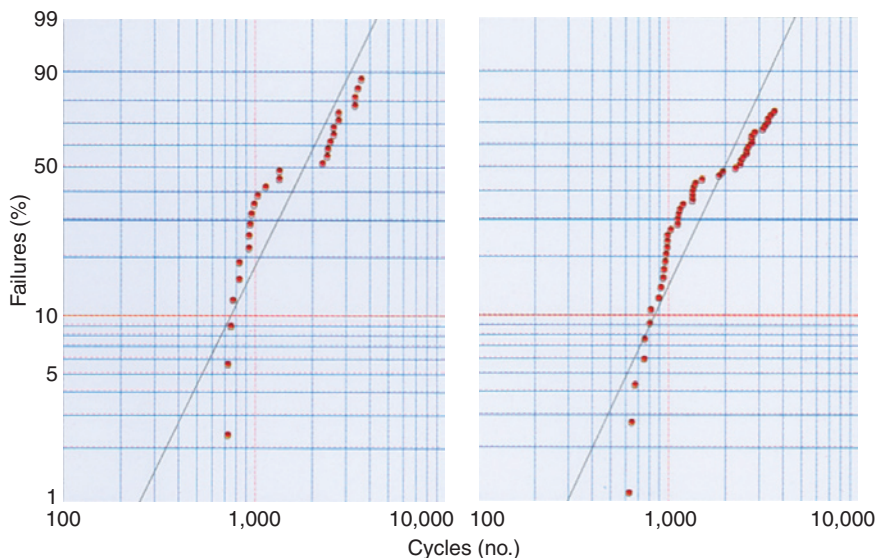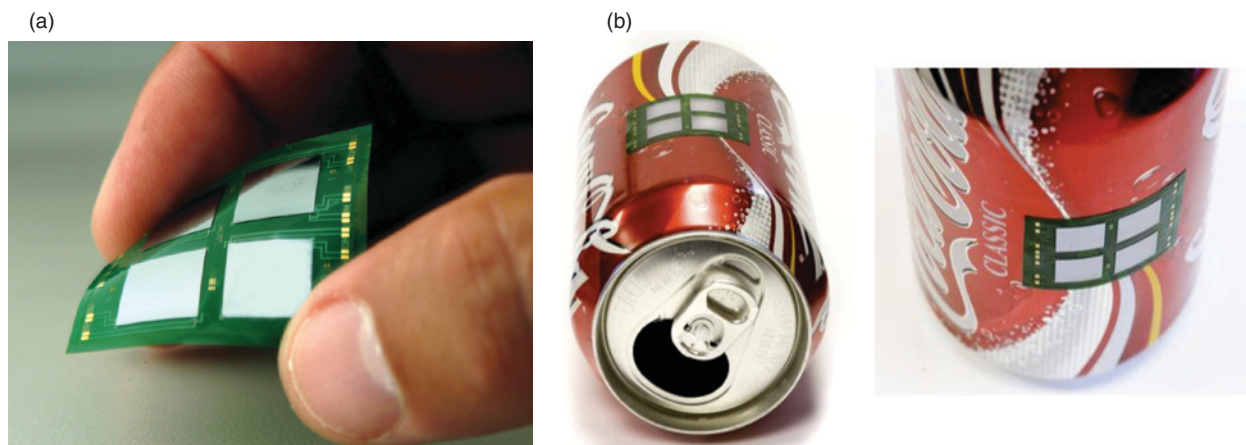

Figure 9. Ultra-thin silicon on flexible circuit-board assembly. (a) Circuit flexed in between fingers. (b) Circuit laminated onto a curved surface with a radius of 3.3 cm.
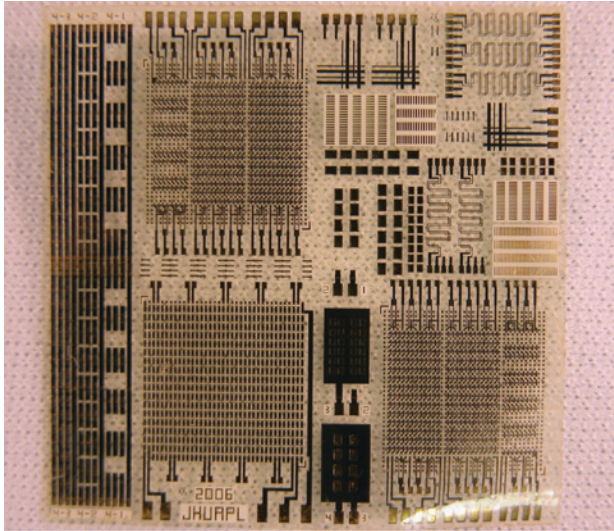
Figure 11. Multilayer, thin-film, flexible substrate that is <25 µm thick. Substrate size is 2.5 cm × 2.5 cm.

fiber optics or planar optical guides is typically accomplished through a free-space path or through a medium that matches the index of refraction of the emitter with that of the guide (either fiber or planar). Solid-state emitters are either edge emitters (conventional semiconductor lasers) or surface emitters (vertical-cavity surface-emitting lasers, or VCSELs). A typical mounting and interconnection of a VCSEL source and a detector by using an integrated light guide are shown in Fig. 12. In this case, the VCSEL and the detector are flip-chip-mounted on one side of the substrate upon which the integrated light guides are fabricated. The flip-chip solder bumps provide the electrical control and power to the semiconductor laser, power the detector chip, and provide the electrical readout of the received laser signals. Typical edge-emitting lasers are coupled directly to an optical fiber. In this arrangement, there is a transition (lens) that matches the change in refractive index Δn from the emitter to the fiber. These transitions typically go from high Δn (associated with on-chip or on-board planar light guides) to low Δn associated with fiber optics. For example, planar light guides, as described above, typically have a high Δn percentage difference (4–5%) between the core and the cladding, whereas in fiber-optic transmission lines, the Δn percentage difference between the core and the

cladding is on the order of 0.5–2.0%. APL, in addition to working with standard transitions and optical couplers, has developed a novel transition technique[26] based on combinations of undoped, doped, and doped and poled electro-optic polymers.[24] The important basis of our technique is that the index of the electro-optic polymer can be changed by doping and changed still further by poling the doped region. With such ability to change a given polymer's index, there is no need to form complex transition structures by depositing ordinary materials of different dielectric constant and thickness. Given the reversibility of poling with field removal in selected chromophores and polymers, and the increase in index as a function of field strength, it may be possible to have an electrically controllable index change that has applications in switching, beam deflection, and modulation and demodulation of light beams.

Packaging Structures

Individual or single-chip "packaging" technology has evolved into two major branches: (*i*) area-array packages, such as ball grid arrays (BGAs), which are rapidly replacing historic high-density, perimeter-leaded, surface-mount packages such as quad-flat packages (QFPs), and (*ii*) chips mounted directly to PWBs (or substrates) without an intervening packaging structure. This direct-chip mounting is called DCA (see above) or chip on board.[5]

BGA technology offers significant advantages over QFPs and the older dual-in-line packages (DIPs) that still dominate in most box electronics. Even today, DIPs account for >50% of the single-chip packages. The advantages of BGA include constant I/O density (regardless of the total number of I/Os). Because the I/Os are spaced on a grid, the I/O density remains constant as the package size (or I/O number) increases, thus facilitating board design. The area array can also make effective use of path-length-matching techniques that minimize differences in length between the shortest and longest I/O paths, as well as provide enhanced impedance control due to the available ground/signal/ground package structure. The importance of the BGA is evidenced by its rapid growth, and it is currently challenging the DIP for leadership as the dominant packaging style. The BGA has spawned a series of compact high-density versions with reduced grid spacings and smaller solder bumps. These
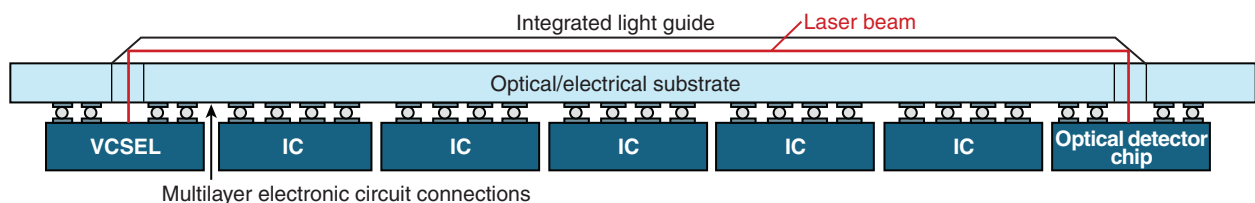

Figure 12. Schematic representation of a combined electrical- and optical-packaging configuration using integrated light guides and VCSELs.

micro packages are also giving rise to reliability issues. In a full-size BGA (Fig. 13a), the package substrate is typically glass-fiber-reinforced PWB material with most, if not all, of the solder joints outboard of the chip area. In this version of the package, the CTE matched that of the underlying PWB, thus producing little stress on the solder joints and providing good interconnection reliability. When the BGA was shrunk to the micro version (Fig. 13b), the package substrate was switched to a thin flexible tape, and the reduced-size solder joints covered the area under the chip. The chip then controlled the CTE of the package ("chip-dominated package"), and thus large CTE mismatches occurred between the package and the underlying PWB, causing reliability issues. These issues have been addressed by several techniques that effectively decouple the IC from the package structure, thus reducing the forces experienced by the solder joints. The simplest decoupling scheme is use of a compliant (low-modulus) die-attach adhesive. Other remedies for improving chip-dominated-package reliability include use of underfill or a floating die structure.

The use of standard multichip packages has declined significantly from the "hybrid era" of the 1970s and 1980s. The decline is due to several factors, including increasingly large and more complex chips; digital replacement of analog circuits; and the growth of packageless configurations, DCA and chip on board, and the inherent yield issues[37] associated with large numbers of chips in a single package. Today, multichip packages or modules exist for high-end applications, such as multicore processors and other complex system functions. These multichip modules (MCMs) involve densely packed bare chips on a multiconductor layer substrate housed within a large QFP or BGA-type structure, which is then subsequently a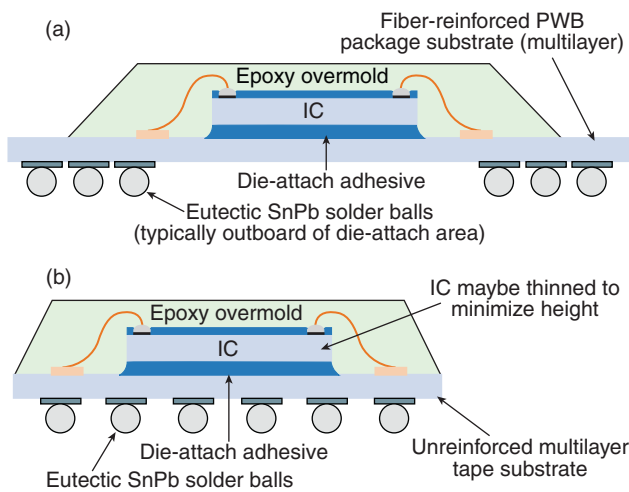ttached to a PWB like a standard single-chip package. Typically, because of the high power density of these devices, special heat-sinking or other cooling arrangements may be necessary.

MCMs are characterized by the substrate technology (the inter-chip interconnection structure within the module) used. The following three types of substrate technologies have evolved:

1. MCM-C: Screen-printed conductors on screen-printed ceramic dielectric layers or green-state ceramic sheets
2. MCM-D: Deposited and photolithographically patterned metal and insulating thin-film layers on a silicon or highly polished ceramic carrier
3. MCM-L: Copper conductors laminated to organic dielectric layers similar to a PWB but with finer traces and a different method for producing the interlayer conductive connections (vias)

In MCMs, the active devices (ICs) cover >50% of the substrate area, in contrast to the board-level packaging densities of ≈10% mentioned above. Continued work on the integration of passive components (R, C, and L) into the substrate is further increasing packaging density and extending the MCM technology to a broader range of applications. Both integrated or embedded passives (R and C) are well proven in MCM-C technology and have achieved limited production in MCM-D modules. Organic resistive and capacitor layers have been used in PWBs and MCM-Ls. Organic-based inductive layers are under development. The advantages and disadvantages of the various MCM types have been discussed previously.[38]

A rising star in the multichip packaging world is the chip stack or the 3-D stacking of chips (shown in Fig. 14). The 3-D stacking of chips is designed to reduce the board area or footprint required by non-stacked chips at the expense of vertical height. Today's electronics are relatively planar in nature, and area space is at a premium. In contrast, the third dimension, although usually limited, still has available space. Because of the

Figure 13. BGA package cross-sections. (a) Standard BGA (large solder balls outboard of die). (b) Miniature BGA (small solder balls covering entire package bottom, including the area under the die).
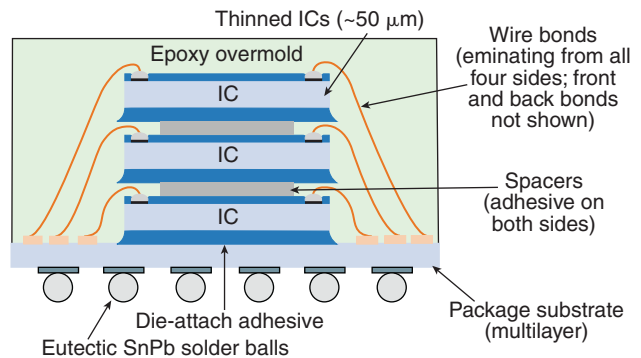

Figure 14. Schematic representation of a modern stacked chip. As many as eight chips have been stacked (four to six is most common). For other stacking arrangements, see Ref. 5.

stacked nature of the multiple devices and the difficulty of connecting each device separately to pads at the board level, 3-D stacking has been mainly confined to parallel architectures with relatively low I/O (e.g., memory). Currently, as many as six to eight die have been stacked. Dies in stacks are typically thinned (nominally 50–100 μm) to reduce the overall stack height. If a chip in a stacked die package fails, the entire package is usually discarded. Package yield as a function of stack height and individual chip reliability has been studied at APL.[39] Also, in complete analogy to stacked chips, entire circuit boards could be stacked by using prepatterned compliant interposers.

Wafer-Scale Packaging

A major focus of the semiconductor industry in the last decade has been the creation of ever-smaller, high-performance packages for ICs and other electronic components. The primary drivers for packaged parts of reduced size (and weight) are consumer products such as camcorders, digital cameras, cell phones, and other wireless devices. The solution to the performance and size issues has been the introduction of the chip-scale package (CSP) mentioned above. Currently, wafer-scale packages, or more properly, wafer-level packages (WLPs), are a rapidly increasing element of the CSP market. Growth of WLPs as part of the miniature packaging market is shown in Fig. 15. In WLPs, the package-like interconnection structure is built onto the IC while still in wafer form with IC-like processes. These WLPs include both the environmental protection and the redistribution layer(s) for the I/Os (from peripheral contact pads on the chip to area-array solder bumps on the "package"). WLPs offer significant promise for even greater market penetration and much lower cost. Other WLP benefits include enhanced performance, reduced packaging and testing time, improved process control, and shortened time to market for new products. WLPs could

Figure 15. Growth of WLPs. Inset shows distribution of current WLP products.

ultimately eliminate the need for conventional packaging operations, provided that chip device yield is high. In WLPs, the "packaged" parts would be tested and burned in (thermally screened) on the wafer before separation, in contrast to today's packaging operations, in which functional ICs are assembled only after they have passed wafer-level testing and have been separated. Thermal screening, if required, is performed only on electrically good packaged parts. A schematic representation of a WLP has been shown previously (Fig. 11, Ref. 5).

Today, WLPs are in production for low-I/O-count (<100) products, in which large pitches and solder balls can be used to mitigate the reliability concerns generated by large CTE mismatches between the chip and the underlying circuit board. Large solder balls (>200 μm) and pad pitches (spacing) reduce the need for underfilling. I/O requirements on IC chips continue to grow rapidly, and researchers predict 104 I/Os on a single chip within the next few years. Thus, WLP solutions must be able to address these high I/O numbers to sustain projected future growth. The approach, to date, has been to develop very flexible short-lead structures (to solve the CTE mismatch problem) at reduced scale. Because the features of these interconnect structures have dimensions smaller than 100 nm, the industry is beginning to call this advanced, miniaturized, on-wafer packaging technology "nano-WLP."

Globalization

The globalization of the electronic and electro-optical packaging industry has taken place over the last 50 years, ever since the U.S. consumer electronics manufacturers sought low-cost assembly labor beginning in the late 1950s. Today, packaging is worldwide, and >90% of the assembly is done offshore. The major location for packaging is greater Asia (with both Taiwan and mainland China accounting for a significant fraction). Other pockets of worldwide packaging growth are accounted for by Europe (both Western and Eastern), Brazil, and Mexico.

With <10% of the world's packaging activity done within the United States, the relevant question for U.S. researchers becomes one of access rather than who is leading the research and development (R&D) in the field. Packaging R&D is being led by government-sponsored industrial institutes in the Far East and Europe. Typically, these institutions receive 50–60% of their funding from the government and 40–50% from industry. This close industry coupling ensures that their research is relevant (to the country's economic growth and technological-base development). Notable examples include KAIST (Korea Advanced Institute of Science and Technology) in Korea, the Institute of Microelectronics in Singapore, and the Fraunhofer Institute in Germany. Many foreign universities are also focused on packaging R&D (more than 20). These universities also work closely with
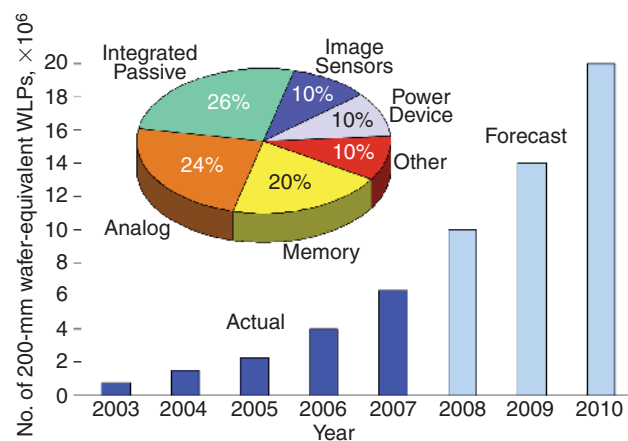
industry to find solutions for practical application problems in addition to pure R&D.

Today in the United States, a packaging research institute does not exist. Similarly, there are at best three universities with a focused packaging R&D program: Georgia Institute of Technology,[40] University of Arkansas, and University of Maryland. Other programs exist at the State University of New York at Binghamton, Auburn University, and the University of Arizona.

APL IMPACT

Electronic and electro-optical packaging is an important enabler for the implementation of all APL-developed electronic and optoelectronic systems. Whether the packaging involves the simple soldering of a commercially packaged part onto a PWB or the advanced application of a thinned, custom optical die onto multilayer thin-film flex, the packaging method is highly important to both the reliability and cost of the system. APL has had a long history of successful electronic packaging,[41] ranging from the VT fuze to advanced spacecraft such as New Horizons. In fact, the Laboratory is a pioneer in advanced packaging, ranging from single-chip interconnect and microcircuits to the packaging of entire systems for space, ocean, and biomedical use.

The future, however, holds many challenges for APL in the development of electronic and optoelectronic systems and their packaging. These challenges can be broken down into two major areas: technology advances and globalization (access to technology).

Technology Advances

Many of the technological advances in the area of electronic and electro-optical devices and packaging have been described above. These advances have a definite impact not only on system architecture, design, performance, and application but also on APL's ability to field working system prototypes and one-of-a-kind deliverables, such as Earth satellites or interplanetary probes. For the near future, ICs will continue to increase in performance and density with little outward change in appearance (despite major physical changes in gate structure and materials) or in their form of interconnection to the rest of the system. Design parameters and tools for these evolutionary changes will keep pace. As we move further out in time, major device changes will occur, including widespread use of organic transistors (pentacene types described above) and the CNT. Once they become mainstream, these devices will have major implications for electronic and electro-optical system architecture and functionality. Imagine a single active device that can act as a transistor or an optical light source simply by changing voltage bias conditions.

Although outward manifestations of IC technology are slowly evolving, one factor is rapidly increasing: the number of I/O connections required to support these chips. This increased number of connections is forcing major shifts in packaging style. Perimeter-type packages are giving way to area arrays. Area-array packages with direct solder attachment are becoming the mainstay for high-I/O configurations. In an attempt to keep the package size as small as practical, the size of the solder joints and the spacing between them are rapidly decreasing, giving rise to reliability issues (joint fatigue) and the need to mitigate these issues by using underfill and alternate structures, such as thinned die on multilayer flexible substrates. Such structures not only improve reliability but also provide great possibilities (because of their inherent flexible nature) for putting electronics into a wide variety of new applications, including clothing, conformal skin-like layers, appliqués, small-size products of all types, and areas requiring extreme flexibility. While these thin, flexible structures will have importance for APL and its customers, much of the commercial interest will be driven by the impact of these structures on the next consumer product. Wafer-level packaging for more standard electronic products will be a dominant packaging growth area in the consumer-product world.

Globalization

Globalization is a reality in the electronics business. Even the IC design process, which has been focused in the United States for many years, has finally become globalized. (See the discussion of Intel's 45-nm technology above.) Every other aspect of IC manufacturing and packaging has been globalized for many years, and the Far East is the dominant location (≈65% of the world's electronic products are produced in greater Asia). Taiwan and South Korea are major players, especially in electronic and electro-optical devices and packaging. Packaging R&D is especially strong in the Far East along with packaging education.

Thus, the challenge for APL and its sponsors is not globalization (which has already occurred) but how to gain access to both the globalized products and the information on their technical performance. APL often exploits ICs and other electronics in ways not envisioned or intended by the commercial parts developers, so we often require design and performance data in much greater detail than the data typically supplied by the manufacturer to commercial customers. These data are, at best, difficult to get from domestic manufacturers but almost impossible to get from abroad. Access to IC and electro-optical products is also a challenge because of APL's typically small volume requirements. We command little leverage with suppliers, especially those overseas.

So how does APL survive in this globalized electronics and electro-optics world? First, we have to maintain our ability to exploit current and future chip technology. To do this, we must invest in engineers and facilities to design, measure, test, and prototype hardware with the

latest device advances. We must also maintain a cadre of IC designers who can understand modern IC devices and their structures. Applications need to be developed so these IC designers can produce custom chips and thus use the latest foundries and design rules. Similarly, we must maintain and enhance our packaging capabilities, ranging from substrate fabrication to board-level interconnection. Having such capabilities fosters the ability to rapidly respond to new applications and provides a resource that could be used to team with others on end-use solutions.

Teaming is crucial in this world of globalized technology. This teaming must be international in scope. Thus, we must find ways to bring electronics and optics experts from abroad to APL. In addition, we must send our staff to work in institutions abroad, and, above all, we must find mechanisms to fund R&D abroad. These activities won't be easy, but they are necessary to maintain our knowledge base and technological access.

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