Miniaturized Electronics

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Semiconductor device and circuit technology, coupled with its associated electronic packaging, forms the backbone of high-performance miniaturized electronic systems. This article examines some of the current and future electronic device technology that is, or will be, important to APL. It also looks at the latest trends in packaging and how packaging is key to the development of high-performance systems. This integration of advanced devices with high-density packaging has been a cornerstone of APL activities, ranging from the VT fuze to the latest satellite. A glimpse into the potential of increased silicon integration, wide bandgap semiconductors, and carbon nanotubes for greater device performance is presented. The packaging discussion focuses on advanced interconnect and the use of flexible substrates.

INTRODUCTION

Miniaturized electronics (or microelectronics, as it is sometimes called) is a key enabler for APL's systems business ranging from at-sea testing to the development of interplanetary spacecraft. A previous *Technical Digest* article[1] on electronic technology gave many examples of the current and past use of miniaturized electronics at the Laboratory. The questions now are: Where is miniaturized electronic technology headed, and how will APL embrace this rapidly changing area of technology? To lay the groundwork to answer these questions, one must examine the future trends and technological advances in integrated circuits (ICs), electronic packaging, and systems integration.

INTEGRATED CIRCUITS

Silicon-based IC technology has continued to evolve dynamically from its beginnings in 1958.[2] The predictions of Moore's Law[3,4] for device density still hold, with the number of components (active devices or transistors) on a single chip doubling every 1.5 to 2 years, depending on device technology. A graphical embodiment of Moore's Law is given in Fig. 1. For example, an Intel Pentium 4 chip microprocessor (introduced November 2000) contained approximately 55 million transistors (plus other integrated components) on a piece of silicon not much larger than an average-sized fingernail (≈80 mm^2). Later versions of the Pentium 4 have contained more than 10^8 individual transistors, with the latest Intel Itanium series approaching 5×10^8 devices. In contrast, the first IC contained only one transistor and a few passive components and was about one-fifth the size (10.6×1.5 mm). Today, commercial ICs exist with more than 10^8 active devices on chips less than 100 mm^2 in area. Prototype devices with

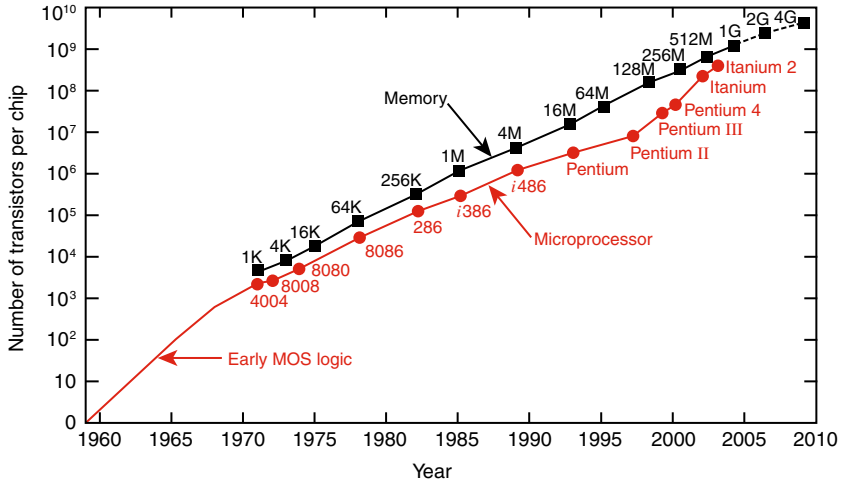

Figure 1. Moore's Law reflecting the exponential growth in transistor density on a single chip. (i386, i486, Pentium, Pentium I, Pentium II, Pentium III, Pentium 4, Itanium, and Itanium 2 are all Intel Corp. trademarks.)

10^9 transistors have been demonstrated; by early in the next decade, this number of devices or transistors should reach 10^{11} on similarly sized chips.

As IC technology evolves, other changes besides an increase in device density will happen. In high-performance devices, the standard aluminum-silicon alloy chip metallization, which is becoming more resistive as the on-chip interconnection dimensions shrink, is already being replaced by copper, with its much higher electrical conductivity.[5] Similarly, the on-chip inorganic dielectric layers between the multilayer metallization are being replaced by organic materials with lower dielectric constants such as polyimide, benzocyclobutene, or Teflon-based materials. In the future, if interconnection topologies can be defined, air may be used as the dielectric. The combination of low resistivity (and resistance) from the copper and air's very low dielectric constant will allow ICs to operate at extremely high speeds. With today's high-density chips, the typical charge within devices and moving between devices is on the order of 1000 electrons. As the number of devices on a chip increases to the 10^{10} range, with a resultant device size of less than 10^{-8} mm^2, the number of electrons per device drops into the single digit regime. Because of leakage and bulk charges, the storage and movement of such a small quantity of charge cannot be performed reliably by current device technology (bipolar junction transistors or field effect transistors) and will require the development of new device structures and other semiconductor methods of electronic transport control.[6]

Wide Bandgap Semiconductors

In addition to new device structures, other semiconductor materials will be needed to address special application requirements. For example, GaAs has been used in high-frequency and high-power applications. It is the mainstay active device for microwave power devices due to its high electron mobility and the ability to operate at high temperatures (above 150°–200°C) due to its semi-insulating behavior. However, such behavior also makes it difficult to remove heat from high-power devices, thus necessitating the thinning of GaAs chips to less than 100 μm thick compared to a standard silicon chip, which is approximately 500 μm thick. The thinned GaAs chips are extremely fragile, making assembly difficult. The answer to high-temperature, high-power operation may lie in alternate semiconductors such as silicon carbide[7] or a III-nitride–based compound such as GaN.[8] Silicon carbide is by far the most mature of these materials. In fact, mass-produced single-crystal SiC wafers have been commercially available for more than a decade, while III-nitride device crystals have been grown mostly by heteroepitaxy on foreign substrates such as sapphire or SiC. Such III-nitride growth processes are expensive, have limited ability to be scaled to large-volume production, and produce relatively poor quality (high defect density) III-nitride crystals. SiC device crystals typically have orders of magnitude fewer defects (crystal dislocations) than GaN, and thus are closer to becoming commercial electronic devices. Silicon carbide possesses many favorable properties that make it suitable for high-temperature, high-frequency, and high-power applications. These include wide bandgap, high thermal conductivity (better than copper at room temperature), high electric field breakdown strength (approximately 10 times that of Si), high saturated drift velocity (greater than GaAs), and chemical inertness.

While SiC sounds promising, several problems must be overcome to achieve commercial success. Defect density, although much better than in III-nitrides, is still a major issue in SiC. Defects stack and form micropipes, i.e., small holes (0.1–5.0 μm in diameter) that penetrate the substrates. These micropipes can cause shorts and other leakage conditions that can destroy or seriously degrade device performance. The density of the micropipes is on the order of 10^3 micropipes/cm^2 for the best commercially available substrates. Such a density, assuming a uniform distribution, would result in an extremely low yield for devices (ICs) larger than a fraction of a millimeter. Other problems include producing thick SiC layers (greater than 50 μm) with low doping levels (less than 10^{15} carriers/cm^3) and long minority carrier lifetimes. A recent announcement by the Toyota Central

Research and Development Laboratories in Nagakute, Japan, has indicated that Toyota has produced SiC single crystals up to 7 cm across, with defect densities in the range of 10/cm^2 or a 2 order of magnitude improvement over conventionally produced SiC, hence allowing the production of larger devices with reasonable yield.

Despite nonoptimal crystals, low-power prototype SiC electronic circuits,[9–11] as well as III-nitride devices, have demonstrated operation in the 300°–600°C temperature range. In fact, SiC devices have demonstrated transistor action well above 900°C. Given such demonstrated performance, SiC holds significant promise for solving instrument and sensor high-temperature application problems in airplanes, spacecraft, automobiles, manufacturing and power plants, deep Earth exploration and oil drilling, and high-power communications. Such robust high-temperature performance would also provide a measure of security for our electronic systems against the effects of nuclear or other weapons that generate high temperatures. In addition to the devices themselves, high-temperature packaging will also be a major challenge to the widespread deployment of SiC or GaN.

Carbon Nanotubes

Today, MOSFETs are the mainstay electronic devices for ICs. The dominance of MOSFETs over other device types is mostly due to their desirable scaling properties. As dimensions of the MOSFET shrink, the device gets faster and consumes less power, thus fueling the ever-increasing desire for more devices on a single piece of silicon (Moore's Law). Current MOSFETs have gate lengths on the order of 100 nm, with a projected minimum feature size of 50 nm by the start of the next decade. By the middle of the next decade, many researchers believe that the MOSFET will encounter critical technological barriers and even fundamental physical limitations to any further size reduction. Yet, scaling fuels the economic engine of the electronics industry, so there is a very strong push to find new devices (materials) that overcome some or most of the problems anticipated with the continued scaling of MOSFETs. Carbon nanotubes (CNTs) are considered by many researchers to be the answer.

Sumio Iijima[12] first observed CNTs in 1991 while studying soot produced by the electrical discharge between carbon electrodes. Iijima's nanotubes consisted of several graphite sheets (composed of multiple layers of carbon atoms) rolled into concentric cylinders. These concentric cylinders are now called multiwalled nanotubes. In 1993, Iijima and others found that by adding small amounts of catalytic metals to the carbon electrodes they could produce CNTs consisting of a single atomic layer of carbon (graphite structure) for the walls. These CNTs are now called single-walled nanotubes. Today, various techniques, including laser ablation of carbon targets and metal-catalyzed chemical vapor disposition, have been used to produce CNTs. Single-walled CNTs are the more promising structures for electronic applications.

Single-walled CNTs are typically 2 nm in diameter and can be up to several millimeters in length. Given the extremely large length/width ratio, CNTs behave like ideal 1-D systems. They are incredibly strong (their tensile strength is many times greater than steel), with extremely high thermal conductivities (comparable to diamond). The method of preparation and tube properties (such as diameter) determine whether a nanotube acts as a metal or a semiconductor. The existence of both types of single-walled CNTs has raised hopes for the creation of all-carbon–based nanoelectronic technology in which the active devices are semiconducting single-walled CNTs and the electrical interconnects are metallic CNTs.[13]

Various types of devices can be made from single-walled CNTs. The most significant appears to be the CNT field effect transistor (CNTFET), which parallels the silicon-based FET of today's conventional technology. Schematic representations of CNTFETs are given in Fig. 2. Conventional FETs have limitations upon further scaling, including quantum mechanical tunneling as the length of the channel and the thickness

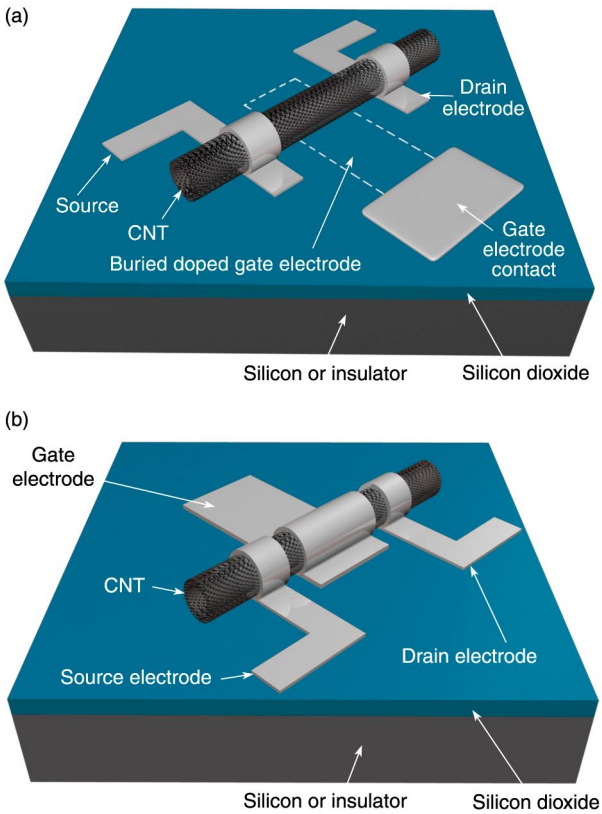

Figure 2. Schematic representation of CNTFETs: (a) bottom gate and (b) top gate.

of the gate oxide decrease. This tunneling creates large leakage currents, which degrade the function of the transistor as a switch. The leakage currents also contribute to high standby power and overall chip power consumption. Metallization on scaled FETs shrinks in cross-sectional area, leading to increased resistance (resulting in reduced chip and system performance). In addition, closer line spacing leads to a greater propensity for electromigration-induced shorting. Single-walled nanotubes are 1-D systems, which do not allow the small-angle scattering of electrons (or holes) by lattice defects or phonons that occur in 3-D systems. In CNTs, carriers have only two directions of propagation—forward or backward. The backscattering that results in electrical resistance requires carrier momentum reversal, and the probability for this to occur in a CNT is extremely small. Because of the reduced scattering, single-walled CNTs exhibit lower resistivity than conventional 3-D devices. In metallic nanotubes, electronic transport is ballistic (no scattering) over a few micrometers of length at room temperature. Even semiconducting nanotubes exhibit ballistic behavior over at least a few hundred nanometers. Thus, energy dissipation in single-walled nanotubes is minimal and channel power density concerns are significantly reduced. Nanotubes do not suffer from electromigration, and metallic nanotubes can carry current densities 100–1000 times greater than metals such as aluminum or copper—the metals used on today's semiconductor chips.

Semiconducting single-walled nanotubes are direct bandgap materials (nominally a 1-eV bandgap) and can directly absorb and emit light, thereby offering the potential of enabling a new optoelectronics technology based on single-walled CNTs. Both n-type and p-type CNFETs can be produced, thus giving promise that today's CMOS technology can be realized with nanotubes at a much smaller scale. Single-walled CNTs are ideally suited for CMOS applications because they have symmetric valence and conduction bands, and electrons and holes have nearly the same effective mass. One-dimensional Schottky barrier–like devices can also be formed at metal/single-walled CNT interfaces. If the interface gate insulating layer is thin enough, Schottky barrier CNTs become ambipolar. An ambipolar device displays electron conduction when a positive bias is applied and hole conduction when a negative bias is applied. Under certain bias conditions, electrons and holes can be simultaneously injected from the opposite ends of the CNT. Such behavior, although not useful in the normal transistor-based circuit technology of today, offers great promise for optical light sources.[14] Single-walled CNTs have also been suspended between two electrodes and used as electromechanical oscillators. Stable oscillations between 3 and 200 MHz have been demonstrated. Not only can they be used as a frequency standard but also, because of their extremely low mass, as a sensor. Such a sensor holds the promise that it might be able to weigh an atom.[15]

Other Devices

Other semiconductor-based technologies, such as integrated optics[16] and microelectromechanical systems (MEMS),[17] should see major growth in product applications as their technology matures. Each of these will exert significant influence on both device development and electronic packaging activities. With the combined influence of new device technology, the sensing and transduction aspects of MEMS, and the wide bandwidths (information handling ability) afforded by integrated optics, electronic miniaturization is headed for complete system integration onto a single piece of semiconductor material. The complexity and natural differences between the optical and microminiature mechanical world make thorough discussion of their impact on miniaturized electronics and its packaging impossible in a short article. However, certain fundamentals can be explored.

MEMS devices are mechanical and electromechanical parts fabricated at micrometer scales using the design and processing methods associated with the IC industry. A MEMS device consists of one or more mechanical elements (e.g., cantilevers, hinges, pivots, shutters, gears, etc.) that are free to move under externally applied forces or internally generated electric or magnetic fields. Applications for MEMS technology range from simple mechanical parts used as sensors and actuators to complex systems combining extensive electronic control and signal processing integrated on the chip adjacent to the mechanical parts.

Effectively integrating electronic circuitry on the same chip with the MEMS parts, together with the appropriate packaging, is challenging, especially for high-density electronic circuitry. Integrated systems combining active electronic circuits with MEMS pressure sensors, accelerometers, and optical mirrors have already achieved commercial success. Devices such as chip-sized chromatography systems, fluid pumping systems, and microphone amplifier systems will soon penetrate the marketplace. Since most MEMS layers and structures are relatively thin because of process limits in the thickness of the sacrificial layers (typically polysilicon), it is difficult to make mechanical devices such as motors and actuators that need large cross-sectional areas to deliver larger forces or torques. This "thickness" problem has been partially solved by the development of the lithography, electroplating, and molding process (LIGA).[1] In the LIGA process, metals such as nickel are patterned plated within steep photo-resist walls to thicknesses of 200 μm or greater, increasing the respective cross sections by a factor of 100 or more. APL activities in the MEMS arena have been detailed in previous articles.[1,16,17]

DEVICE TECHNOLOGY AND ITS IMPACT ON APL

APL is not in the chip fabrication business, although we tried in the early years of the transistor/IC revolution.[18] We rely on commercial sources for a steady supply of ICs. Generally, we use chip designs that originate with commercial vendors and apply them in standard or unique ways. There are two exceptions to these commercial-off-the-shelf (COTS) designs. One is the use of gate arrays where the vendor supplies a standard chip composed of multiple circuit building blocks and APL engineers specify how they are interconnected. The latest embodiment of the gate array at APL is the field programmable gate array (FPGA). In FPGAs, the interconnections between building blocks already exist; in fact, all functions are accessible through a series of electrically programmable fuses and antifuses. In this way, different circuit configurations can be achieved with the same chip by developing different programming algorithms. Once the interconnected pattern is developed in software, the FPGA is placed in a special hardware unit that programs (opens and closes fusible links) or "burns" the interconnected pattern into the chip itself. The second exception is the design of custom ICs that are needed when neither COTS nor FPGA components can meet the circuit and system requirements. APL has a long, successful history in designing custom chips.[1]

The importance of ICs to APL cannot be overemphasized, and we must have assured access to a wide array of ICs to meet the varying sponsor system demands. As the future of IC technology evolves, APL must keep pace with the latest changes in device technology to be a smart applier. As noted above, these changes can be quite radical, ranging from digital chips with over 10^9 transistors to high-performance microwave chips based on SiC and GaN technology. Chips are not only becoming denser and using more exotic semiconducting materials, they are also becoming more adaptable. Unlike FPGAs and custom chips, certain new chips can actually change their circuit configurations at will under software control. These adaptable chips will certainly find their way into many future APL system developments. While much of the above discussion involves enhancements of traditional electronic circuitry and components, many new challenges face circuit designers, including new materials and radically new devices such as the CNT. APL must continually enhance its knowledge of advanced device technology and be fully conversant in its application to ensure that our customer needs for electronics will be met in the future.

ELECTRONIC PACKAGING

While chip (IC) technology and performance seem to be growing without bounds, the electronic packaging world is undergoing major changes to try and keep pace with the ever-increasing demands imposed by the ICs and the end-use system applications. Packaging is defined as the methodology for connecting and interfacing the IC technology with a system and, ultimately, the physical world. In recent years, there have been major shifts in packaging as it responds to the changing worldwide electronics industry. In today's electronic world, the emphasis is on portability. Along with portability go several other system-level factors, e.g., small size, low weight, low cost, high functionality, ease of use, and connectivity (wireless). These system-level drivers pervade electronic products from PCs and wireless telephones to military field hardware, biomedical instrumentation, and spaceflight electronics. Small, lightweight, low-cost, highly functional, and connected hardware products are key to all modern electronic system applications. Such hardware products and their associated system-level developments have forced major paradigm shifts in electronic packaging. These paradigm shifts are schematically captured in Fig. 3

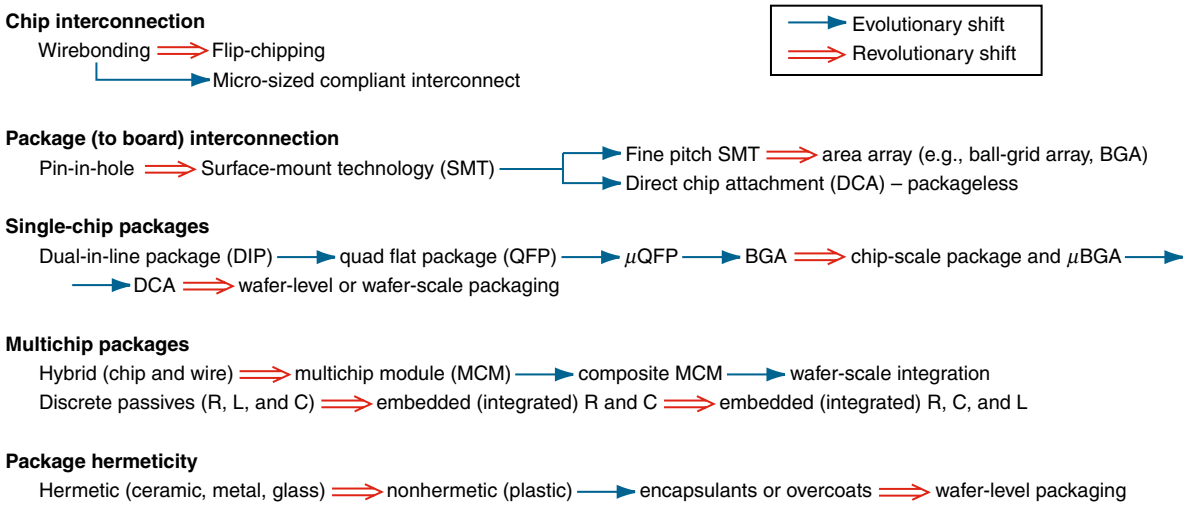

Figure 3. Electronic packaging paradigm shifts.

for some of the most important concepts in the electronic packaging arena.

As mentioned above, both integrated optics and MEMS will play extremely important roles in the performance of future "electronic" systems. Their impact on packaging will be significant as the electronic world shifts from individually packaged integrated components to fully integrated systems. The development of integrated package elements containing optical, electrical, and mechanical devices and systems, all operating in complete synergy, will be routine.

Even with today's high-density packaging, packaging efficiency (ratio of the area of the IC chips to the area of the underlying printed wiring board or PWB) is still extremely low (nominally 8–10%). The full integration of all components (e.g., resistors, capacitors, inductors, waveguides, optoelectronics, etc.) has the potential to raise the packaging efficiency above 80%. Such a concept, as schematically pictured in Fig. 4, requires packaging technology to advance to the point where individual passive components, optoelectronic components, and RF or microwave components are embedded in the board and thus do not take up additional board surface area. With this component integration and the extensive wiring density made possible by the use of thin-film conductors, the surface of the board can be covered with flip-chip bonded ICs (in a close-packed configuration).

Interconnections

There is a major shift in first-level interconnect (chip to package or board) from wirebonding to flip-chipping. Although not new,[19] flip-chip technology continues to make major inroads into the electronic packaging world, which was solely dominated by wirebonding a few years ago. Still, despite the trend toward flip-chip interconnection, more than 10^{12} wirebonds are made annually.[20] Flip-chipping is more costly than wirebonding, even in high volume, because of the increased IC processing required to put the solder balls on the bonding pads and the need for special reflow equipment. Despite the increased cost, the switch to flip-chip interconnections is necessary to increase chip performance. Wirebonds have frequency response limitations (loss), which limit their effectiveness to frequencies less than 10 GHz. The short, robust pillar of the flip-chip joint exhibits low signal loss at frequencies exceeding 100 GHz. While digital circuits are not operating at these clock frequencies (>10 GHz) today, the current rise times of high-performance IC clock signals are 100 ps or less, thus necessitating low-loss signal paths with interconnect bandwidths approaching 35 GHz.[21] Figure 5 illustrates typical wirebond and flip-chip interconnection geometries.

The attachment of bare ICs directly to a circuit board (without a single-chip package) by either wirebonding or flip-chipping will increase. Such direct attachment will provide new interconnection challenges as circuit boards evolve from the standard glass-fiber–reinforced PWBs (rigid boards) to thin, nonrigid board structures (flex boards or flex tapes). Wirebonding on nonrigid structures has been studied extensively, indicating that by changing bonding parameters and bonding frequency, strong bonds can be effected.[22]

Flip-chip interconnects are also being used on flexible circuit boards. While the flip-chip to flex attachment process (solder reflow) is relatively straightforward

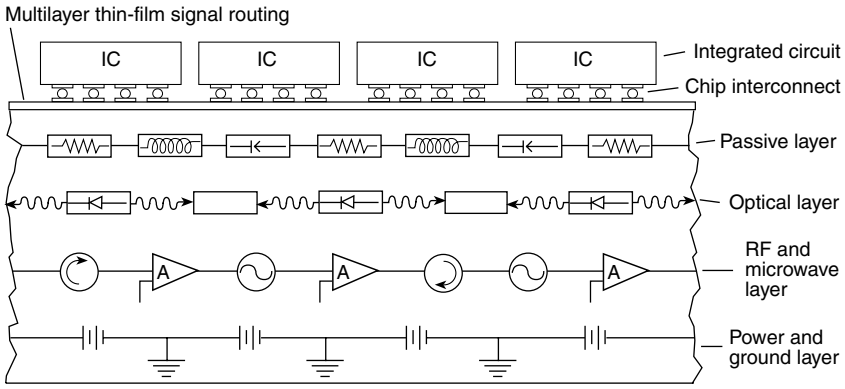

Figure 4. Schematic representation of next-generation integrated substrate technology with embedded RF, microwave, optical, and passive component layers coupled with integral power and ground.

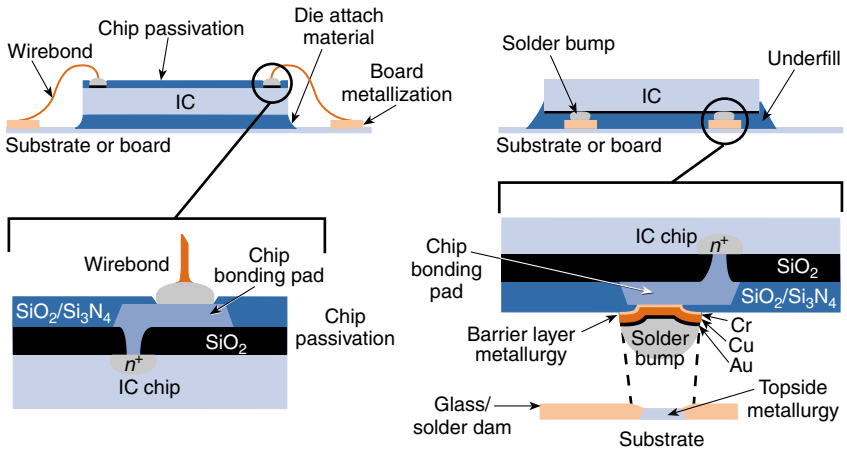

Figure 5. Schematic representation of wirebond (left) and flip-chip (right) geometry.

without the bond attachment, some concerns associated with wirebonding remain. One major concern is a potential reliability issue arising from the coefficient of thermal expansion (CTE) mismatch between the rigid semiconducting chip (low CTE) and the unreinforced flexible circuit board (high CTE). Large CTE mismatches between chip and circuit board can produce large strains on the solder joints, leading to fatigue failure. This problem is exacerbated when the chip geometry is large and the diameter of the solder ball interconnects is minimized to achieve high density (large input/output numbers). A possible solution to the reliability concerns is the use of underfill, which is an epoxy injected between the chip and the circuit board to fill the space and "glue" the surface of the chip to the surface of the board while fully encapsulating the solder joints. The use of underfill on flip-chip-standard fiber-reinforced PWB assemblies (rigid boards) has been shown to significantly improve reliability. Underfill for flip-chip on flex is only beginning to be applied in volume production with mixed results on reliability improvement. Since most of the semiconductor material in an IC chip is only needed for handling the wafer and chip during processing, the use of thinned die on flex holds promise for solving reliability issues without underfilling.[23] Die as thin as 25 μm have been attached to 25- to 50-μm-thick flex boards, making overall flexible assemblies less than 100 μm thick (see Fig. 6). Special handling methods for these thin chips have to be used to avoid damage during assembly.[23]

Driven by cost and process complexity, alternatives to conventional flip-chip technology are being pursued. Two examples are shown in Fig. 7. Both use single-ended ball bonds, produced by automatic wirebonding machines using special wire, that are placed on the chip's bonding pads coupled with a conducting organic adhesive. In the first technique, these single-ended ball bonds or "stud bumps" are placed and then coined or tamped to achieve uniform height above the chip surface. The stud-bumped chip is then pressed on a plate containing a thin layer of conductive adhesive. As the chip is lifted from the plate, a small amount of the conductive adhesive adheres to each bump. The chip is then placed

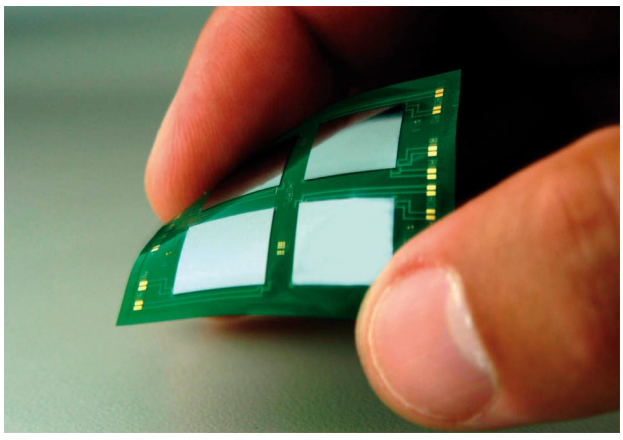

Figure 6. Ultra-thin silicon on flexible circuit board assembly. The chips are 50 μm thick and each contains 1368 solder bumps. The flex board is also 50 μm thick.

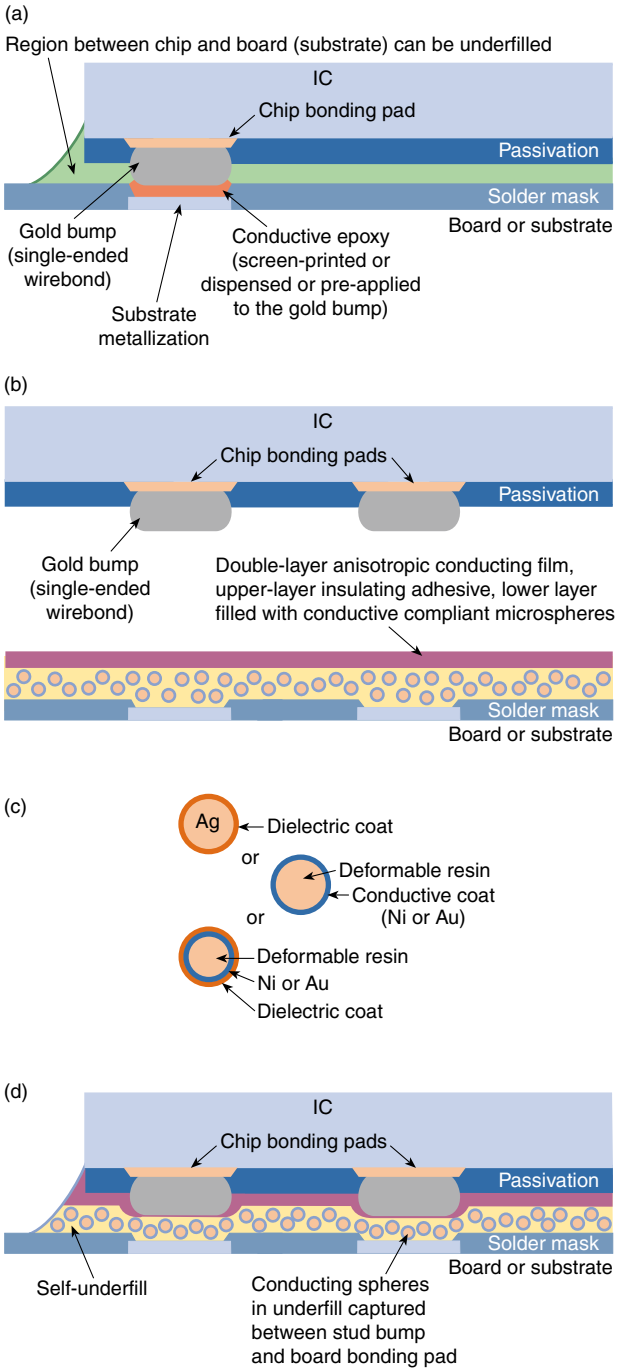

Figure 7. Adhesive-based flip-chip technology. The stud bumps (single-ended wirebonds) are placed on the chip using an automatic wirebonder: (a) standard conductive epoxy attach, (b) double-layer anisotropic adhesive pre-applied to board, (c) conductive filler particle detail, and (d) chip attached to board with double-layer anisotropic conducting film, which also provides a self-underfill.

on corresponding substrate pads and held in place while the adhesive cures, resulting in the geometry shown in Fig. 7a. In a variant of this technique, the epoxy can be pre-applied to the substrate by screen printing.

The second example uses an anisotropic adhesive, i.e., an adhesive that has small electrically conductive particles embedded in a nonconducting organic matrix. A bumped chip (Fig. 7b) is then pushed down into the adhesive, capturing a few conducting particles between the bump and the mating bonding pad on the package or substrate. Typical particle details are shown in Fig. 7c. When the adhesive is cured, an electrical interconnect is made. Also, the anisotropic adhesive fills the entire gap between the chip and the substrate (Fig. 7d), thus acting as an underfill once it is cured.[24] Such a technique holds significant promise for future low-cost flip-chip implementations, provided processing, repairability, and reliability issues can be resolved.

Numerous other advanced interconnect schemes have been proposed over the years, ranging from laser pantography to mechanical spring-like fingers. Laser pantography used a laser to deposit metal traces by decomposing a metal-bearing gas in a sealed chamber directly on the chip and substrate. While achieving high linear I/O numbers (over 600 I/Os per centimeter), the complexity of the process, including the need to taper the edges of the semiconductor, made the cost prohibitive. Mechanical finger-like interconnects have appeared from time to time. Several years ago, micromachined fingers of metal or conductive silicon were proposed as a replacement for wirebonding. These MEMS-like structures received little attention because the trend for high-performance interconnect was toward the flip-chip solder joint.

Today, people are developing flexible leads that attach to flip-chip or ball-grid array (BGA) solder pads and bridge the gap to the bonding pad. These wires or ribbons come in many materials and shapes, ranging from gold wirebonded "S"-shaped leads to flexible copper ribbons that are either straight or fabricated in a spiral. Such compliant leads take up CTE mismatches between the inorganic die (low CTE) and the organic substrate (high CTE). Long columns made of solder or wire (solder attached at both ends) are also used. Schematic representations of such lead systems are shown in Fig. 8.

Single-Chip Packaging

Individual or single-chip packaging technology is rapidly evolving in two major directions: (1) grid array packages, such as BGAs, are rapidly replacing current high-density surface-mount packages, such as the quad-flat package (QFP; a rectangular or square package style with perimeter leads on all four sides), and (2) chips are being mounted directly to underlying circuit boards without a package structure. This direct mounting is described in the literature as either direct-chip attach (DCA) or chip-on-board. Compared to the QFP and the old through-hole–mounted dual-in-line package (DIP) that still exists in most electronic products today (accounts for well over half of the single-chip packages), the BGA offers significant advantages, including constant I/O density (regardless of the total number of I/Os). Because the I/Os are spaced on a grid, the I/O density can remain

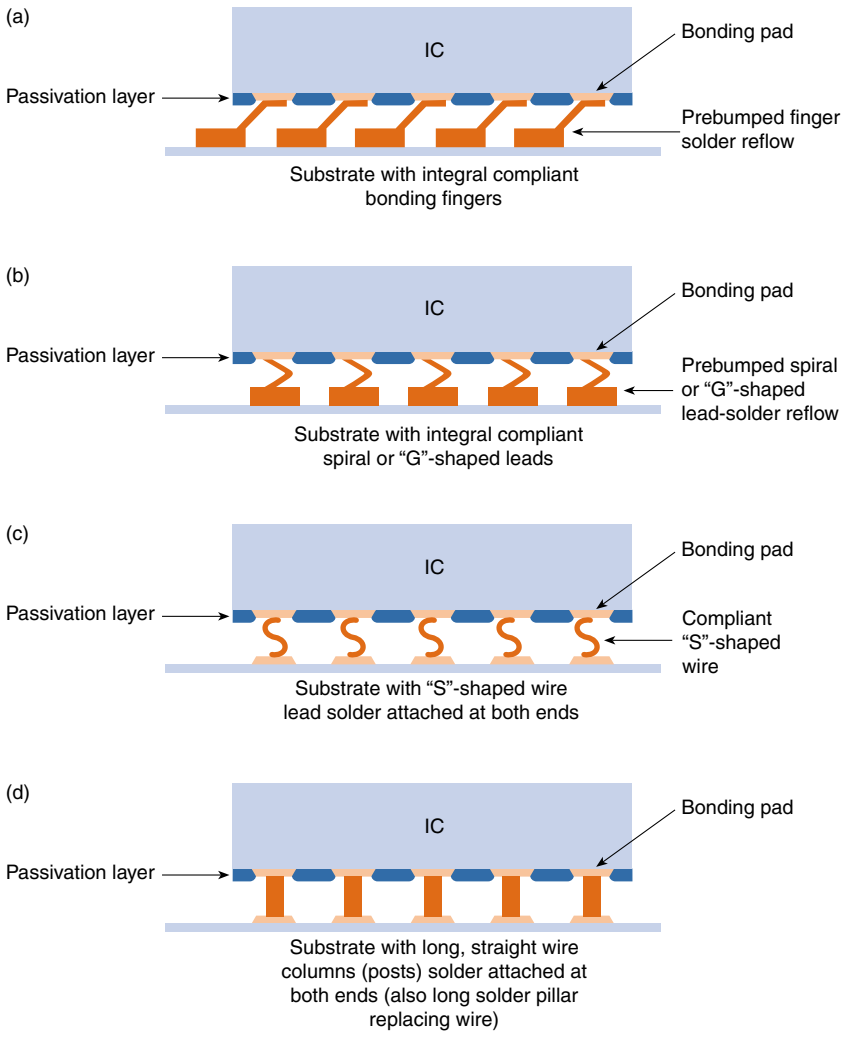

Figure 8. Schematic views of compliant chip interconnection methods.

constant as the package size or I/O number increases, facilitating board design and minimizing differences in path length. The importance of the BGA is evidenced by its rapid growth to second place behind the DIP as the dominant single-chip packaging style. It is also rapidly spawning high-density versions, such as the micro-BGA, as well as a whole family of high-density, minimal volume packages called chip-scale packages (CSPs). CSPs are defined as package structures with footprint areas not much larger than the chip itself. Typical CSP definitions require that the total area of the CSP must be less than 1.5 times the area of the enclosed chip. Historically, packaged parts are preferred to DCA because packaged parts can be fully pretested and then attached with simple solder reflow operations without having to handle fragile ICs. Other advantages and disadvantages of CSPs versus DCA have been given previously.[25]

Multichip Packages

The multichip module (MCM) is the current focus of most multichip packaging activities involving bare chips placed closely together on a multiconductor layer substrate, as contrasted to individually packaged single chips soldered to a PWB. MCMs exist in three primary forms based on the type of substrate used for the interconnection between the chips:

1. MCM-C: screen-printed conductors on either screen-printed ceramic dielectric layers or thin green-state ceramic sheets[26]
2. MCM-D: deposited and photolithographically patterned metal and insulating thin-film layers on a silicon or highly polished ceramic carrier
3. MCM-L: copper conductors laminated to organic dielectric layers similar to PWBs but with finer traces and a different method for producing the interlayer connections (vias)

Chips (ICs) are mounted and interconnected to these high-density substrates by using either wirebonding after the back of the chip has been attached to the substrate (die attach) or by flip-chipping. The MCMs are then connected to conventional circuit boards (e.g., PWBs) using area array solder bumps or pins. Sometimes in the past, they have also been placed in larger versions of conventional packages such as QFPs.

In MCMs, the active devices (ICs) cover more than 50% of the substrate area, in contrast to the traditional packaging density of 8–10% mentioned above. The integration of passive components (R, C, and L) into the substrate structure is important in extending MCM technology to a broader range of applications. Integrated or embedded passives are well proven in MCM-C technology and have achieved limited production in MCM-D modules. Organic-based inductive and capacitive (dielectric) layers compatible with MCM-Ls are under development. Organic-based resistive layers for PWB applications already exist.

Each of the three major MCM technologies has certain advantages and disadvantages as described previously.[26] Which technology is the most important for the future? Many packaging experts feel that, as MCM technology evolves, only two technologies will survive: MCM-D and MCM-L. MCM-D will survive because it has the required performance and interconnect density needed for the next-generation ICs; however, its disadvantage is the complexity of the process and, hence, higher cost. MCM-L will survive because of its low cost, despite its present lack of density. MCM-C is a middle-ground technology with circuit densities greater than those of MCM-L but less than those of MCM-D. Similarly, ceramic technology typically costs more than the organic-based laminate technology used in MCM-L, but much less than MCM-D with its complex processing and patterning steps. MCM-C technology is used widely in modules for cell phones and other RF and microwave applications. It typically offers reduced size with relatively good thermal conductivity for high-power applications. Its major disadvantage over MCM-L and MCM-D is its use of inorganic dielectric layers with high relative dielectric constants (8–10). Even some glass-filled inorganic dielectric layers used in ceramic co-fired technology[26] still have relative dielectric constants in the range of 5–6, and they have reduced thermal conductivity. Low dielectric constant layers are necessary for achieving high-speed system (interchip) performance.

Two other multichip packaging schemes are worth noting. The first is the 3-D stacking of chips as shown in Fig. 9. The 3-D stacking of chips is designed to reduce the board area or footprint of the high-density stacked component at the expense of vertical height. Because of the stacked nature of the multiple devices and the difficulty of connecting each device to separate pads at the board level, 3-D stacking tends to be most popular with parallel, relatively low I/O chip architectures such as memory.

Currently, as many as six to eight die have been vertically stacked or horizontally layered. Future projections using thinned die may allow the number of die in the stacks to go even higher. If a chip in a stacked die package fails, the entire package is usually discarded. Also, in complete analogy to stacked chips, entire circuit boards could be stacked using prepatterned compliant interposers. The interposers have through-board conductive channels, allowing the I/O of one circuit board to be connected to the next. The stacked assembly would be either clamped mechanically or encapsulated to ensure good electrical contact. If clamped, the 3-D board stack could be repaired.

The second MCM technology of potential future interest is a method where the chips are embedded in

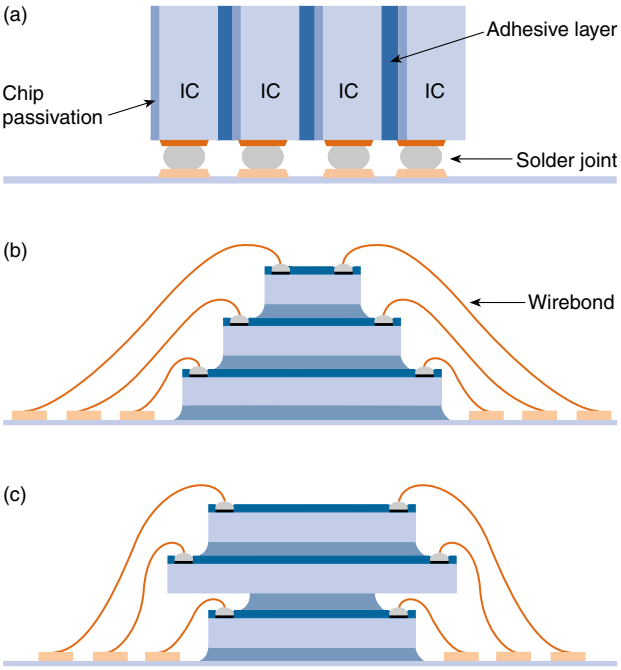

Figure 9. Three-dimensional stacking of ICs: (a) vertical stack edge mounted, (b) horizontal stack with decreasing die size, and (c) horizontal stack with overlapping (cantilever) die. (In wirebonded chips, wirebonds in and out of the page are not shown for clarity.)

a carrier substrate flush with the substrate's surface (Fig. 10). The space around the chips is then filled so that the chip and carrier appear as a smooth single unit. Multilayer thin-film interconnects using MCM-D technology are then deposited on the planar chip/carrier surface. The result is a monolithic module of extreme density and potentially very high performance, both electrically and thermally. This "chip-first" technology has a major drawback in that it cannot be repaired. Once encapsulated and overlayered with interconnect, the chip cannot be removed; thus the complex module is a throwaway. Repair schemes such as dissolvable substrates have been investigated. If dissolvable substrate techniques work, then extremely low profile board assemblies can be made—especially with thinned die as shown in Fig. 6.

Wafer-Scale Packaging

A major focus of the semiconductor industry in the last decade has been the creation of ever-smaller high-performance packages for ICs and other electronic components. The primary drivers for reduced size (and weight) packaged parts are consumer products such as camcorders, digital cameras, cell phones, and other wireless devices.

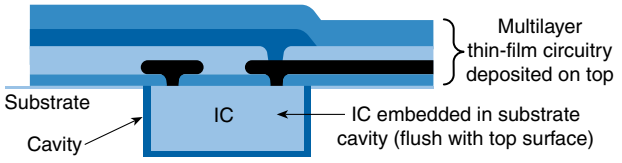

Figure 10. Chip-first high-density interconnect.

The solution to the performance and small size issues has been the introduction of CSPs as mentioned above. Currently, wafer-scale packages (WSPs) or wafer-level packages (WLPs) are a small but emerging subset of the CSP market. In WSPs, the package structure is built on the IC at the wafer level. This includes both the environmental protection and the redistribution of I/Os. WSPs or WLPs offer significant promise for even smaller size and much lower cost. Other WSP benefits include enhanced speed, reduced packaging and test cycle time, improved process feedback control, and shortened time to market for new products. WSPs ultimately will eliminate the need for conventional packaging operations, provided chip yield is high. In WSPs, the "packaged" parts would be tested and burned in (thermally screened) on the wafer before dicing, in contrast to today's packaging operations, which only assemble functioning ICs after they have passed wafer-level testing and have been separated. Thermal screening, if necessary, would be performed on the electrically good packaged parts. A schematic representation of the WSP process is shown in Fig. 11.

Currently, WSPs are in production for low I/O count products (<100) where large pitches and solder balls can be used to mitigate the reliability concerns generated by CTE mismatches between the chip and the circuit board. Large solder balls (≈200 μm) and pitches reduce the need for underfilling.

As the demands for increased I/O continue (prediction of 10^4 I/Os on a single chip within the decade are now common), the need to provide a WSP solution to these high I/O demand numbers is paramount. The

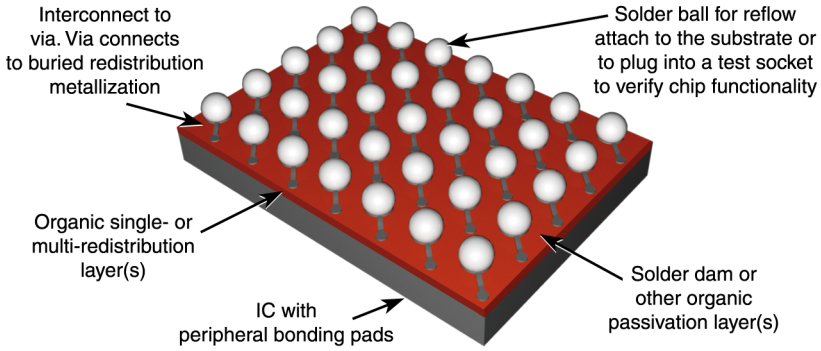

Figure 11. Schematic representation of wafer-scale (-level) packaging. An organic redistribution layer and integral passivation are applied at wafer level before chip separation. Thus chips are "prepackaged" as they are sawn from the wafer

approach to date has been the development of very flexible short leads at reduced scale. Since features of these packaging elements have dimensions below 0.1 μm, the industry is beginning to call this advanced miniaturized on-wafer packaging technology "nano-WSP" (or nano-WLP).

PACKAGING TECHNOLOGY AND ITS IMPACT ON APL

Electronic packaging is a key enabler for the implementation of all APL-developed electronic systems. Whether the packaging is simply the soldering of a commercially packaged part on a PWB or the more advanced application of a thinned custom die on a flexible substrate less than 25 μm thick, it is extremely important to the reliability and performance of the system. Packaging in its truest sense provides mechanisms to get the wanted electrical signals to and from the chip, provide heat sink paths to dissipate excessive thermal energy, provide strength and support to fragile chip elements, and protect this chip from the environment and in certain cases (human implants), the environment from the chip.

APL has had a long history of successful electronic packaging.[1,25,26] In fact the Laboratory has been a pioneer in advanced electronic packaging ranging from simple chip interconnect to the packaging of entire systems for space, ocean, and biomedical use. At APL's founding, the VT fuze was a marvel of advanced packaging.[26] That history has been carried forth on a wide variety of systems that are important to our country and the national defense.

The future holds many challenges for APL in the electronic packaging arena. There have been major paradigm shifts in the packaging world as mentioned above. APL must continue to embrace these changes to be able to handle future devices and circuits. A gradual but steady change from hand to machine assembly must continue to be fostered because of ever-shrinking device and interconnect sizes. Some form of solder assembly will continue to be important for the foreseeable future, but new methods and materials will undoubtedly be used. There is an international push to ban all lead in electronics and APL, even though its operations are small in terms of the electronics industry, will have to follow suit. The change to lead-free solder will require new equipment and processes. The widespread use of flip-chips and WSPs will force changes in our packaging design as well as in the handling, assembly, and testing of packaged boards and systems. Embedded components will require the development of custom in-house processes until commercial sources can provide the flexibility needed to meet APL system requirements. High-power and high-temperature device operation will push the packaging technology even further, requiring robust interconnect and heat sinking configurations capable of sustained performance at temperatures exceeding 300°C.

SUMMARY

APL has a long and innovative history in miniaturized electronics. This history has relied on, and will continue to rely on, access to advanced devices coupled with flexible, custom packaging. The application of advanced devices from adaptable ICs to CNTs requires a working familiarity with materials, technology, and device design and performance. In a similar vein, APL must develop the necessary packaging technology to allow the integration of these advanced devices into system-level applications for our customers. This continual learning, understanding, development, and exploitation of advanced electronic devices and packaging will provide APL with the necessary edge in its prototype systems business.

ACKNOWLEDGMENTS: APL's miniaturized electronics technology is widely based, with key elements residing in most departments. Though too numerous to mention, I am indebted to the many scientists, engineers, and skilled technicians throughout the Laboratory who are developing and implementing electronic systems. Their efforts, both past and present, have made APL an important player in the application of miniaturized electronics to prototype systems. In the future their efforts will be even more critical as device and packaging technologies continue their path of rapid, never-ending evolution.

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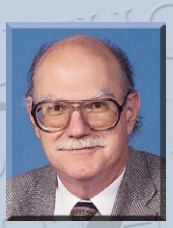

Harry K. Charles Jr.