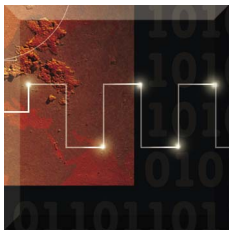

Advances in Ka-Band Power Amplifier Technology for Space Communications Systems

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APL's research and development efforts in high-efficiency Ka-band solid-state power amplifiers have positioned the Laboratory at the leading edge of this technology. APL reached this position through significant contributions in several areas related to the design of power amplifiers. Methods for applying harmonically controlled terminations for improved efficiency (a first at Ka-band) have been developed. To demonstrate this, an advanced transistor model capable of accurately simulating the transistor's nonlinear behavior over a wide operating range was generated by our collaborative partner, Morgan State University. Through the creation of a software tool, the processes required to construct the model was standardized and documented. This device model was then validated by comparing measured performance with the model predictions.

INTRODUCTION

APL has a long history of innovations in small spacecraft design for near-Earth and deep space science missions. In these missions, spacecraft power is a precious resource and must be allocated judiciously to the major subsystems, including the telecommunications system. A power amplifier (PA) is often one of the most critical components of a spacecraft's telecommunications system since the PA's output power and efficiency drive the overall system's power budget. Increased efficiency in a spacecraft PA translates to increased science data return for a fixed DC power budget or reduced DC power consumption for a fixed science return. APL introduced the use of an X-band solid-state power amplifier (SSPA) for the NEAR (Near Earth Asteroid Rendezvous) Deep Space Mission.[1] Since then, the Laboratory has continued to improve the efficiency of SSPAs to provide increased science data and to better position APL for future space missions.

As part of the NASA/APL Advanced Technology Development (ATD) program, APL began work on the characterization of X-band devices and the improvement of their efficiency. This work allowed us to propose a highly efficient, yet low-risk approach to the MESSENGER (MErcury Surface, Space ENvironment, GEochemistry, and Ranging) SSPA. Also, as part of the ATD program, APL developed a 0.5-W, 32-GHz (Ka-band) MMIC (monolithic microwave integrated circuit) PA having 30% efficiency.[2] These important firsts and our continuing research have demonstrated that the design of high-efficiency PAs is an APL strength—a strength that becomes increasingly more important as our mission requirements call for smaller power budgets.

This article presents our effort to build on this strength and advance Ka-band PA technology for space communications systems.

Motivation for Ka-Band Research

The total science data returned from a spacecraft is limited by the downlink data rate and the Deep Space Network (DSN) usage time (and associated cost) allocated for the data downlink. Therefore, improvements in data rates mean either increased total science return for a fixed cost or reduced cost for a fixed science return. A Ka-band communications system with antennas and amplifiers similar to those used at X-band will theoretically yield a 5- to 6-dB increase in effective isotropic radiated power or a factor of 3 to 4 improvement in data rate. This improvement accounts for atmospheric losses, noise, and DSN antenna imperfections, which tend to reduce the gain.[3] Another advantage of Ka-band is that it is more tolerant of solar corona effects than X-band. This is particularly important to the Solar Probe mission.

Solar Probe is a mission that sends a spacecraft close to the Sun (4 solar radii from the center of the Sun) to gather *in situ* data on solar wind, map the magnetosphere, and obtain extreme ultraviolet images. To receive real-time science data from the spacecraft while it is this close to the Sun, the telecommunications system must be designed to overcome the solar impairments on the RF signal.

Studies on Magellan[4] and Galileo[5] spacecraft established that solar corona link degradation was frequency dependent: S-band frequency links were more severely degraded than X-band frequency links. A model[6,7] of radio-wave propagation in turbulent media generated similar conclusions and predicted that Ka-band links would be more resistant to corona scintillation effects than X-band and S-band links. Improvements in link performance at Ka-band have been confirmed by simultaneous transmission of telemetry on X-band and Ka-band links during solar conjunctions with Mars Global Surveyor (MGS),[8] Deep Space 1 (DS-1),[9] and Cassini.[10] But all of these data are from spacecraft that are situated well outside the solar corona.

Through a combination of analysis and simulation based on Webster,[4] Feria et al.[11] predicted that for a spacecraft immersed in the solar corona at a Sun-Earth-probe angle of 1°, a Ka-band link would experience a loss of a few tenths of a decibel, whereas a corresponding X-band link would degrade 8.2 dB. This scintillation loss is in addition to the degradation caused by the angular proximity of the solar disk to the main lobe of the ground station's antenna. The existing body of evidence regarding solar coronal link degradation drives the consideration of Ka-band links for the Solar Probe mission.

The baseline telecommunications system for the Solar Probe mission is driven by the mission science data requirements, solar coronal effects on RF propagation, and the paucity of prime power. The use of a traveling wave tube amplifier (TWTA) was initially considered for the telemetry downlink. However, we were thwarted primarily because of the low prime power (20 W) available for this function. Low-power TWTAs such as those flown on Cassini are no longer available from the TWTA vendor. Other TWTA vendors balk at delivering high efficiency (40%) at low-input prime power because of the fixed amount of filament heater power that is consumed independent of RF output. The Solar Probe baseline subsystem uses eight 1-W SSPA modules with a target efficiency greater than 60%. Since this efficiency exceeds the current state of the art,[12] a strategic plan was developed to significantly improve Ka-band PA efficiency.

Strategic Components

The strategic plan for accomplishing the above goal leverages three principal components: APL Independent Research and Development (IR&D), Morgan State University (MSU) research, and postdoctoral fellow research. The interaction of these components is illustrated in Fig. 1. The APL IR&D is an ongoing effort that focuses on the characterization of RF transistors with the best intrinsic efficiency in conjunction with the application of a circuit technique known as harmonic control to improve efficiency. MSU focuses on the development of an advanced modeling tool that generates adaptable nonlinear RF power transistor device models. One such model, developed by MSU and validated with measurements conducted under IR&D, has demonstrated the ability to accurately predict the performance of the device in a harmonically controlled circuit.

An additional benefit of this collaboration is that the Center of Advanced Microwave Research (CAMRA) within MSU has been operating under a NASA grant.

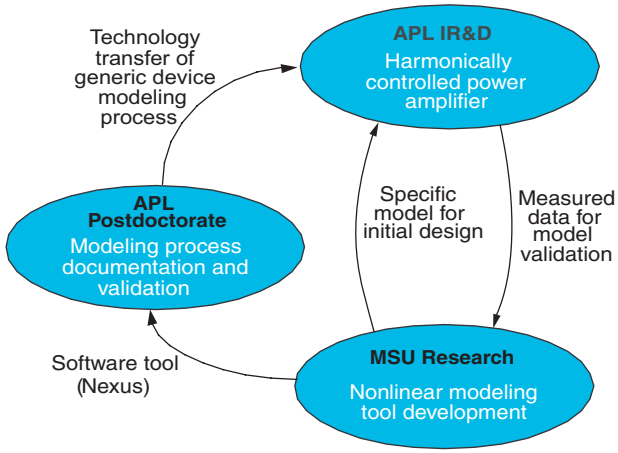


Figure 1. Ka-band high-efficiency SSPA collaboration leverages the strengths of APL and MSU.

CAMRA's primary objective is twofold: the development of microwave technology of interest to NASA programs and the production of advanced engineering degrees in NASA-related fields. A graduate from CAMRA with a doctorate in engineering, whose thesis work involved harmonically controlled Ka-band amplifiers for increased efficiency, is now working at APL under the Postdoctoral Fellow Program. Currently, the focus of the postdoctorate component is documenting a systematic process for the development and validation of adaptable nonlinear neural-network device models.

The following sections present the contributions of the three strategic components to the high-efficiency Ka-band SSPA initiative in more detail.

APL INDEPENDENT RESEARCH AND DEVELOPMENT

Characterization of Advanced Devices

SSPAs in the multiwatt power range typically combine individual field effect transistor (FET) cells by on-chip techniques using low-loss planar combining circuits. At Ka-band frequencies, where circuit parasitic losses have a greater impact on overall efficiency, spatial power combining techniques have been used to achieve the lowest possible losses and least impact on power-added efficiency (PAE). APL's current work focuses on achieving the highest possible efficiency in the unit FET cell structure and, through optimal Ka-band power combining, high efficiency in the overall integrated assembly. Apart from harmonic tuning techniques discussed below, achieving high efficiency begins with the best choice of FET device technology.

The materials structure and processing technology of a molecular beam epitaxy device determine, at a fundamental level, the circuit efficiency that can ultimately be achieved. We have therefore placed considerable attention on determining the best possible device technology for this application. A review of device R&D showed at least one promising approach: metamorphic high electron mobility transistors (mHEMTs). This technology takes advantage of the excellent high-frequency properties of indium phosphide (InP) HEMTs with high indium content in the InGaAs channel and combines it with special materials growth techniques that allow the InP HEMT structure to be built on a conventional GaAs substrate. This avoids some practical and technical difficulties that are encountered when using an InP substrate.[13] Relationships have been established with the appropriate R&D organizations from the commercial sector to take advantage of this device technology in our own Ka-band development program.

Throughout the execution of the IR&D, we have used our load pull measurement system extensively for the experimental evaluation of these high-performance devices. A load pull measurement is a technique for varying the output load termination of a device under test and measuring the power delivered to the load. The load pull system, shown in Fig. 2, consists of input and output tuners mounted on *xyz* positioners for placing the on-wafer probe tips on the device's gate and drain pads. A microscope is placed between the tuners to visually check for proper alignment of the probe tips. We have measured mHEMT device performance in the fundamental load pull system and observed PAE of over 52%, with corresponding power density of 470 mW/mm and associated gain of 9.7 dB at 32 GHz.

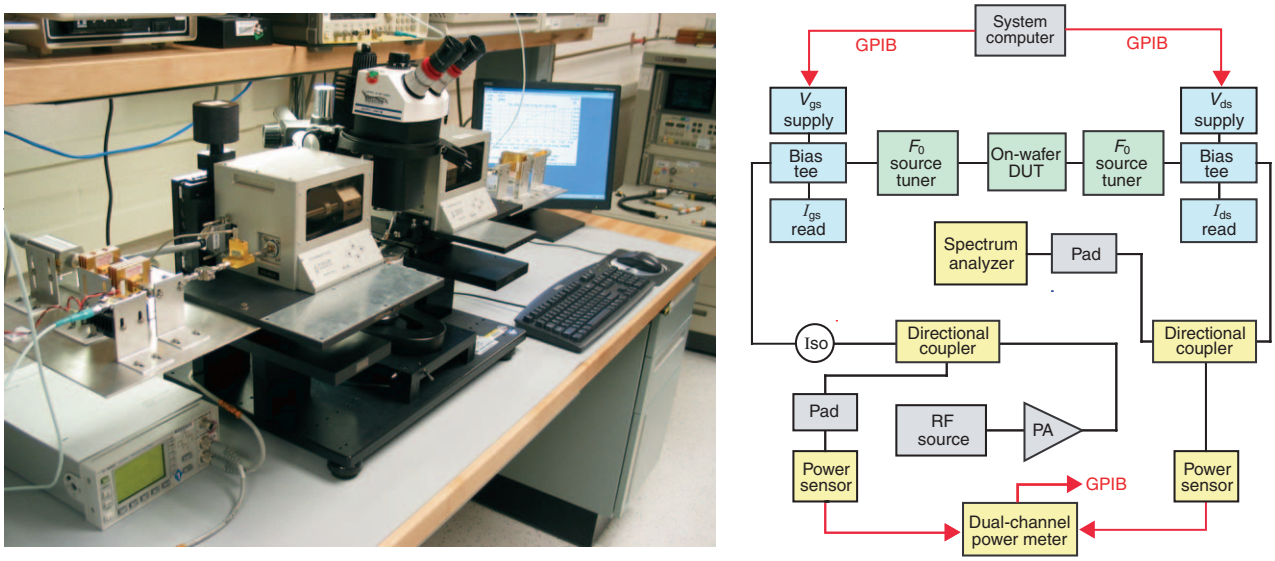


Figure 2. The APL load pull measurement system allows characterization of RF transistors into variable fundamental and harmonic loads. (DUT = device under test, F_0 = fundamental frequency, GPIB = general-purpose interface bus, I_{ds} = drain-source current, I_{gs} = gate-source current, Iso = isolator, PA = power amplifier, V_{ds} = drain-source voltage, and V_{gs} = gate-source voltage.)

In addition to space science applications, mHEMT device technology has many uses, for example, in high-speed digital circuits, lightwave communications, battery-powered devices, and high-frequency/high-efficiency amplifiers for wireless applications. As such, intense commercial interest in further improving the device manufacturability, performance, and reliability is expected to continue.

Waveform Generation Techniques for High Efficiency

The fundamental principle in any type of harmonic tuning of a PA device is to create current and voltage waveforms at the device output terminal to minimize DC power consumption while maintaining the useful RF output power at the output terminal of the amplifier. Various harmonic tuning techniques have been demonstrated numerous times in SSPAs at low frequencies.[14] For harmonic tuning to be useful, the device must be operating in a nonlinear mode where the harmonic signal levels are great enough to achieve useful waveform shaping. These conditions are more suited to applications in which strict linearity performance specifications do not apply or when efficiency performance is much more important than linearity. In the linear range of operation, the efficiency performance is largely independent of harmonic tuning.

In a mode of operation known as Class-F, the drain voltage includes odd harmonics to approximate a square wave while the drain current waveform includes even harmonics to approximate a half-sine wave. Class-F operation refers specifically to the manner in which the output tuning circuit is designed at the harmonic frequencies, as opposed to the more traditional Class-A or -B modes discussed later that refer to the level of quiescent drain-source current set by the gate voltage. The Class-F composite waveforms are shifted in phase by 180° so that the current is low when the voltage is high and vice versa. A similar tuning method, known as inverse Class-F, creates a condition in which the voltage approximates a half-sine wave and the current a square wave.[15] In either case, the significance of the Class-F method is that it keeps the instantaneous current/voltage product low. Since this represents the power dissipated in the device, the low-current/voltage product tends to boost efficiency.

A low-current/voltage product may be achieved by tuning the load such that either the voltage or current waveform approximates a square wave. To create a square wave in the time domain, one must have odd harmonics of prescribed levels and no even harmonics. These tuning conditions are typically created at microwave frequencies having open or short-circuited transmission lines at the device drain, with the proper electrical length chosen to create the necessary high- or low-impedance conditions at the harmonics. In a practical Ka-band circuit, the design focuses only on the second and third harmonics. Higher-order harmonics have progressively less impact on overall efficiency, and in addition, the extra loss created in the output network with higher harmonic tuning may more than offset the small incremental efficiency improvement.[16] Further details on these classes of operation and current/voltage waveform shaping with harmonic tuning can be found in the PA design text by Cripps.[17]

Nonlinear Model Validation

The key to achieving the cost-effective design of a high-efficiency PA is a computer-aided design (CAD)-compatible FET device model that maintains accuracy over a broad range of power levels and bias voltage conditions. Harmonic generation is also necessary for proper waveform shaping at the drain, thereby yielding high-efficiency operation. Thus, voltage levels at harmonic frequencies must be accurately modeled as a function of load impedance as well as gate and drain bias. In addition, the drain-source current at the quiescent bias point (Class-A to Class-B) will affect efficiency performance and is a useful parameter to examine during circuit optimization in the design phase. This requires that the device model maintain accuracy in gain compression up to saturation as well as gate biases from Class-A operation down to pinch-off. Device models based on closed-form equations have typically shown limitations in both of these regions, compromising a full optimization of amplifier performance.

To overcome these limitations, a new adaptable neural network FET (ANNFET) model was developed that can be dynamically reconfigured by the user.[18] This modeling approach requires measured data on the device in the form of small-signal S-parameters and DC current versus voltage (I-V) data. The S-parameter data files are measured at each point of a grid of up to 100 gate- and drain-bias combinations. This model will contribute to amplifier design technology in several areas:

- The device model is accurate over operating regions where existing models have shown weaknesses.
- It reduces or may eliminate the time and expense of experimental load pull measurements as preliminary steps to PA design.
- It will allow designers to explore the potential benefits of harmonic tuning on both the drain and gate sides of the circuit without the hardware expense of performing measurements using harmonic load pull techniques.

The design of harmonically tuned PAs at Ka-band and higher frequencies is complicated by the difficulty of measuring harmonic load pull behavior at such high frequencies. In our case, the fundamental frequency is 32 GHz, and thus the second harmonic is 64 GHz and the third is 96 GHz. It is extremely hard to obtain useful

harmonic load pull data at these frequencies because of losses and other parasitic effects in the harmonic tuner that are not problematic at lower frequencies. These factors place additional demands on the performance of the device model in that it must predict the harmonic tuning behavior at frequencies considerably beyond the measurement bandwidth of the underlying experimental data used for model extraction.

In this work we have taken a methodical approach of validating the modeling technique, first at S-band, and then at X-band, where harmonic load pull data are readily obtained with existing tuner technology. This effort was successful in validating both the specific device model and the generic device modeling process.[19] For example, at X-band, Fig. 3 shows the modeled and measured results for a 4.8-mm pseudomorphic HEMT (pHEMT). The primary parameters of interest are output power on the left axis and the PAE on the right axis, both plotted as a function of input power. The device gain, also on the left axis, represents the difference between output and input power in decibels. In general, the model versus measured agreement is excellent in the low-power region, roughly less than 22 dBm of input drive for a device of this size. Traditionally, the most difficult region to accurately model, even without the effect of harmonic tuning, is the nonlinear range, where the device starts to saturate as indicated by the leveling off of the output power curve. For this comparison, some deviation is evident in this range, although the agreement is noteworthy and still very useful for the design of harmonically tuned amplifiers.

The measured data were taken using the load pull system in which the fundamental (8.4-GHz) and harmonic terminating impedances are controlled. The good agreement between the model predictions under simulated load pull tuning and measured performance shows the model's ability to predict enhanced amplifier performance under harmonic tuning conditions. Similar agreement was obtained at S-band (2.2 GHz). Note that these simulations are not the result of expressions fit to specific (frequency- and drive-level dependent) large signal data but rather are based on small-signal S-parameters and DC (I-V) data only. Because this method does not depend on empirically derived equations, it is very adaptable to a wide range of devices and frequency and bias conditions.

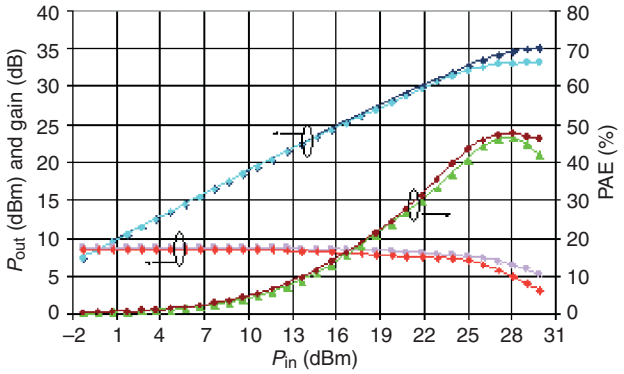


Figure 3. Model simulation and measured output power, gain, and power-added efficiency (PAE) for a 4.8-mm pHEMT at 8.4 GHz. The device model is validated by good agreement with the measured data and can be used to accurately predict future circuit designs. Dark blue = measured output power, light blue = model output power, brown = model PAE, green = measured PAE, purple = measured gain, and red = model gain.

Ka-Band Simulated Power and Efficiency

Neural network models were derived for 300- and 600-μm mHEMT devices using the small-signal S-parameters and DC I-V characteristics of the devices. Thus far, we have incorporated the 300-μm model into the circuit design software and created a prototype high-efficiency Ka-band SSPA design. Figure 4 shows the simulated output power, PAE, and gain of the 300-μm device, with optimal fundamental impedance matching on the input and optimal fundamental and harmonic terminating impedances on the output. A similar amplifier using the 600-μm device cell will be derived using the same approach, taking into account the lower impedance levels in the larger device. The full 1-W amplifier, required for the Solar Probe mission, will use multiple 600-μm cells combined in-phase in the output stage. These results, although only simulations, provide encouragement that the 1-W, 60% efficiency goal is reasonable.

APL AND MSU STRATEGIC RESEARCH COLLABORATION

The APL Space Department RF Engineering Group is working with MSU's Center of Microwave, Satellite, and RF Engineering (COMSARE, affiliated with CAMRA) to support APL's IR&D efforts related to the application of neural-network device modeling techniques. The goal is to significantly improve high-efficiency SSPA technology by developing an integrated computer-aided

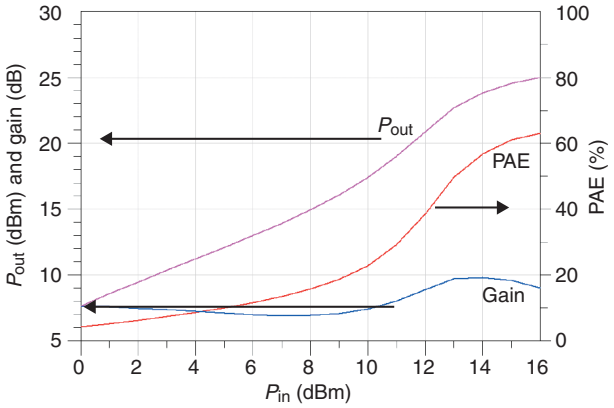


Figure 4. The simulated performance of the 32-GHz, 300-μm amplifier demonstrates the effectiveness of harmonic terminations by achieving state-of-the-art PAE.

environment for the production of user-defined models (see the boxed insert). These models will be implemented into microwave circuit design software and employed to design highly efficient SSPAs using Class-F design techniques. MSU and APL have worked together to validate the device models with linear and nonlinear measurements and have used the models with enhanced matching techniques to design a highly efficient Ka-band SSPA.

To design a state-of-the-art Ka-band SSPA, advanced device models capable of simulating Class-F behavior under extreme bias conditions are needed. These models would require the ability to

- Mimic the highly nonlinear behavior of the transistor over a wide dynamic range, including gate-drain and gate-source capacitance and drain-current sources
- Be driven into high compression (1–3 dB), thereby demanding that the model be more robust and less prone to solution convergence problems
- Update the model for improved accuracy and adapt the model to changing technologies
- Mimic both the DC and RF behavior over the operating range of the device

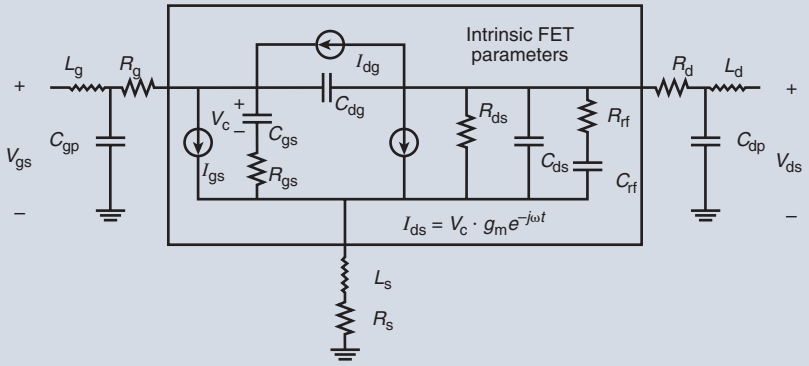
Nonlinear models, commonly integrated within commercially available circuit simulators, are generally either table-based or based on analytical expressions to model the device's nonlinear behavior. Table-based models require extensive device measurements. In addition, because these models depend on the simulator's spline interpolation functions, they often exhibit discontinuities for data external to the measurement domain, which results in convergence problems during simulation.[20] Models based on analytical expressions, while robust, have a very limited dynamic range and require intensive extraction procedures.[21] There is a trade-off in time, cost, and accuracy in choosing the best model. Because of the limitations of the existing models, MSU and APL have developed user-defined

NONLINEAR EQUIVALENT CIRCUIT MODEL

The accurate prediction of amplifier performance requires an accurate behavior model of the active device. A circuit model of the active device is often the preferred method to describe the device because it is more easily adapted over a large dynamic range compared to look-up table-based models and models based on analytical expressions. The circuit model also provides a more concise description of the device compared to a look-up table. A typical nonlinear equivalent circuit for a microwave FET is shown in the figure. Resistors, inductors, capacitors, current sources, and voltages are symbolized with the letters R, L, C, I, and V, respectively. The subscripts g, s, and d refer to the device terminals: gate, source, and drain. The resistance R_{rf} and capacitance C_{rf} allow the model to accurately predict the device dispersive output impedance from low frequencies, including DC through the microwave frequency range. The device transconductance G_m, AC transconductance g_m, and a phase delay τ are independent parameters that determine the drain-source current I_{ds} as a function of frequency ω. Parameters that are shown outside of the intrinsic area are known as extrinsic or parasitic parameters. These parameters represent circuit elements external to the semiconductor device such as bond wire inductance (L_g, L_s, and L_d) and package capacitances (C_{gp} and C_{dp}) that must be included for a practical and accurate model.

Measurements of the DC current versus voltage characteristic (I-V) and RF S-parameters are used to determine the values of the circuit elements. The process of determining these values based on the measured data is known as "parameter extraction." In a linear model, the element values are extracted at a single bias point and the current sources I_{gs} and I_{dg} may not be required. In a nonlinear model, the intrinsic circuit element values depend to varying degrees on the bias conditions. This dependency causes the process of extracting the circuit values from the measured data to be complex and time-consuming.

MSU's COMSARE group has developed an integrated set of software tools, known as Nexus, that provides a systematic, accurate, and efficient method for extracting the circuit element values. Nexus can extract the linear and nonlinear elements of a general equivalent circuit FET model similar to the one shown in the figure. An overview of Nexus can be found in the Appendix.



Equivalent circuit model for the ANNFET provides a very efficient and accurate description of the nonlinear behavior of a typical microwave FET.

models capable of utilizing empirical algorithms embedded within neural networks. This type of neural network is recognized as a knowledge-based neural network (KBNN).

Neural networks have the ability to learn from data, generalize patterns in data, and model nonlinear relationships. These appealing features make neural networks an excellent candidate for overcoming some of the difficulties in traditional device and circuit modeling and optimization.[18] However, to develop nonlinear models using neural networks, a large amount of training data is usually needed to ensure model accuracy. Neural networks, in which knowledge is in the form of analytical approximations, are incorporated into the processing of elements of the neurons, which greatly enhances the accuracy and reduces the need for large sets of training data.

As a result of this research, MSU and APL have developed a KBNN model capable of predicting harmonically terminated SSPA performance.[19] Currently, COMSARE is developing KBNN models to be used by APL circuit designers. To make the development of adaptable models more efficient, the Nexus software developed by COMSARE provides an integrated model development tool that will become the platform for transfer of the modeling technology from MSU to the Laboratory. A detail description of Nexus is provided in the Appendix.

Recall that the ANNFET model can be dynamically reconfigured by the user such that any element of the traditional FET model can be exchanged for a neural network component. A neural network component is defined by an electrical element such as a resistor, capacitor, or current source whose value is determined by a neural network. This neural network also has knowledge in that there are empirical equations in the knowledge layer of the neural-network architecture.

This model shares the advantages of a model based on analytical expressions in that it is very robust with respect to simulation anomalies. Unlike empirical models, however, the ANNFET accurately models the device behavior over the full range of operation and can model highly nonlinear characteristics because of the nature of neural networks. In contrast to table-based models, ANNFET requires a small sample data set based on direct measurements of S-parameters and DC I-V curves. Because the ANNFET is based on a neural network, it inherently has the ability to interpolate between data and the knowledge associated with the model, enabling extrapolation capabilities that cannot be observed in a table-based model.

ANNFET MODEL EVALUATION

Under the postdoctoral research component of the work reported here, a discrete FET was investigated to demonstrate the ANNFET's ability to accurately model a device's small- and large-signal behavior. The discrete FET is based on a Triquint Texas pHEMT process where the gate length is 0.25 μm and the gate width is 600 μm. The device's DC and RF characteristics obtained from measurements are compared to results predicted by the newly introduced ANNFET model and an industry-standard FET model known as the Materka model.[22] The root-mean-square (rms) error between the model's simulated value and measured data quantifies the accuracy of each model's performance. The rms error is given by

$$\text{rms error} = \sqrt{\frac{\sum_{i=1}^{N} (\text{MeasuredValue} - \text{SimulatedValue})^2}{N}} .$$

DC Model

Because the device's drain current exhibits the greatest nonlinearity, the designer must verify the model's drain-source current/voltage behavior over the full operating range of the device. The drain-source current fit indicates how well the fundamental power characteristics will be predicted. Figure 5 presents the I-V data for the 600-μm GaAs pHEMT device. The I-V data illustrate the relationship between the drain-source current I_{ds} and the drain-source voltage V_{ds} over varying gate-source voltages V_{gs} for both nonlinear models and measurements. The ANNFET model predicts the measured I-V curves quite well, whereas the Materka does not. The Materka model's performance is limited by the analytical expressions that describe the bias-dependent parameters such as I_{ds}. The ANNFET's excellent fit to the data is particularly significant because the model is based directly upon measured DC I-V data and uses

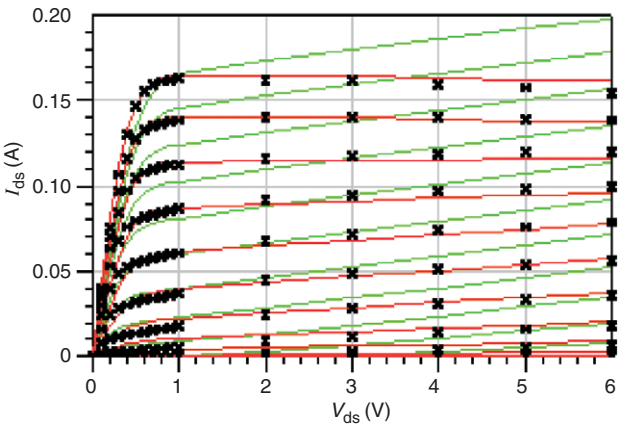


Figure 5. DC I-V comparison of the ANNFET model (red curves), Materka model (green curves), and measured 0.25 × 600 μm Triquint pHEMT data (black points) for -0.9 V < V_{gs} < 0.1 V in steps of 0.1 V. The ANNFET model provides an advantage as seen by the improved fit to the measured data.

embedded knowledge to accurately interpolate among (training) data points to achieve accurate results.

It is important for the designer to verify the model's static drain-source current along with its derivatives. The first-order derivative of the drain-source current with respect to the gate voltage is referred to as the transconductance G_m. Proper modeling of this parameter is required to accurately predict gain. The simulated and measured peak G_m are shown in Fig. 6 as a function of the gate control voltage. Given a sparse data set, the ANNFET model can obtain good agreement with the measured response.

Table 1 summarizes the rms error of the DC characteristics for the ANNFET and Materka nonlinear models. The rms error of the I_{ds} model corresponds to the entire area of device operation, i.e., knee and saturation, for V_{gs} values ranging from close to pinch-off to forward conduction, whereas the rms error of the drain-source current derivatives, G_m and G_d, are found over a range of V_{gs} and V_{ds} values, respectively, with the other voltage held constant. The rms error provides a quantitative measure of how well the model fits the data. Table 1 shows that, overall, the ANNFET model with the lower average rms error predicts the DC characteristics better than the industry-standard Materka model.

Table 1. Root-mean-square errors for the ANNFET and Materka models' DC parameters.

DC parameter	Units	ANNFET model rms error	Materka model rms error
I_{ds}	mA	3.3	16.8
G_m (@ V_{ds} = 1 V)	mS	14.8	49.4
G_d (@ I_{ds} = 60 mA)	mS	24.7	17.2
$\partial G_m/\partial V_{gs}$ (@ V_{ds} = 1 V)	mS/V	150.0	319.6
Average rms error		48.2	100.8

RF Model

A device's RF behavior is normally characterized by its S-parameters, which are measurements representing microwave signals along a transmission line and are generally a function of frequency and bias. For a two-port device, such as an FET, there are four S-parameters: S11 and S22 are the complex reflection coefficients, and S12 and S21 are the complex transmission coefficients. A device's S-parameters are normally measured as a function of frequency at fixed bias points and under small-signal conditions where the transistor exhibits linear characteristics.

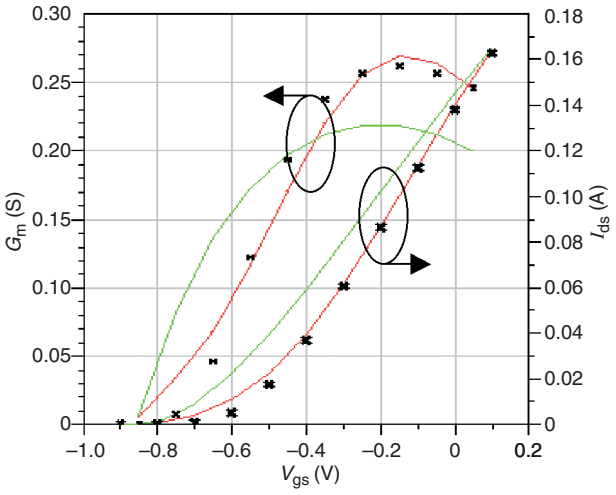


Figure 6. Transconductance and drain-source current comparison of the ANNFET model (red curves), Materka model (green curves), and measured data (black points) as a function of gate voltage at a drain voltage of 1 V. The accuracy of the ANNFET model is verified by the fit to the measured drain current and its derivative G_m.

Figure 7 illustrates the nonlinear models' S-parameter response compared to measured data for the 0.25 × 600 μm GaAs pHEMT. All data are shown in a complex plane format, where the magnitude of the response is indicated by the radial distance from the chart's center and the phase is indicated by the angular position about the center. The reflection parameters, S11 and S22, are plotted on a Smith Chart format, which has additional contours that indicate values of the real and imaginary parts ($\pm jX$) of the complex impedance. The perimeter of the Smith chart represents unit magnitude or complete reflection. The perimeter of the S21 transmission parameter represents a voltage gain of 6, and the perimeter of the S12 transmission parameter represents a voltage gain of 0.06.

Table 2 provides the magnitude of the rms vector difference between the model and measured S-parameters. The rms errors of the models correspond to a frequency range of 5–35 GHz at a bias of V_{ds} = 6 V and I_{ds} = 60 mA. To accurately predict an amplifier's performance, the model must provide a good fit to all four measured S-parameters. The ANNFET model with the lower average rms error has a better fit to the device's S-parameters compared to the Materka model.

Parameter extraction is a process of deriving equivalent-circuit elements from measured S-parameter data. The S-parameter performance of both models is based on the accuracy of extraction of the equivalent circuit elements (see the boxed insert figure) at a specified bias point.[23] If the extracted element values are not correct, the model will not be able to reproduce accurate S-parameters.[24] The higher rms errors for the S21 and S22 parameters of the Materka model are attributed to the model's inability to accurately characterize the dispersion in the output conductance G_d and transconductance G_m. Dispersion refers to the fact that the

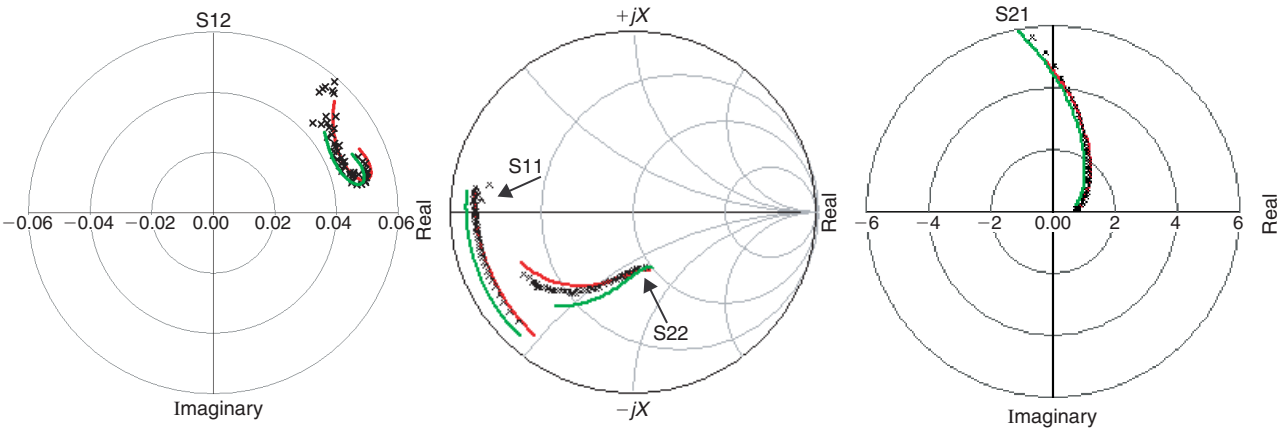


Figure 7. S-parameter comparison of the ANNFET model (red curves) to the industry-standard Materka model (green curves) and measured data (black points) for a bias of V_{ds} = 6 V and I_{ds} = 60 mA over a frequency range of 5–35 GHz.

Table 2. Vector difference rms errors for the ANNFET and Materka models' S-parameters.

Parameter	ANNFET model rms error × 1000	Materka model rms error × 1000
S11	56.9	61.4
S12	3.6	30.6
S21	79.4	236.9
S22	53.3	125.4
Average rms error	48.3	113.6

DC value of G_d and G_m is different than the RF value of G_d and G_m.

CONCLUSION

The state of the art in Ka-band PA technology has been significantly advanced by leveraging research efforts at APL and MSU. Neural network models that have been developed, such as the ANNFET, have demonstrated accuracy and flexibility for high-efficiency SSPAs and nonlinear applications. Using these models, we have established that the harmonically controlled termination technique promises significant improvement to the state of the art of efficiency for Ka-band SSPAs. With the development of the software tool and documentation, the microwave designer now has the capability to construct adaptable models directly through a standardized, streamlined, and documented process.

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APPENDIX: NEXUS—A NONLINEAR DEVICE MODELING TOOL

Nexus is an integrated model development toolkit, developed by MSU's COMSARE, that combines the main processes needed to develop a nonlinear FET model. Nexus aids designers in creating adaptable device models for high performance and accurate circuit designs. With Nexus, designers require less model development and implementation time and have the flexibility to create adaptable model topologies for improved circuit performance.[1] Nexus integrates all model development processes with a Modeling Process Protocol[2] that provides documentation of the procedures required to develop standard large-signal models for FETs and bipolar junction transistors. Nexus integrates the following processes.

Device characterization (DC and RF measurements)

Nexus requires import of measured data that consist of bias-dependent S-parameters over frequency and DC measurements of current/voltage characteristics.

Model topology definition

Nexus can generate customized equivalent circuit model topologies. The topology is derived from the specification of each element in the equivalent circuit model. The nonlinear elements can be denoted by analytical expressions, a neural network, or a discrete value.

Parameter extraction

Nexus can extract the linear and nonlinear elements of a general equivalent circuit FET model as a function of bias from measured S-parameter and DC data.

Parameter optimization

Once the nonlinear parameters (i.e., capacitance and current) have been determined as a function of bias, Nexus can be used to optimize the parameters via different neural network engines. The outputs of the optimization are the neural network–equivalent weight sets of the nonlinear parameters.

Circuit simulator integration

Nexus can export the device model into a commercially available CAD tool (i.e., Agilent's Advanced Design System). The model is translated into a user-defined equivalent circuit topology within the circuit simulator that characterizes the device's DC and RF behavior. The working executable model can be used in a circuit simulator environment. This is achieved by the dynamic generation and compilation of source code that links the parameter types, analytical or neural network, to user-defined model functions within the circuit simulator.

Model validation and testing

Nexus allows the user to visualize the model's simulated DC and RF performance through sophisticated plotting and graphing routines and to validate the model's performance with measurements. Individual parameters can be isolated and tested to determine the impact on the model's performance. Performance successes and limitations are embedded within the model's documentation.

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