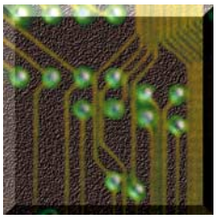

APL's Electronic Services at the Turn of the Century

Phillip F. Hider, E. Brian Alvarez, Jay R. Dettmer, Howard S. Feldmesser, A. Shaun Francomacaro, Karen L. Moore, and Scott E. Schlemmer

Electronic Services at APL range from an array of engineering, circuit, and packaging design capabilities, through hardware fabrication and assembly, to final inspection and test of a completed product. These products range from the very small to the very large, from space to submarine applications, and everything in between. The Laboratory's in-house Electronic Services are primarily provided by the Engineering, Design, and Fabrication activity (EDF) within the Technical Services Department. The bulk of EDF's electronic design and development activities resides within the Electronic Services Group. This article highlights technologies and trends in electronic services and capabilities necessary to meet APL customer requirements, both today and in the future. (Keywords: Electronics, Engineering, Microelectronics, Packaging, Substrate.)

INTRODUCTION

The long and successful history of Electronic Services provided by APL dates back more than 50 years to Van Allen and the Central Services Group.[1] Three groups in the Technical Services Department (TSD)—electronic design, electronic fabrication, and microelectronics—were merged in the early 1990s[2,3] to form the current Electronic Services Group (TSE). The Group, part of TSD's Engineering, Design, and Fabrication (EDF) activity, is carrying out the long APL tradition of innovative electronic products and services, ranging from the VT fuze of World War II to today's state-of-the-art electronic devices and packaging techniques.[4]

TSE comprises people with a wide diversity of skills and experience who are charged with taking an electrical product concept from any of the sponsored Laboratory departments and shepherding it through engineering, design, and fabrication to test and installation. This close and personal interaction between our Electronic Services personnel and the customer departments has saved our sponsors much time, effort, and money. It also enables rapid, onsite response to changes and problems as they develop, which has proven critical for many programs. TSE also works closely with the other major component of the EDF, the Mechanical Services Group (TSM), whose work is described elsewhere in this issue. TSM provides mechanical platforms for numerous spacecraft and miscellaneous parts for submarines, surface vessels, and aircraft.

Our electrical engineers can develop circuits from the chip level to full electronic systems, ranging from direct current (dc) to microwave frequencies. A team of electrical packaging engineers and designers, using the latest software and hardware, supports our circuit engineering team as well as electrical engineers

throughout APL. Packaging design professionals transform the circuit diagrams generated by electrical engineers into detailed manufacturing documentation for both onsite and offsite fabricators.

Within the board and substrate processing function, process engineers and chemists produce hardware devices ranging from sensors to large-area spaceflight-qualified circuit boards using their own specialized equipment and skills. The assembly function provides complete hardware assembly capabilities from microcircuits to entire spacecraft. Our own team of inspectors is responsible for electronic test and qualification to meet rigorous military and space certification requirements, and finally, our Metrology Office oversees the outsourcing of equipment calibration and maintenance for APL.

TSE provides a wide range of electrical/electronic services to APL in the areas noted above, i.e., system/circuit and electronic packaging engineering; board, substrate, and device fabrication; assembly; electronic test and qualification; and metrology (Table 1). Details of the products and services in each area are presented in the following sections, with the exception of metrology. (For further discussion of quality assurance and metrology, see Charles and Weiner, this issue.)

Table 1. Major Electronic Services capabilities.

Major area	Capabilities
System/circuit and electronic packaging engineering	Digital circuit engineering development Analog circuit engineering development RF and microwave engineering development Very large scale integration (VLSI) Thermal/stress analysis packaging design
Board, substrate, and device fabrication	Printed wiring boards (PWBs) (Mil Spec) Thick film substrates Thin film substrates Multichip modules (MCMs types L, C, and D) Microelectromechanical systems (MEMS) Chip-on-board (COB) Precious metal plating Precision chemical etching Laser machining Wafer dicing
Assembly	Wirebonding (wedge and ball) Semi-automated assembly Hand soldering to NASA Std-8739.3 Die attach COB MCMs to Mil-PRF-38534 Cables and harnesses Wirewrap
Electronic test and qualification	Automated substrate testing Inspection to military/NASA/IPC Society standards Environmental part screening
Metrology	Calibration and testing of APL standard equipment

SYSTEM/CIRCUIT AND ELECTRONIC PACKAGING ENGINEERING

System/Circuit Engineering

Products and Services

As a central electronic engineering resource for APL, our staff has an extensive range of expertise and experience. This enables us to function either as a primary design agent or an extension to an existing development team, where we take responsibility for all aspects of a project solution including major system and subsystem development. Because of the range of available services, we can provide help to customers at any stage of their development activity. However, we can be most efficient and cost-effective when we are involved during initial design considerations so that the project can take maximum advantage of our wide range of resources.

Specific engineering services include concept formulation, specification development, systems and circuit design, component selection, packaging design, design and fabrication oversight, embedded software development, bench testing, system integration and test, and field support. TSE also provides specialty engineering services: application-specific integrated circuit (ASIC) design; field-programmable gate array (FPGA) development; sensor and data acquisition systems development; low-power embedded systems design; biomedical systems development; and digital signal processing methods, tools, and processors.

Recently completed circuitry for the Digital Multibeam Steering (DIMUS) Project exemplifies our custom IC design capability, described elsewhere in this issue by Charles and Weiner. DIMUS (Fig. 1) is a computing engine for high-speed sonar beamforming

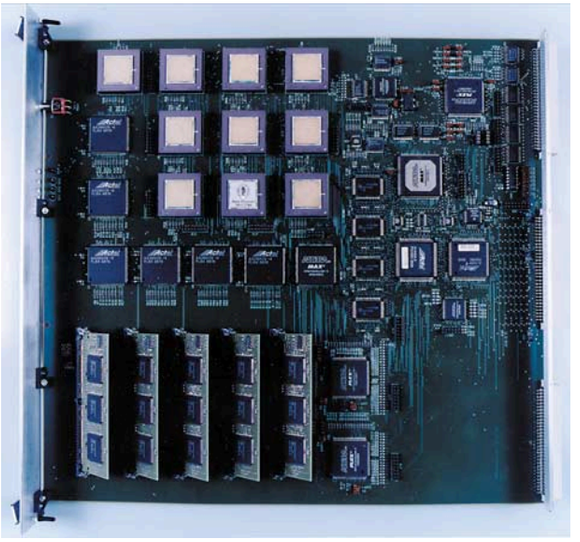

Figure 1. The Digital Multibeam Steering (DIMUS) board performs 59 billion operations per second.

designed to process signals from an array of 960 hydrophones. When operating at maximum speed, the DIMUS system computes 60 million beams per second, performing an estimated 59 billion operations per second.

Another unique, recently completed application is the Inter Ocular Pressure Monitor (Fig. 2). This wireless, remote sensor system sits on the surface of the eye to measure pressure variations inside the eye using a miniature capacitive pressure sensor and transmitter. Pressure changes are transmitted to a receiver near the eye, possibly on a pair of glasses. The sensor is undergoing development in our sensor processing facility.

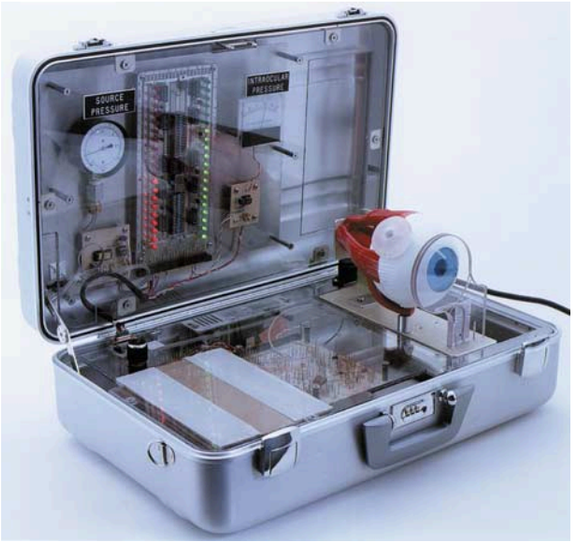

Figure 2. The Inter Ocular Pressure Monitor demo unit.

Evolution and Trends

APL engineering trends are similar to those occurring throughout the entire electronics industry. Our customers are seeking both higher levels of integration and capability and reduced power, size, and development time. This trend is resulting in systems of ever-increasing complexity and greater dependence on computer power for design, modeling, simulation, testing, and operation.

FPGAs are becoming a part of most engineering designs. Programmable gate arrays offer a high level of integration without incurring the traditionally large, nonrecurring engineering and fabrication costs of custom ASICs. The implementation of a custom ASIC design in a programmable gate array configuration allows the designer orders of magnitude savings over traditional ASIC design, development, and fabrication costs. State-of-the-art gate arrays are currently available with up to 1.1 million gates and are in-circuit programmable, greatly enhancing the ability to make changes rapidly. Laser-programmable techniques can produce prototype microcircuit chips for validation within a matter of days, dramatically reducing costs associated with development time.

The high costs of traditional ASIC fabrication have often been prohibitive for users who need only small quantities of devices. However, small-quantity custom device requirements have been made possible owing to the availability of proven university shareware tools and fabrication processes like MOSIS.[5] In addition, the use of hardware description languages such as VHDL[6] has proven to be of significant benefit. With the advances in programmable logic and "systems on a chip," we are approaching a time when hardware designs will be as programmable as the software that runs on them.

Electronic Packaging Engineering

The electronic packaging engineering and design function at APL uses sophisticated, computer-aided design (CAD) tools to translate engineering schematics into PWBs; substrate forms such as COB, MCM, and hybrids; thick/thin film structures; and MEMS. Technological advances have mandated the advancement of CAD tools. Artificially intelligent autorouters have greatly enhanced the productivity of engineering designers and enabled designs of ever-increasing complexity. We are developing means for the real-time thermal analysis of the packaging designs we undertake. Real-time thermal analysis becomes increasingly necessary as the designs become more complex, demanding greater power dissipation within smaller physical confines. For example, Fig. 3 shows three evolving packages that contain the same IC and provide the same circuit function. We can no longer afford to invest the time and effort to complete a packaging design only to find

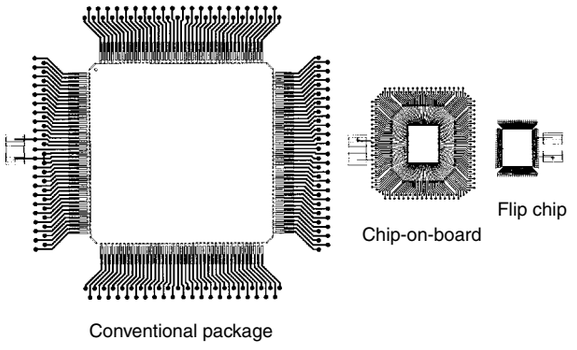

Figure 3. IC package evolution. These packages contain the same IC and provide the same circuit function.

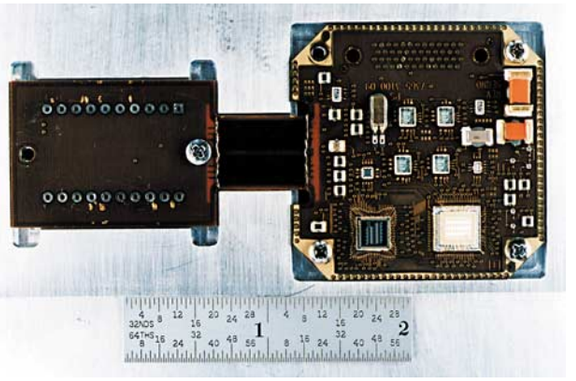

Figure 4. COB version of a solid-state imager for a 14:1 volume reduction.

that it lacks thermal or electrical interference integrity, forcing a packaging redesign effort. Also under investigation is the use of real-time cross talk and interference analysis.

Products and Services

To ensure that our designs are "correct by construction," we use an integrated set of Mentor Graphics CAD software for electronic packaging engineering and design. This means that the databases created for the design are sufficiently intelligent that information contained in them is passed from one tool to the next as the design proceeds. All parts of the packaging design process are linked together from the same source information, typically the schematic diagram.

We also use an extensive, evolving, centrally controlled software library of electronic components, which can be accessed through custom software menus. Each part has a graphic symbol and device outline drawing (geometry) associated with it that can be used by any compatible CAD tool during the design process. All of our library parts have been designed to be compatible throughout our fabrication and assembly processes.

A large number of our electronic packages are designed for space applications, dictating small size, low mass, and high integrity. An example of shrinking size is the processor board for a spacecraft command and data handling system which employs COB format and can literally fit in the palm of one's hand. Another example is a solid-state imager using packaged parts. (These surface-mounted parts already provide for considerably more shrinkage over similar devices with older package styles.) The imager required a volume of approximately 10 × 10 × 18 cm. A COB version was developed (Fig. 4), with increased image memory and a more sophisticated interface to the external electronics,[7] that only occupied 130 cm^3, a 14:1 volume improvement.

Not all of the requirements are for the very small. Two boards built for the Navy were at the opposite end of the size spectrum. One such PWB was a 24-layer motherboard, with 10,000 holes, measuring approximately 46 × 30 cm. and weighing 4 kg. Another was the 16-layer Triage board, with 400 parts and 6000 traces, operating at 200 MHz. The critical 20% of this board was manually routed to accommodate the requirements for the high-speed, emitter-coupled-logic circuitry. Manual routing significantly reduced the via count and critical path lengths. The remaining 80% of the less-critical circuitry was autorouted, resulting in a saving of approximately 100 design hours. The autorouter can be configured to obey the same design rules as for manual routing. It can run unattended, overnight or throughout weekends, enabling multiple iterations until acceptable track routing and component placement are achieved.

Evolution and Trends

High-speed PWBs and the fast switching speeds of the latest high-technology ICs produce elusive effects in digital designs, including cross talk, ringing, and overshoot. If these effects are not addressed at design inception, the entire architecture may fail to meet electrical specifications, even though all components are logically interconnected.

We are exploring the use of interconnect synthesis software tools that allow electrical engineers to minimize switching effects, meet timing requirements, and design PWBs that optimize IC performance. These tools promote "first-pass success" designs, helping engineers meet the short design cycles dictated by today's development environment.

The trend in electronic design today is again for higher levels of integration, lower power per gate, and shorter development cycles. The first two improvements are being achieved through the use of FPGAs and ASICs versus discrete logic; high-density packaging,

including surface-mount devices and chip scale packages (CSPs); and bare die as in COB. We are using blind and buried vias and micro laser vias to achieve ever-decreasing feature sizes for vias, pads, and traces. A blind via connects one or more internal layers of the device with only one outside surface. Buried vias are those internal connections that link one or more internal layers without connecting to either of the outside layers of the board or substrate. Micro laser vias are those connections generated by laser because classic, mechanical drills are too large to create the hole sizes necessitated by the emerging technology. These holes typically are below 250 μm in diameter.

To accomplish quick-turnaround development cycles for our customers, TSE staff are exploring new and innovative CAD tools. We have already spoken of the need for additional packaging design tools to reduce packaging design cycle time. We also need circuit/system design engineers to make increasing use of circuit and system emulators to verify design integrity before fabrication. Industry analysts at Collett International,[8] for example, estimated that in 1998, boards operating at speeds below 50 MHz represented only 34% of printed circuit board (PCB) designs, down from 57% in 1996. In contrast, boards running at 100 MHz accounted for 43% of all designs, compared with 19% of board designs just a few years ago.

BOARD, SUBSTRATE, AND DEVICE FABRICATION

Capabilities Overview

APL's board, substrate, and device fabrication area provides the highly complex platforms on which circuits and devices are assembled. This area can be divided into three broad categories of technology: organic laminates, thin film deposition technology, and thick film print and fire technology. Organic laminate substrate technology supports the fabrication of PCBs, laminate-based MCMs (MCM-L), and various controlled and matched-impedance circuits including transmission lines and antennae. Our thin film deposition technology enables the manufacture of MEMS, thin film–deposited MCMs (MCM-D), biomedical sensors, opto-electronic devices, monolithic microwave ICs (MMICs), and controlled and matched-impedance circuits as already noted. Thick film print and fire technology is employed to build multilayer substrates using low-temperature co-fired ceramic (LTCC) substrates or conventional thick films. Since each of these thick film techniques has ceramic technology as a base, these MCMs are called MCM-C.

A computer-aided manufacturing and photoplotting facility capable of translating design files into the physical artwork is used when building most of our boards and substrates. The emulsion photoplots are on Mylar-based material capable of resolving 50 μm feature sizes with a tolerance of 12.7 μm. The maximum dimensions of the photoplots are 30.5 × 45.7 cm, which coincides with the facility's panel size for organic substrates. Through process engineering we have developed many unique fabrication procedures that have directly supported our customers' programs and enabled us to continually improve on feature and substrate size. For MCM-L packages we routinely handle substrates of 20 × 20 cm, with lines of 127 μm and holes of 254 μm; MCM-C substrates are nominally 7.6 × 10.2 cm, with 50 μm lines and 154-μm holes; and MCM-D packages are typically produced on 15-cm substrates with feature sizes of 15-μm lines and 20-μm holes.

Organic Substrate Process Technology

A common factor that continues to guide our efforts with organic substrate technology is to increase packaging density and efficiency while maintaining our Mil-spec certifications. We have been building multilayer laminates since 1990. Indeed, APL's Electronic Services area is the only organization of its kind with certification to Mil-P-55110 for polyimide laminates since 1991, MCM laminate production since 1996, and certification to Mil-P-50884 for rigid-flex boards since 1997. These process technologies have been used to build spaceflight hardware for numerous programs. A case in point is the development of the MCM-L substrate fabrication process.[9] In 1996 and 1997, processes were developed for creating multilayer laminates with both blind and buried vias to maximize via density. A unique process was formulated for electroless, autocatalytic gold plating so that the metal on the board surface could be prepared for direct chip attach and subsequent wirebonding necessary when fabricating MCM-L substrates. The resultant technology was used to manufacture MCM-Ls for a miniature imager. This MCM-L board consists of 10 layers with blind and buried vias as small as 250 μm in diameter and conductor trace widths down to 127 μm.

Thin Film Deposition Technology

For over 40 years we have been using thin film technology to fabricate a wide variety of microelectronic devices.[2] This technology has enabled us to fabricate MCM-D circuits for military applications since 1995.[10] Since 1993, we have been developing MEMS for sensors[11] and materials research.[12] Our biosensor processing technology improved throughout the 1990s to enable the building of microfabricated glucose and pH sensors for the JHU Department of Biomedical Engineering. We have also established processes for constructing opto-electronic waveguides, switches, and

couplers in electro-optically active material.[13] Our microplating techniques have advanced to include electroless plating of nickel with varying phosphorous content as well as wirebondable gold.

Working with APL's Sensor Sciences Group (RSS) and the Army Research Laboratory, we have been developing MEMS-based sensors for a variety of applications. Miniature magnetometers previously developed by RSS have been further reduced in size and weight through a combination of surface and bulk micromachining techniques. Made of polycrystalline silicon, these devices have potential applications in magnetic field detection and imaging as well as location, attitude, and motion sensing. A photomicrograph of the latest polycrystalline silicon MEMS magnetometer is shown in Fig. 5.

In another application of thin film technology, a telecommunications module was built using our MCM-D technology for an external customer. The circuit contains over 1000 electrical nodes with more than 160 I/O connections and over 1200 internal wirebonds. The MCM-D substrate consists of six layers with feature sizes as small as 20 μm.

Thick Film Print and Fire Technology

A long-time stalwart in packaging technology, thick film processing has taken on new applications at APL. Spaceflight-certified thick film substrates have been manufactured for more than 15 years. Our efforts to develop state-of-the-art processing capabilities led to work with LTCC. We have been building spaceflight-certified LTCC MCM substrates since 1990. Through the years, the technology was modified to accommodate smaller feature sizes, increased layer count, cutouts and cavities, and advanced metallizations for wirebonding, soldering, and brazing.[14] In 1997 a process was created for integrating laser-trimmed resistors into our multilayer thick film substrate. This new technology was used to fabricate interconnection substrates in support of NASA/Goddard's Space Infrared Telescope Facility Program. The substrates (Fig. 6) consist of 16 screen-printed layers with features as small as 100 μm.

Evolution and Trends

The past has provided a solid foundation on which to build future capabilities. Organic substrate technology is continually evolving. Efforts are under way to create processes for reducing the size of features such as via holes, conductor traces, and the spaces between conductors down to 76 μm. The purchase of a laser drilling device to help achieve these dimensions is planned. The added packaging density will accommodate the ever-increasing I/O pads on IC die in the future. We are experimenting with processes that can be used to create heat sinks, which are integral to the laminate board. We are also investigating a sequential build-up technology that will capitalize on the advantages of blind vias and thin dielectric layers and will also improve the overlay accuracy. New processes are being developed using dielectric materials such as Teflon-based substrates to meet the requirements of high-speed circuitry. Many of these techniques will be used to build hardware for future space programs such as CONTOUR and MESSENGER. These efforts should ensure that our soft laminate technology remains state of the art long after the year 2000. For example, Table 2 captures this trend for PWB design rules into 2005.

In our MEMS development work, efforts are under way to further improve the sensitivity of magnetometer

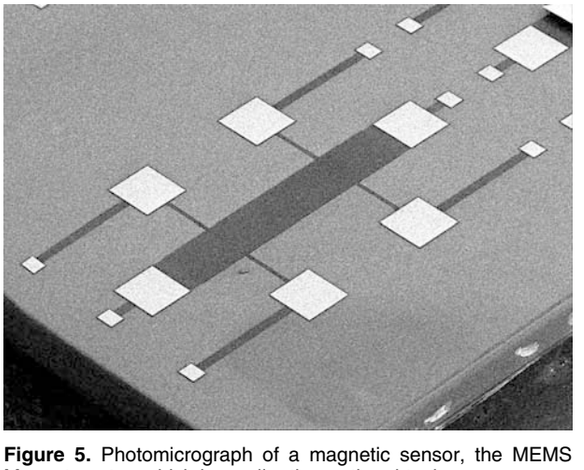

Figure 5. Photomicrograph of a magnetic sensor, the MEMS Magnetometer, which is smaller than a thumbtack.

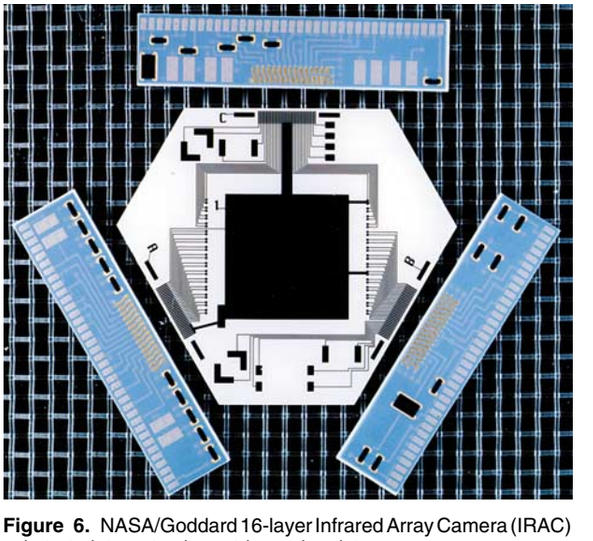

Figure 6. NASA/Goddard 16-layer Infrared Array Camera (IRAC) substrate integrates laser-trimmed resistors.

devices using thin film piezoelectric materials, with the ultimate goal of packaging a three-axis magnetometer in a volume of approximately 16 cm^3. Piezoelectric thin films and micromachining techniques will also be used to develop MEMS-based high-pressure sensors for artillery-launched munitions as part of the Army's Hardened Subminiature Telemetry and Sensor System. Essential to the development of devices such as these is a thorough understanding of the mechanical properties of the thin film materials used in MEMS. We have been a leader in the fabrication of thin film test structures such as diaphragms and miniature tensile test specimens. Current work extends these fabrication methods to other MEMS materials (e.g., piezoelectric films, new epoxy-based polymers).

The many development efforts in thin film technology show our breadth of capabilities. Processes are being developed to integrate passive components such as resistors, capacitors, and inductors into MCM-D substrates to free up more surface area for active devices. Polymer dielectric materials are being created that display the electro-optical effect and can be used subsequently in an MCM-D for laser-based electrical testing, or in opto-electronics as waveguides, couplers, and switches. Microplating techniques are being developed that are compatible with features as small as 50 μm. We are developing tin/lead and indium bump-plating processes to support flip chip assembly techniques and experimenting with hardware plating processes for advanced materials such as magnesium and titanium. Thin film technology within the board, substrate, and device fabrication function is becoming increasingly important to a range of APL products and services and will continually be improved to keep pace with demands.

Currently we are developing an MCM-C process using photo-imageable thick film conductor and dielectric pastes. This technology will enable feature sizes down to 50 μm for vias, traces, and the spaces in between. The conductors display superior edge profiles that help to limit RF transmission losses. We are also developing processes that include surface and buried passive circuit elements.

Table 2. PWB design rules.

Design parameter	Current standard (in./μm)	Current advanced (in./μm)	Year 2005 (in./μm)
Via diameter	0.015/380	0.010/254	0.004/100
Via cover pad	0.040/1016	0.025/635	0.010/254
Line width/space	0.008/203	0.005/127	0.003/76

ASSEMBLY

Within our wide spectrum of services are wire wrap for breadboard circuits, hybrid circuit assembly, wirebonding, flip chip bonding, PCB assembly (both spaceflight- and nonspaceflight-qualified), cables and harnesses, ground support equipment, electronic racks for military applications, and site installations, all requiring limited field support. Boards, modules, devices, cables, and subsystems have been produced for a wide variety of Laboratory sponsors—NASA, Army, Air Force, and Navy (both surface and submarine)—and have required our assembly expertise, not only at APL but also in the field during installation and follow-on test and operations.

Products and Services

Board-Level Assembly

Our spaceflight-qualified personnel have developed the ability to hand solder to NASA Std-8739.3. This is particularly important when required quantities are small and hand soldering is the only viable method to produce the desired product. Typically, the front-end cost for automated soldering runs with high-precision space-qualified devices is sufficiently expensive that small-quantity lots become prohibitively expensive. This has driven our capability for precision hand soldering with selective automation as schedule and cost permit.

When appropriate, mass solder reflow can be used. Hand soldering is limited in its ability to place very fine-featured, high-interconnect-quantity devices required in some applications. For these we use paste dispensers and semi-automated pick-and-place machinery to obtain the precision placement of fine-featured devices. Mass reflow soldering is then used to complete the soldering task.

We must also be adept at handling the many different IC packaging styles. Although the technology is changing, we fully expect that the fine-pitch-leaded packages we have today will remain in use for many more years. These packages have I/O counts ranging from 84 to 256 and up, and lead pitches (center-to-center spacing) down to 508 μm, which are expected to go to 406 and 305 μm.

Instead of decreasing lead pitch, parts with very high I/O density will dispense with leads altogether. Ball grid arrays (BGAs) and CSPs will become commonplace since they use the area beneath the part for the connections. This area consists of an array of solder balls, each approximately 0.066 cm^3, known as bumps, which are used for the device interconnections. A CSP is generally defined as any device housing whose footprint and perimeter are, respectively, $\leq$1.5 and $\leq$1.2 times that of the die. A CSP uses a header or interposer to

connect the die to the substrate, thus differentiating it from a direct die attach device such as BGA or flip chip.[15] Bonding wires are connected between the IC and the interposer, and the IC is sealed with a hermetic coating commonly known as "glob topped." The underside of the interposer has an array of pads that will eventually be soldered to the circuit board that contains the rest of the circuitry. BGAs and CSPs may have I/O counts up to several hundred.[16]

Both BGA and flip chip product technologies share a serious drawback, i.e., the small size of the IC bonding pads (Fig. 7) makes it almost impossible to create the temporary contacts necessary to test the functionality of the IC before it is packaged. Since no IC manufacturer has been able to achieve a 100% yield, this poses serious problems for low-volume manufacturers who must ensure that every part works as intended before shipping. (Large-volume manufacturers absorb the failures in warranty costs.) Many, including some of the high-volume assemblers, resort to CSPs to package their ICs since they take up very little more area on the circuit board than the IC itself. However, the area necessary for connecting a machine that tests the IC has been significantly increased. Thus, the entire bottom of the chip is used for connection points. Testing becomes relatively simple and adds little to the cost of the bare die. The advanced capabilities for making substrates have also allowed advances in assembly.[17] We can now mount ICs directly to the circuit board using COB technology, eliminating the package entirely.

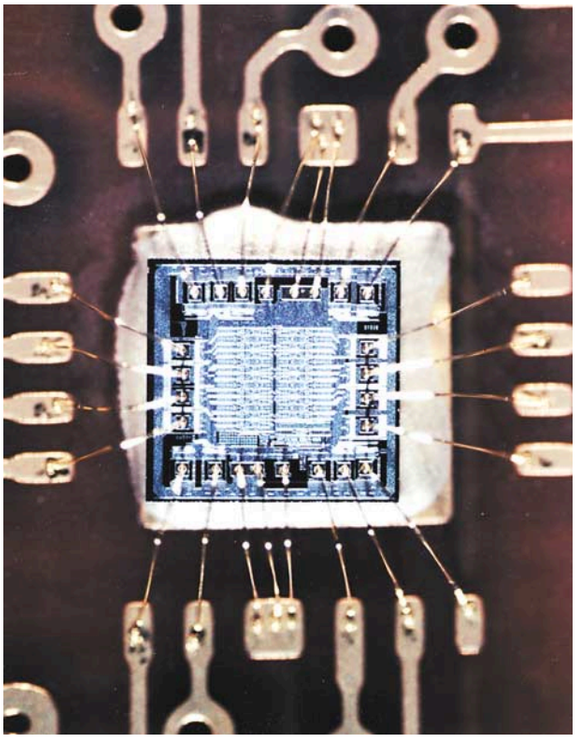

Figure 7. IC chip showing bonds and pads. Their small size makes testing difficult.

We are developing the tools and techniques to ensure that the final assembly has the reliability of a hermetically sealed part. To fully utilize COB, environmentally resistant boards are necessary. We use tarnish-resistant gold over the copper traces, which enhances the wire bonds connecting the IC to the trace. Glob-topped materials that protect the IC itself and the interconnecting wires must go on efficiently and must not in themselves induce stresses in the silicon of the IC, the delicate interconnecting wires, or the diffusion bonds. The entire board is then coated with Parylene.

Component Assembly

The assembly function includes extensive hybrid and MCM assembly, which takes advantage of our expertise with conductive pastes and our many interconnection techniques. Our conventional hybrid function has enabled us to produce any device so far requested. We can assemble, electrically test, and hermetically seal the devices. Typically, semi-automatic and/or automatic wirebonding techniques are used for conventional hybrid circuits. An example of TSE's hybrid capability is the five-channel, very low noise amplifier built for Goddard Space Flight Center, which was part of the Cassini space mission.

The MCM assembly functions include MCM-C and MCM-D capability. Our level of expertise ranges from the development and design of the support frames for the delicate substrates we use to the development of the gold surfaces to which we bond. We work with a selection of wire bonders (manual and automatic, ball and wedge). Gold and aluminum wires typically range from 18 to 25 μm, depending on the method of construction and circuit requirements. To enable bonding to the exotic materials being used as detectors, we must continually develop new techniques. Recently we produced a sensing device made of cadmium/zinc/telluride to which we successfully made 22,000 bonds. Figure 8 shows an MCM-D with wirebonded ICs.

Cable and Harness Assembly

Many complete wiring harnesses have been developed and fabricated for the various APL-produced spacecraft, inlcuding ACE, NEAR, and TIMED. The typical wiring harness of the past was formed on a 1:1 mockup of the spacecraft. The cable harness for the MSX spacecraft weighed a nominal 227 kg, although more typical harnesses weigh 45–90 kg. Effort is being made to further reduce the cable mass. Completed spaceflight cable harnesses are baked to drive out any

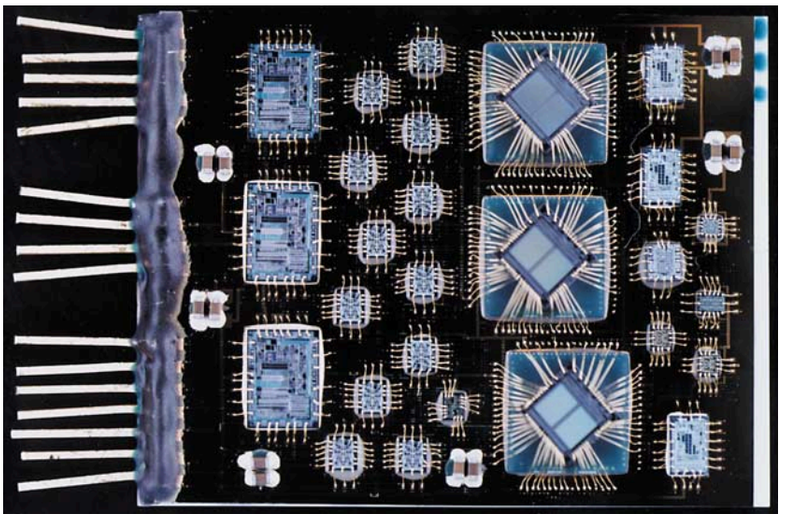

Figure 8. Army Research Laboratory–hardened subminiature telemetry sensor system with wirebonded ICs.

contaminants before their clean room installation on the spacecraft. When necessary, precision semi-rigid coaxial cables are applied to the spacecraft. There is an increasing trend (e.g., as in the TIMED Program) to use rigid-flex cables to simplify the cableforms within a card cage. Owing to circuit complexity and component density constraints in a confined volume, a series of rigid-flex PWB pairs was adopted. Each board pair used a common, central, metallic heat sink, with half of the pair of rigid-flex boards attached to each side of the metallic heat sink, and the common flex connector wrapped around one end. This provided maximum component density in the minimum volume, together with adequate thermal conduction for spaceflight application (Fig. 9). Ground-based systems are beginning to incorporate fiber-optic interconnections, a trend that will increase for space applications as familiarity with and reliability of fiber optics in a space environment grow.

Coating and Encapsulation

The Electronic Services assembly function also has its own coating and encapsulation capability that is an essential part of the technologies just described. The function provides the ability to conformally coat PWBs for protection against foreign matter, which may cause reliability problems during circuit operation. High-reliability programs require conformally coated PWBs as a part of their quality assurance plan to prevent moisture absorption, shorts caused by external conductive particles after the PWBs are built, and contamination by human body salts on plastic-encapsulated microcircuits (PEMs). Detailed process procedures have been developed for each material used and serve as operational steps in the coating process. Many components mounted on PWBs require a thermally conductive path to a heat sink.

We can also encapsulate electronic assemblies using Parylene. This material, which is a dimer, is heated and then deposited on the coating surface in a vacuum chamber. It has been used for high-frequency circuits and more recently for nonhermetic components such as COB and PEMs. Future development plans are to use this material in advanced miniature circuits, biomedical applications, and microwave circuits.

Evolution and Trends

Assembly services provided to APL in the near term are not expected to differ greatly from those offered today. Customer demand will dictate that we continue to build microcircuits and assemblies on PWBs. As some technologies gain the ability to be generated with short turnaround times, some of the usual breadboarding techniques and other legacy services now required by our customer, such as vector board and wire wrap, will disappear. As these services become less significant to the customer, decisions will have to be made as to whether they should be discontinued along with the concomitant training, floor space, and maintenance costs. The uses of rack-and-panel assembly are also likely to decrease as boardless

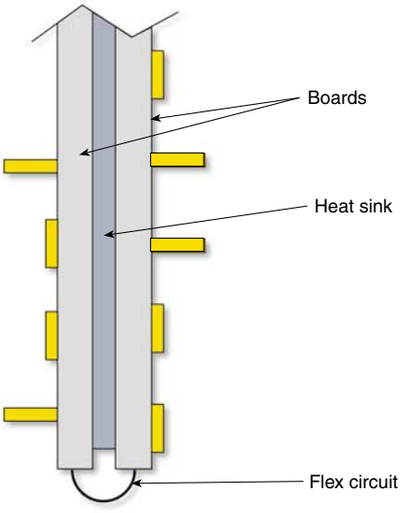

Figure 9. Cross-sectional diagram of centrally heat-sinked rigid-flex boards for space environments showing components on each side.

backplane structures come to the fore and connector technology improves. Clearly, assemblies will be smaller and denser, requiring new tooling for assembly and inspection.

The lead pitch of surface-mount components will probably not decrease further since the ability of commercial parts handling tools to pick up and place them and the soldering tools to attach them seem to have reached their limits. For us, however, the handling of ultrafine pitch parts must become routine. Humans are not generally capable of efficiently transferring parts with lead wires as small as 100 μm on 300-μm centers from a holder to a circuit assembly without causing damage. Most of the machinery available for such work is adapted only for significant volumes of repetitive work. This clearly presents a challenge. However, we have a tradition of overcoming such problems with elegant solutions. No doubt, we will find or build tooling that provides the mechanical assistance necessary for limited-quantity builds within budgetary constraints.

One further advance that will see prominence in the new millennium is flip chip,[18] which was discussed previously. In addition to removing the package to save volume, flip chip removes the need for wire bonds by inverting the IC chip and soldering the IC's connection pads to the circuit board underneath them. Alternatively, a conductive epoxy may be used to make the connections between the IC and the circuit board. We have purchased an evaporation system to help develop our skills with adding or increasing the size of the underside pads or bumping. Customer requirements now include the development of indium bumping for devices to be used at cryogenic temperatures.

ELECTRONIC TEST AND QUALIFICATION

Our trained staff has extensive onsite resources for component and system testing.[19] Class 1,000, 10,000, and 100,000 clean rooms are available to test components and systems that we engineer as is equipment to handle a variety of testing requirements including MIL-STD-883 for microelectronics and MIL-STD-202 for components. We also perform design verification testing including the design and fabrication of test fixtures, simulators, and stimulators. Having the responsibility for APL's Metrology Office ensures that we are meeting program requirements for equipment calibration and verification. Further details of the test and qualification process are presented in the article by Charles and Weiner, this issue.

SUMMARY

APL's Electronic Services will continue to perform both the routine and specific tasks required by our customers on a day-to-day basis. We will also look ahead to anticipate the future technological requirements of our customers and to hire suitable personnel, evolve the technologies, and obtain the equipment needed to stay one step ahead of customer demands. To that end, we strive to maintain close contact with our customers. Development projects are undertaken to steer us in the direction that we believe will satisfy the future needs of our customers. These tasks will sometimes be on a risk-sharing basis with a partner who wishes to develop the same or similar techniques. We will continue to develop external customers where such a step is considered to be to APL's benefit. A more diversified customer base would help to generate a more stable financial platform and to provide an improved cross-pollination of ideas. Electronic Services will continually strive to perform its part in supporting APL's unique ability to be a one-stop location for total problem solving.

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