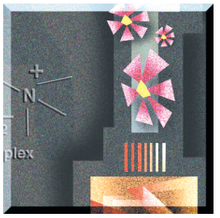


A Low-Cost Miniaturized Scientific Imager Design with Chip-on-Board Technology for Space Applications

Binh Q. Le, Paul D. Schwartz, Sharon X. Ling, Kim Strohbehn, Keith Peacock, Philip J. McNally, S. John Lehtonen, Robert E. Gold, and Robert E. Jenkins

The Miniaturized Scientific Imager uses a reflective telescope, a single filter, and a charge-coupled device detector. This visible imager has a 1.5 × 2° field of view, a focal length of 720 mm, and a spatial resolution of ≈4 m at a range of 500 km. Heaters and radiators control the detector temperature. In this design, the user can control exposure mode, duration, and frame buffer selections. Thirty-two internal frame buffers will store the images captured by the imager. Our goal is to demonstrate and qualify a miniaturized, modularized, smart imager for future space missions. In this article, we present the detailed design of the imager, with emphasis on APL's chip-on-board technology and its significant impact on system weight and volume reduction. The development resulted in an imager design that weighs only 0.5 kg with a low power consumption of 1 W. A similar imager in the Near Earth Asteroid Rendezvous spacecraft weighs 7.7 kg and consumes 6.9 W. (Keywords: 3-D packaging, Charge-coupled device, Chip-on-board, Miniaturized imager, Reflective telescope.)

INTRODUCTION

The imager is among the most powerful tools for many space missions. It can determine the existence, size, spectral and morphologic characteristics, and orbit of any natural satellite.[1] For planetary missions, reflectance spectroscopy at visible and into near-infrared wavelengths (0.4–1.1 μm) can provide important geological identification of a planet's surface. For deep space missions that investigate the shape of the universe, galaxy evolution, evolution of stars, and the life cycle of matter in the universe, an imager with wavelengths in the visible and into the far-infrared (0.5–20.0 μm) is required. The NASA directive for future space programs such as the Sun–Earth connection technology roadmap[2] emphasizes lower cost as well as the innovative design and implementation of lightweight spacecraft and miniaturized instruments.

The APL Miniaturized Scientific Imager (MSI; Fig. 1), which was originally designed for the Glacier Program,[3] combines several leading-edge technologies into a compact, lightweight, and low-cost unit that has many applications when incorporated with a variety of charge-coupled device (CCD) arrays. The MSI is a CCD-based, narrow field-of-view visible imager with a lightweight reflective telescope, high-density

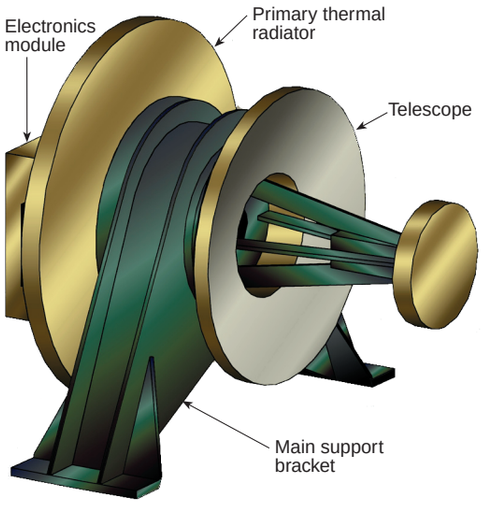


Figure 1. The Miniaturized Scientific Imager (weight = 0.5 kg, power = 1 W, size = 15 × 14 × 13.5 cm).

solid-state memory, and miniaturized chip-on-board (COB) electronics. The detector is the Thomson TH7866[4] with an image dimension of 244 rows × 512 columns and a pixel size of 27 × 16 μm. The telescope is a compact Ritchey-Chretien design[5] with reflective diamond-turned and post-polished mirrors. A similar version of this telescope has been used previously in the Laser Range Finder of the Near Earth Asteroid Rendezvous (NEAR) spacecraft.[6,7]

The MSI electronics design employs miniaturized COB technology wherein bare dies are directly mounted on laminated printed wiring boards without the need for the component's package. Eliminating the package reduces the required board area and assembly weight. Using conventional low-cost printed wiring boards and standard wire bonding, COB technology can yield a factor of at least 10 in weight and volume savings.[8,9] COB technology also reduces the number of interconnect levels between an active die and the substrate (i.e., the package pins). The elimination of the first level of packaging not only reduces the thermal resistance of the system, but also reduces the parasitic impedance of the circuit interconnects.

MSI DESIGN

The MSI has an overall dimension of 15 × 14 × 13.5 cm and weighs 0.5 kg. It consists of the Ritchey-Chretien telescope, a main support bracket, two thermal radiators, and a CCD detector within the electronics module. The design includes a flexible, highly integrated camera with a miniaturized electronics module mounted directly onto the optical system. This configuration can be easily modified or customized for specific mission science objectives. The approach, i.e., reusing essentially the same electronics with minimal modifications, spreads development costs over several missions and results in lower risk, a shorter schedule, and lower costs for a given mission.

In the current MSI design, internal baffles (rather than the external Sun baffles normally used in other imagers) are mounted directly onto the MSI mirror support structure to minimize stray light. For other missions, an external Sun baffle that completely protects both the primary and secondary mirrors of the telescope can easily be added to the existing design. The MSI has been developed with the specifications and requirements listed in Table 1 to meet a variety of planetary space missions.

Electronics Design

The MSI electronics consist of three 5 × 5 cm electronics boards (Fig. 2) which are described in the following paragraphs.

Imager Electronics Board

In the MSI design, the miniature electronics can be easily configured to accommodate a variety of commercially available CCDs for maximum scientific flexibility. The current imager board (Fig. 3) is based on the passively cooled 244 × 550 pixel TH7866 CCD used in the NEAR imager.[1] All of the digital electronics are implemented in a field-programmable gate array (FPGA) that can be customized for a particular instrument. The sequencer interprets data processing unit commands and generates appropriate timing for the CCD clocks and analog-to-digital (A/D) conversion. In addition, the sequencer formats the pixel data into a serial data stream.

We pursued miniaturization of the MSI electronics with a dual strategy. First, we used advanced COB technology in the packaging design to achieve the smallest electronics board for a given design. Second, we integrated as many functions as possible into application-specific integrated circuits (ASICs) to reduce parts count and complexity. The integration of the digital electronics into an FPGA is a clean and practical approach for a flexible instrument. In addition, we implemented a CCD analog interface ASIC that accepts a capacitively coupled CCD output voltage swing as input and converts it to a 12-bit digital output for the digital sequencer. The analog interface integrates an auto-zeroed, low-noise preamplifier; a correlated double sampler; and a pipelined, redundant-signed digital, algorithmic, 12-bit A/D converter on a single ASIC. The input voltage swing is programmable by an external resistor, and conversion speed, power, and noise performance can be traded off with an external resistor and capacitor. At a conversion rate of 100 kpixels/s, we measured an rms noise of about

Table 1. Specifications for the APL MSI.

Requirement	Specification
Power	1W (operating mode); 0.5 W (sleep mode)
Sensor	Thomson Si CCD TH7866
Image format	244 rows × 512 columns
Image size	1,449,136 bits
Exposure control	Automatic or manual
Exposure time	5.70 to 1.38 ms
Thermal readout noise	≤1 least significant bit
Quantization	12 bits
Pixel size	27 × 16 μm
Image storage capability	32
Field of view	1.5 × 2°
Focal length	720 mm
Resolution	7 arc-sec (35 μrad)
Attitude stability requirement	100 μrad (0.006°) for ≤10 ms
Drift	≤2 mr/s
Pointing error	≤0.20°
Maximum satellite spin rate	1 revolution/5 min
Random vibration level	14.1 grms (0.16 g^2/Hz maximum)
Design limit loads	25 *g* axial 15 *g* lateral
Sine burst	32 *g* at 35 Hz axial 20 *g* at 28 Hz lateral
Shock	500 *g* at 500–10,000 Hz
Stiffness	≥100 Hz
Maximum venting rate	≤0.069 bar/s
Power requirements	5 V DC/ 15 V DC
Temperature range	
Storage	−55 to +85°C
Operating/sleep mode	−30 to +60°C
In calibration range	−30 to 0°C

110 electrons at the output of the A/D. The sequencer FPGA provides the analog interface A/D and auto-zero logic-level timing signals. For this ASIC, we intentionally enlarged the bond pads to allow testing of the die before final assembly.

As with most CCD detectors, the TH7866 requires bias and clock-voltage levels that are not compatible with digital-oriented CMOS (complementary metal-oxide semiconductor) processes. In place of an ASIC, we chose commercially available clock drivers and discrete devices that are available as dies and are compatible with the COB technology.

Power conditioning, while achieving reduced power consumption, is the most difficult aspect of a CCD-based camera. The existing miniature camera electronics use 7.2 mA at 15 V and 69 mA at 5 V, which is comparable to the existing NEAR imager design. The camera uses less than 0.5 W of power and regulates its internal 10-V supplies; it also produces a 19-V bias. Although a single power supply would be preferable to a dual-power supply design with both 5 and 15 V, we found that miniature DC/DC converters were too noisy, and regulating down from 15 to 5 V would significantly increase power consumption. Simpler power conditioning is probably not consistent with most CCD detector arrays; however, advanced COB technology makes the use of discrete conditioning parts a practical alternative.[10]

CCD pixel voltage swings are AC-coupled into the chip, and 12-bit digital data are provided to the camera's data-formatting and control-sequencer FPGA. This chip operates at the same voltage (5 down to 3.3 V) as the digital logic circuitry on the camera board and is compatible with a variety of CCD chips because the transconductance and current reference are adjustable with off-chip resistors.

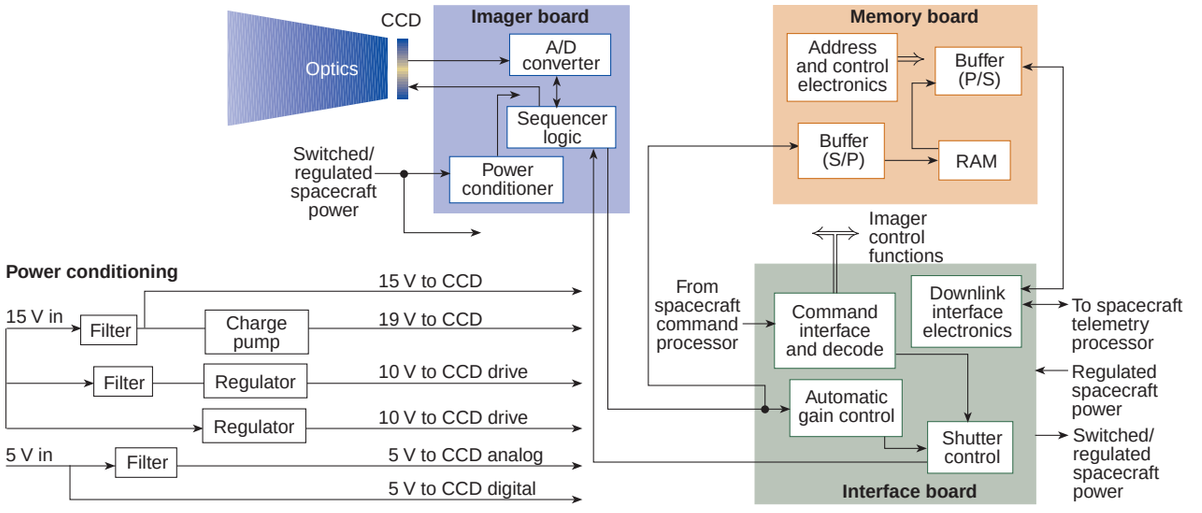


Figure 2. Block diagram of the MSI system (P = parallel, S = serial).

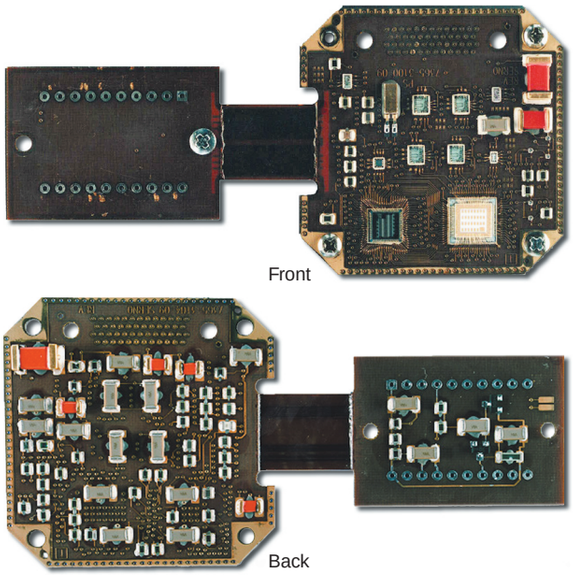


Figure 3. The imager board (5 cm across; detector not shown).

Interface Electronics Board

The MSI captures and stores an image in 1 of 32 defined memory locations upon receiving a command from the spacecraft. It then downlinks the selected/recorded images over its interface with the spacecraft data system upon the appropriate command. The imager electronics generates 1.5-Mbit images every 2 s and stores them in dedicated instrument memory. Uplink command messages decoded on the input/output (I/O) board store images in defined memory locations, downlink images from selected memory locations, control the operating mode of the imager, and directly set the shutter exposure time. Gate array–based logic on the I/O board (Fig. 4) implements an automatic gain control mode that can be activated by ground command to override the selected shutter speed and permit the imager to autonomously select the appropriate shutter setting. Other I/O board logic is used to gather and format imager diagnostic data that can be downlinked upon request.

Memory Board

On the memory board (Fig. 5), state machine logic generates the address information and control signals necessary to store and downlink selected images. Memory board logic also generates the required signals to continuously refresh the image in the dynamic random-access memory (DRAM). All memory board functions are implemented in two Actel-1020 FPGAs.

The MSI is equipped with a low-power sleep mode to help improve spacecraft energy balance conditions. Stored images are retained on the memory board while it is operating in the sleep mode. The MSI powers up in the sleep mode and can be commanded into or out of that mode at any time. The imager requires approximately 1 W of power in the operating mode and 0.5 W in the sleep mode. When the imager is placed in the low-power sleep mode, all stored images are maintained, but record and downlink functions are inhibited.

Optical Design

The MSI uses a reflective optical arrangement (Fig. 6). In a reflective optical system, light is manipulated by a layer of silver or aluminum that is less than 1 wavelength thick. Thus the optics is virtually weightless. A mechanical support structure (i.e., the mirror) is necessary to hold the surface in position to a very high accuracy, about 0.1 wavelength. Since the area of the mirror is dictated by mission science requirements, minimizing its thickness is the only way to reduce the weight of the system. Conventional wisdom for a reflecting telescope suggests that the thickness of a mirror for an astronomical telescope should be 10 to 15% of the mirror diameter There are two reasons for this thickness: (1) it is necessary to avoid distortions during polishing, and (2) it is needed for structural rigidity.

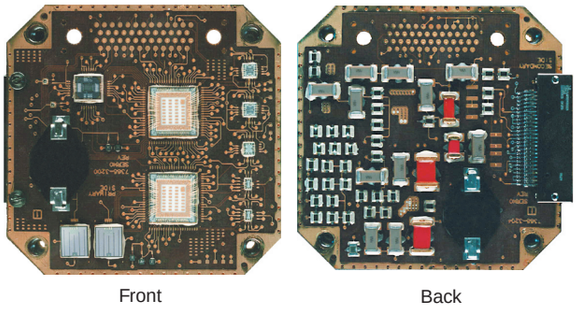


Figure 4. The input/output board (5 cm across).

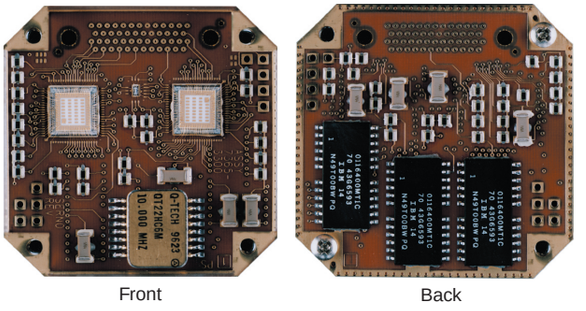


Figure 5. The memory board (5 cm across).

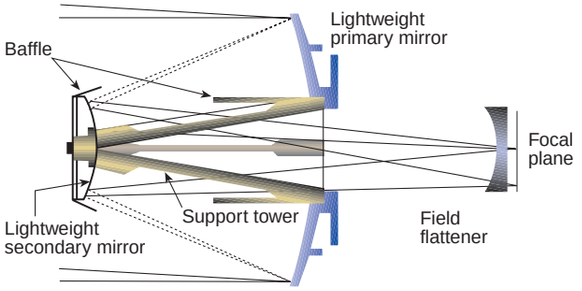


Figure 6. The MSI optical design.

The customary approach to reducing the bulk of a mirror is to machine or cast a honeycomb of cavities on the back. The Hubble Space Telescope's primary mirror consisted of a rectangular honeycomb with 2.54-cm-thick faceplates on the front and back. This allowed a lightweight structure 30.5 cm thick with a 305-cm diameter. Astronomical telescopes are generally designed to achieve resolutions far greater than imagers used in planetary studies. Their spatial resolution is usually about 0.1 arc-sec. For a planetary imager with a focal length of 1 m and a CCD detector with 25-μm pixels, a resolution of 2 to 3 arc-sec is adequate.

The Ritchey-Chretien telescope (Fig. 7) includes a primary mirror, a support tower, a secondary mirror, and two internal baffles. The support tower is of single-piece construction with four webs extending from the central base area of the primary mirror to provide support for the secondary mirror, including the two internal baffles. This support structure has a high stiffness-to-weight ratio and is one of the key features of this lightweight optic design. The support area is in the shadow of the central obscuration, so no additional energy is lost. For the current mission, two baffles were added to the support tower to eliminate unwanted entry of off-axis light. This approach reduces the overall weight of the system since it eliminates the need for an external baffle to protect the entire telescope as in the conventional optical design. The support tower and the two internal baffles are coated with a black anodized coating to eliminate unwanted reflections. The telescope also features a flexural design with a thin cross-sectional wall at the support base to eliminate thermal distortion caused by the thermal expansion mismatch between the mirror and the main support structure. The focal length of the telescope is 720 mm, and the rms diameter of the ray trace spots is less than 10 μm, which is considerably smaller than the pixels on the detector.

The complete telescope assembly is made of aluminum alloy 606-T651. Optical surfaces are diamond-turned, post-polished, and plated with electroless nickel and silver to achieve optimum reflectance in the 400- to 1000-nm range. The aluminum alloy was selected for the MSI telescope because of limited funding.

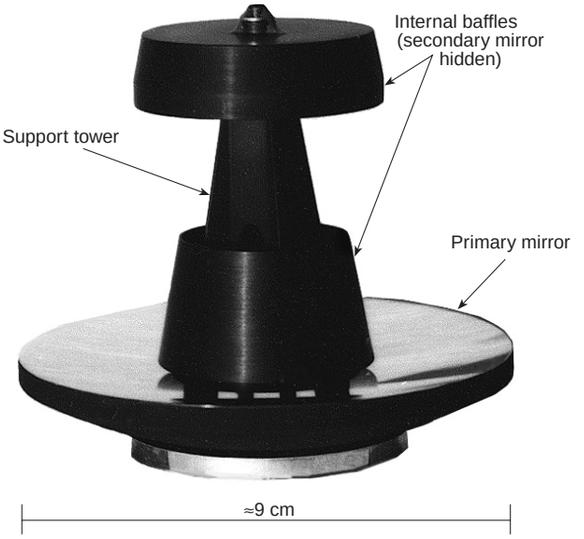


Figure 7. Telescope assembly in the MSI design (photograph courtesy of OCA Applied Optics, Garden Grove, CA).

A lightweight mirror design can be accomplished with a low-density material such as beryllium, whose density is about 70% that of aluminum. In advanced mirror designs, beryllium or silicon carbide materials, whose specific stiffnesses (16.4 and 12.2 $\times$ 10^4 N-m/g) are higher than that of aluminum (2.54 $\times$ 10^4 N-m/g), are preferable.[11] A more rigid material tends to resists deformation caused by the manufacturing process and by vibrations. Designing a lightweight telescope with advanced materials is beyond the scope of this project. However, an additional weight saving of 30 to 40% can be achieved easily by using beryllium.

Mechanical Design

Electronic Packaging

The electronics module, which contains all the necessary circuits for the MSI, has an overall dimension of 5 $\times$ 5 $\times$ 2 cm and weighs 150 g. It contains the three circuit boards discussed previously. Each board is mounted on an Irridite-coated aluminum frame that also serves as an assembly fixture during integration and assembly of the unit. Custom-designed fuzz button connectors with a pin-to-pin spacing of 500 μm provide interconnection between the boards (Fig. 8). This three-dimensional modular packaging design is the key to providing flexibility for future reconfigurations of the imager.

Fuzz button connector technology was first developed by Robert Smolley at TRW in the 1980s.[12] The buttons consist of a continuous length of gold-plated beryllium copper or molybdenum wire randomly woven into a cylindrical shape. They are populated into a

molded insulator housing or a thin layer of dielectric material to form a connector with an array of spring-loaded electrical contacts. The connector, when compressed between two boards with patterns matching those of the buttons, provides the interconnection between the boards. Since electrical connections depend solely on the ability to maintain the contact pressure between the boards and the connector, board deflections caused by manufacturing processes or vibration loads during launch (including the thermal set of the spring material) must be carefully considered during the design phase.

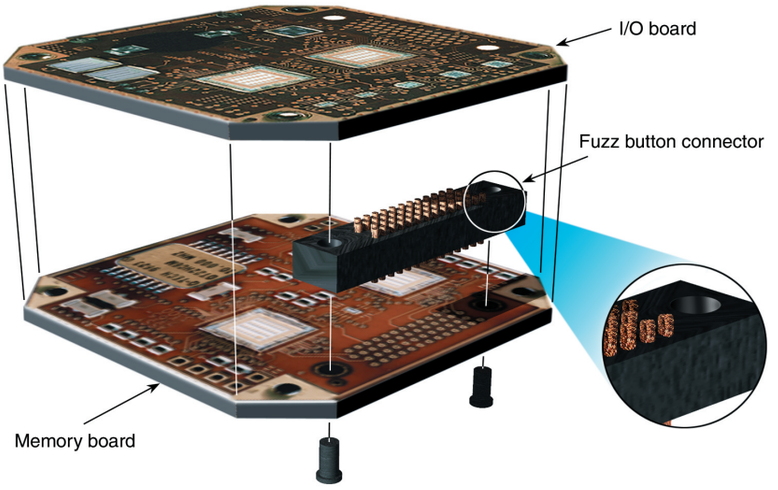


Figure 8. Fuzz button connector.

Figure 9 is a schematic of the assembled electronics module. The rigid-flex imager board has a CCD detector mounted on a heat sink directly coupled to the primary thermal radiator. The other two boards are multilayer rigid boards. To achieve a high-density packaging design, active and passive components are mounted on both sides of the boards. Each board consists of eight layers of interconnections with 127 × 127 μm line width and spacing, including blind vias. All three board are made of copper-clad polyimide laminate material with an autocatalytic plating of bondable gold to support wire bonding and solder assembly.[13]

APL's COB technology[10] is used throughout the MSI design. It permits the utilization of conventional surface-mounted packages and bare dies and, most importantly, it provides reworkability. Yield enhancement improvement can be as high as 400% when rework is considered.[14]

The mixed interconnect technology feature is a significant benefit of COB design in developing the low-cost MSI. More than 90% of the active components in this design are available in die form. The only packaged parts are the DRAMs, the oscillator, and the CCD detector. In COB assemblies, connections between bare dies and the circuit board are made by thermosonic wire bonding, which is a well-matured standard process. Machines exist that have high levels of control for the parameters of force, ultrasonic energy, and heat to form reliable bonds using 25-μm-dia. gold wire. Previous APL studies[15–18] have successfully proven that bare dies can be protected from corrosive environments by applying an epoxy encapsulant on the tops of the dies after wire bonding and then parylene-coating the entire assembly.

Because of the complexity of the board and fabrication yields, the COB process must be reworkable. Since the epoxy encapsulant is applied only to the top of the dies, a defective die can be easily removed and replaced. The board design also includes sufficiently sized wire bonding pads to accommodate additional bonding attempts if rework is required. Epoxy coatings allow the entire electronic packaging scheme to be smaller, lighter, and much lower in cost than an equivalent hermetic system. Hermeticity requires metal or ceramic housings and custom feedthroughs. In addition, it is difficult to reseal a large hermetic module, and often the entire module must be discarded if any internal component fails.

During the development of the MSI, we also devised a low-cost technique to individually test non–known good dies (KGD) before final assembly and have used it to test the Actel-1020 FPGAs. The APL approach is to add an adapter substrate bonded on the top side of the die. All connections from the die are brought to this top-layer substrate. The adapter substrate and die are then assembled and temporarily wire bonded into a package to support die burn-in, programming, and testing. After completion of this test, the now KGD, together with the adapter substrate, is removed from the temporary package and is mounted to the final assembly (Fig. 10).

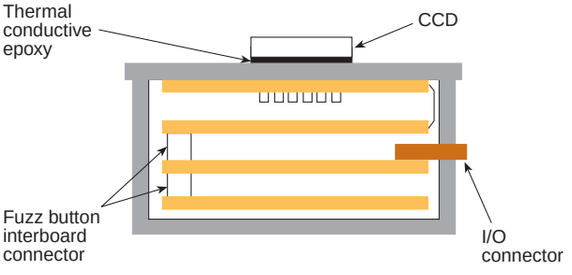


Figure 9. MSI electronics module design.

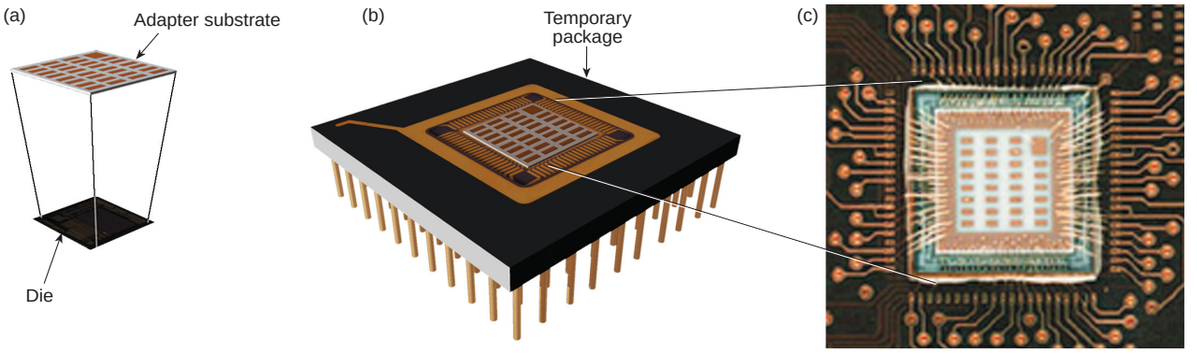


Figure 10. The APL design process for testing non–known good die. (a) Assemble adapter substrate on bare die. (b) Assemble part to be tested in temporary package. (c) Remove tested part and assemble it on board.

Structural Design

The goal of the imager structural design is to develop, wherever possible, the lightest structure to meet the launch and mission requirements. Cost-effective and lightweight materials such as aluminum alloy 6061-T6 and magnesium alloy ZK60A-T5 are used where appropriate. The primary structure, which includes a stiff, machined magnesium main support bracket, supports the optical telescope and the electronics module. The MSI was analyzed for the launch environment both in terms of strength and stiffness. Strength analysis was also performed based on the specified quasi-static load of 25 *g* in each of the three mutually orthogonal axes of the instrument. The stresses on the telescope were maintained below the micro-yield level to ensure optical alignment. In addition, normal mode analysis was performed to verify that the natural frequencies of the MSI did not couple with the launch vehicle dynamics. The first structural mode was found to be 302 Hz (Fig. 11), well above the specified 100 Hz.

Thermal Design

The MSI design uses simple passive thermal control techniques. Heat transfers from the CCD and the support electronics couple directly to deep space via two thermal radiators: (1) the primary radiator, which is a circular plate on which the electronics module is mounted, and (2) the secondary radiator, which is the top surface of the electronics module. The former is a thin-machined plate made from aluminum alloy 6061-T651. Its size is calculated to maintain the maximum operating temperature of the CCD to below 0°C. Figure 12 plots the average CCD temperature versus the radius of the radiator when the imager is fully powered up. To maintain the sub-zero temperature required for the CCD detector, the MSI thermal design uses a passive radiator with a 6.4-cm radius, which keeps the detector below −15°C.

Similar parametric studies have been performed for the "cold" imager—for example, when it is in sleep mode with a reduced power of 0.5 W—to aid in the design of the survival heater. Both thermal radiators were covered with indium-tin-oxide–coated silverized Teflon. To minimize the thermal couplings between the MSI and the spacecraft itself, the imager's external surfaces were covered with a multilayer insulator thermal blanket. Additional thermal insulator washers and titanium hardware were also used at the mounting feet of the unit to further insulate the MSI from the spacecraft.

Figure 13 provides details of the thermal design of the MSI. This approach minimizes heater power and weight while maintaining MSI temperatures within its desired operating range. An orbital analysis and a finite-element thermal analysis have also been performed using PCITAS and COSMOS software. Analysis results have indicated that all electronic devices operate below their maximum junction temperature limits. Figure 14 illustrates the temperature distribution of the imager, interface, and memory boards.

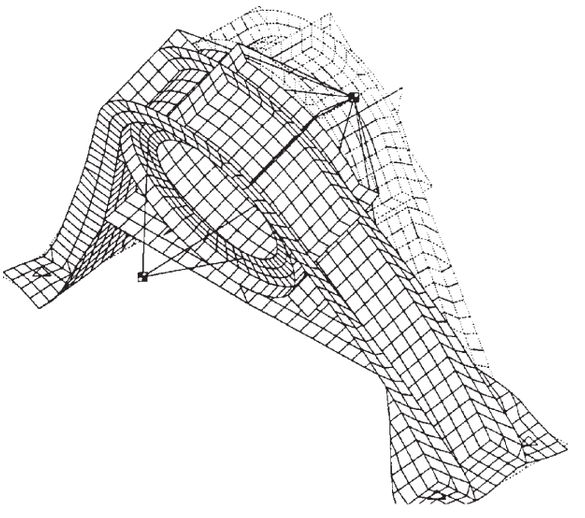


Figure 11. First mode response of the main support bracket at 302 Hz.

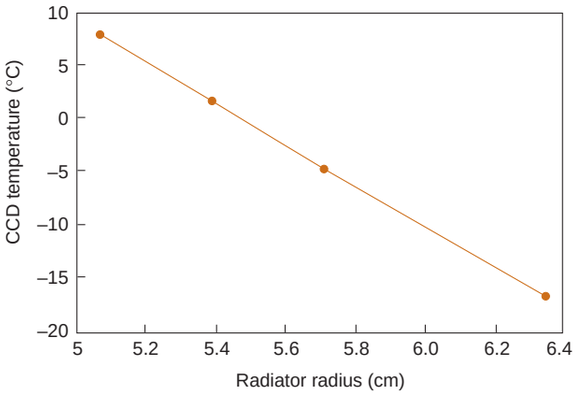


Figure 12. CCD detector temperature versus radiator size: hot case.

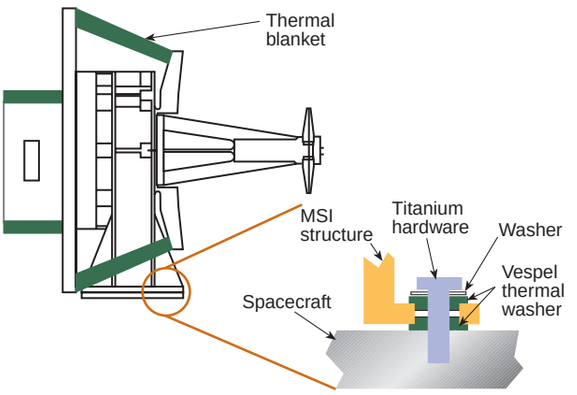


Figure 13. MSI thermal design, with an expanded view of the detailed mounting.

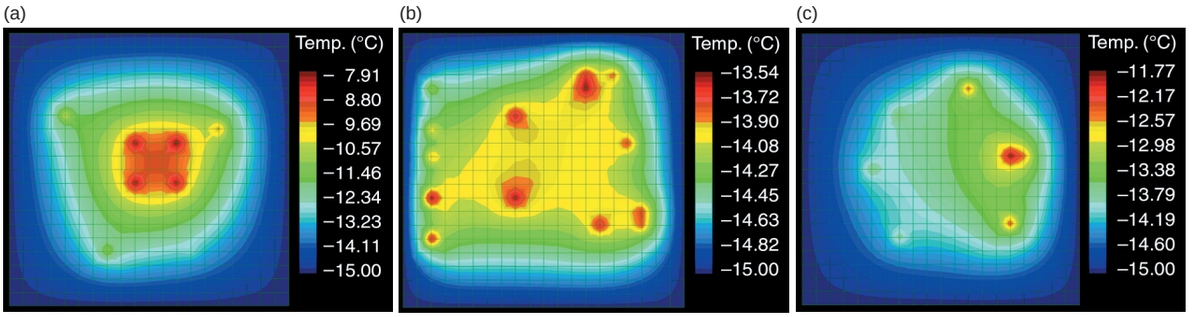


Figure 14. Temperature distribution on the (a) imager board, (b) I/O board, and (c) memory board.

SUMMARY

The MSI design adopts a flexible, modular approach where all subassemblies can be reconfigured to meet future specific space applications. In this design, we have achieved a high integration level of the detector and its support electronics using custom ASIC and advanced COB technology. COB technology allows low-cost designs since it uses conventional manufacturing processes that support both bare dies and packaged devices. It significantly reduces the weight and volume of the MSI electronics module. The result is a single miniaturized unit directly mounted on the telescope, eliminating the need for multiple units as used in standard designs. Although the MSI does not have the exact function as the NEAR Multi-Spectral Imager, we have demonstrated that a reduction of the instrument weight from 7.7 to 0.5 kg is feasible. Reference 10 (Fig. 8) provides a comparison between the MSI design with COB technology and the NEAR Multi-Spectral Imager design with surface-mounted devices. The integration and test of the MSI is in progress.

REFERENCES

[1]Hawkins, S. E. III, Darlington, H. E., Murchie, S. L., Peacock, K., Harris, T. J., et al., "Multi-Spectral Imager on the Near Earth Asteroid Rendezvous Mission," *Space Sci. Rev.* **82**, 31–100 (1997).

[2]*Sun–Earth Connection Roadmap*, NASA, available at http://umbra.nascom.nasa.gov/spd/secr/index.html (accessed 29 Jan 1999).

[3]Hoffman, E. J., *Minutes of Glacier Imager Preliminary Design Review*, SDO-10620, JHU/APL, Laurel, MD (Jan 1996).

[4]*Area Array CCD Image Sensor Data*, Thomson product information (1989).

[5]O'Shea, D. C., *Elements of Modern Optical Design*, John Wiley & Sons, New York (1985).

[6]Cole, T. D., Boies, M. T., El-Dinary, A. S., Reiter, R. A., Rodriguez, D. E., et al., "Laser Range Finder for the (NEAR) Near Earth Asteroid Rendezvous Mission," in *Proc. European Symp. on Satellite Remote Sensing (SPIE), Lidar Techniques for Remote Sensing II*, Vol. 2581, pp. 2–26 (1995).

[7]Le, B. Q., Cole, T. D., Rodriguez, D. E., Reiter, R. A., Moore, R. C., et al., "The NEAR Laser Range Finder Light-Weight Packaging Design," in *Proc. Int. Symp. on Optical Science, Engineering, and Instrumentation*, *SPIE*, Vol. 2811, pp. 208–216 (1996).

[8]Cherukuni, N., Liao, J. M., Denuit, R. V., and Kawano, K., "A Pentium Processor Based L/D MCM Test Vehicle: A Subsystem for Portable Applications," in *Proc. Int. Conf. on Multichip Module, IMAPS*, pp. 1–5 (1996).

[9]Le, B. Q., Nhan, E., Maurer, R. H., Lew, A. L., and Lander, J., *Chip-on-Board Technology 1996 Year-End Report*, SDO 10748, JHU/APL, Laurel, MD (Nov 1996).

[10]Le, B. Q., Nhan, E., Maurer, R. H., Jenkins, R. E., Lew, A. L., et al., "Miniaturization of Space Electronics with Chip-on-Board Technology," *Johns Hopkins APL Tech. Dig.* **20**(1), 50–61 (1999).

[11]Yoder, P. R., *Opto-Mechanical Systems Design*, Marcel Decker, Inc., New York (1986).

[12]*Button Board: The Short-Cut Connector*, TRW product literature (1986).

[13]Charles, H. K., Jr., Mach, K. J., Edwards, R. L., Letonen, S. J., and Lee, D. M., "Wirebonding on Various Multichip Module Substrates and Metallurgies," in *Proc. 47th IEEE Electronic Components and Technology Conf.*, pp. 670–675 (1997).

[14]Charles, Jr., H. K., "APL's Packaging Future: The Next Few Years," *Johns Hopkins APL Tech. Dig.* **20**(1), 101–110 (1999).

[15]Le, B. Q., Nhan, E., Maurer, R. H., Lew, A. L., Lander, J., et al., "Evaluation of Die Coating Materials for Chip-on-Board Technology Insertion in Spaceborne Applications," in *Proc. 6th Int. Conf. on Multichip Modules, IMAPS*, pp. 142–147 (Apr 1997).

[16]Nhan, E., Le, B. Q., Maurer, R. H., Lew, A. L., Lander, J., et al., "Reliability Study of Chip-on-Board Technology for Space Applications with a 3-D

Stacked DRAM as Test Vehicle," *Adv. Electron. Packag.* **1**, 1679–1684 (Jun 1997).
[17]Le, B. Q., Darrin, M. A., and Kadesch, J., "Study of Conformal Coating on Chip-on-Board Technology for Space Applications," *NASA IEEE Links* **3**(2), 2–5 (1997).
[18]Maurer, R. H., Le, B. Q., Nhan, E., Lew, A. L., and Darrin, M. A., "Fabrication and Qualification of Coated Chip-on-Board Technology for Miniaturized Space Systems," in *Proc. Third ESA Electronic Components Conf.*, pp. 199–204 (Apr 1997).

ACKNOWLEDGMENTS: The authors gratefully acknowledge A. Lew, E. Hoffman, T. Sholar, E. Nhan, and R. McEntire of the Space Department, without whose help and supports the development described in this article would not have been possible. We also would like to extend our thanks to H. Charles, Jr., J. Dettmer, J. Davis, J. O'Donnell, D. Lee, J. Folkerts, A. Dietrich, and other members of the Technical Services Department for their valuable contributions during the design and manufacture of the MSI.

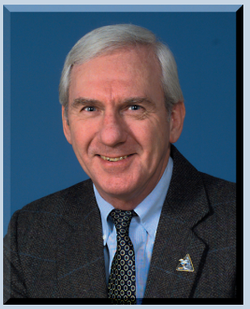
THE AUTHORS

BINH Q. LE is a member of APL's Principal Professional Staff. He received his B.A. in mathematics from the Université de Paris Sud, France, in 1976, and a B.S.M.E. and M.S.M.E., both from The Catholic University of America, in 1978 and 1980, respectively. Prior to coming to APL, he spent 13 years in structural and thermal analyses, electronic packaging design, and mechanical design for the nuclear and space industries. Mr. Le joined the APL Space Department in 1991 and is currently an electronics packaging engineer in the Electronic Systems Group. He is a member of IMAPS (The Microelectronics and Packaging Society) and Tau Beta Pi. Mr. Le has been the lead electronic packaging engineer for MSX, ACE, and NEAR. He is currently the Principal Investigator for COB technology to miniaturize spacecraft electronics and the lead packaging engineer for the MSI and the C&DH IYP. He has published over 30 papers in the electronic packaging field, holds 1 patent, and has submitted several patent disclosures. His e-mail address is binh.le@jhuapl.edu.

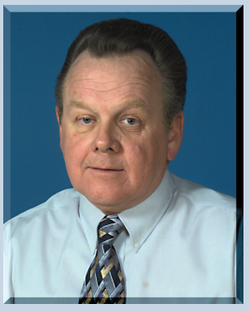
PAUL D. SCHWARTZ received B.S. and M.Eng. degrees in electrical engineering from Cornell University. Since joining the APL Space Department in 1973, he has been the lead design engineer for the development of numerous spacecraft subsystems including the AMPTE Command System, the COBE Momentum Management Assembly, and the MSX Data Handling System. Mr. Schwartz was the lead hardware design engineer for the NEAR Command Telemetry Processor. He has designed power-conditioning electronics for several space instruments including the Galileo EPD and the Ulysses LAN Experiment. He is currently the system engineer for efforts to develop a miniaturized visible imager and spacecraft. Mr. Schwartz holds one patent and has submitted several patent disclosures. His e-mail address is paul.schwartz@jhuapl.edu.

SHARON X. LING received an M.S. degree in mechanical engineering from Drexel University in 1990 and a Ph.D. degree in mechanical engineering from the CALCE Electric Product and System Center at the University of Maryland in 1997. She has been a member of APL's Senior Professional Staff in the Electric System Group of the Space Department since joining the Laboratory in 1997. Dr. Ling is the lead engineer for the structural and thermal analyses of the COB designed for the C&DH IYP and the PBeX projects. She has many publications in the area of electronic packaging as well as one patent disclosure. Her professional interests include reliability assessment of miniaturized space electronics, advanced interconnection methods, and other innovative technologies applicable to reliable, miniaturized space instruments. Her e-mail address is sharon.ling@jhuapl.edu.

KIM STROHBEHN received a Ph.D. in electrical engineering from Iowa State University in 1979. He is currently a Principal Professional Staff engineer in APL's Space Instrumentation Group. His primary interest is mixed signal analog/digital VLSI design with an emphasis on advanced astronomical instrumentation. His e-mail address is kim.strohbehn@jhuapl.edu.



KEITH PEACOCK received a B.Sc. from Durham University in 1961, an M.Sc. in radioactivity from Birmingham University in 1962, a Ph.D. in astronomy from Manchester University in 1967, and an M.S. in technical management from JHU in 1984. Before coming to APL in 1979, he worked at Bendix Aerospace Systems Division and Los Alamos National Laboratory. He has worked in the APL Space Science Instrumentation Group for 12 years. Dr. Peacock received two Lawrence Hafstad fellowships to pursue optical design projects in JHU's Department of Physics and Astronomy. His primary field of interest is optics; he designed the five MSX UVISI spectrographs, the Special Sensor Ultraviolet Imager, the Global Ultraviolet Imager, the Near-Infrared Spectrometer, and the TIDI telescopes. Dr. Peacock also teaches optics at JHU's G. W. C. Whiting School of Engineering. His e-mail address is keith.peacock@jhuapl.edu.



PHILIP J. McNALLY received a B.S. degree in physics from St. Francis College in 1959 and pursued graduate studies at Pennsylvania State University and Northeastern University. Before joining APL in 1991, he worked at COMSAT Laboratories, Honeywell, and Ion Physics Corp., conducting research on the ion implantation of semiconductors and developing silicon and gallium-arsenide microwave device technology. Mr. McNally is currently a member of the Microwave and Subsystems Section of the Radar Systems Development Group engaged in advanced semiconductor technology. He has published numerous technical articles on semiconductor materials and devices and has two patents. His e-mail address is philip.mcnally@jhuapl.edu.

S. JOHN LEHTONEN received a B.S. in electrical engineering from Florida Atlantic University in 1985. He is a Senior Staff engineer with the Electronic Services Group at APL, where he is involved with advanced microelectronics packaging technology development. Before joining APL in 1991, he worked at Solitron Devices, Inc., as a project engineer for hybrid microcircuits being made for the AMRAAM and HARM missile programs. His current interests include high-reliability assembly process development for multichip modules, COB, flip chip packaging technology development, and indium bump bonding for use in X-ray detectors in spacecraft instrumentation. Mr. Lehtonen has worked for 15 years in the microelectronics field and is a member of IMAPS (The Microelectronics and Packaging Society). His e-mail address is s.lehtonen@jhuapl.edu.

ROBERT E. GOLD received a Ph.D. in physics from the University of Denver in 1972. He is a physicist specializing in remote sensing, planetary composition, and heliospheric structure. He serves as assistant supervisor of the APL Space Engineering and Technology Branch and the payload manager for the NEAR mission. Dr. Gold was the project scientist for the Delta Star remote-sensing spacecraft and is an investigator with the HI-SCALE instrument on the Ulysses mission that has recently made the first observations over the poles of the Sun. He is the co-investigator for the Geotail EPIC instrument and the lead investigator for both ULEIS and EPAM instruments on the ACE spacecraft. His e-mail address is robert.gold@jhuapl.edu.

ROBERT E. JENKINS received a B.S. degree in engineering and an M.S. degree in physics from the University of Maryland in 1965. He is a lecturer in the JHU School of Engineering and a Principal Professional Staff engineer at APL. He is also a member of the Program Committee for the Part-Time Master's Degree Program in Electrical Engineering at Hopkins. Mr. Jenkins joined APL in 1961 and is currently Assistant Supervisor of the Space Department's Engineering Branch and Program Manager for the Space Department's advanced technology programs. He has over 25 years of experience in space systems. His e-mail address is robert.jenkins@jhuapl.edu.