History of Electronic Packaging at APL: From the VT Fuze to the NEAR Spacecraft

G. Donald Wagner

Electronic packaging has played a major role in the success of systems developed by the Applied Physics Laboratory. This article briefly chronicles some selected and often unique examples of APL's electronic packages over its 56-year history. The early APL electronic packages were needed for the famous VT fuze of World War II; in that case, four vacuum tubes and the ancillary electronics in the nose of an artillery shell had to be packaged. This presented a challenge: to develop miniaturized parts and techniques capable of withstanding the gun launch in a broad range of military environments and to ensure the highest degree of reliability. Further improved packaging techniques were employed as APL engineers designed devices for high-altitude research instruments, guided missiles, satellite and spacecraft instruments, underwater instruments, shipboard communications and radar systems, and biomedical devices. Technology changes progressing from vacuum tubes, transistor circuits, and simple integrated circuits to modern, very large scale integrated circuits that influenced APL's electronic packages are described.
(Keywords: Electronic packaging, Hybrid packaging, Integrated circuit packaging, Miniaturization, Multichip modules, Printed wiring.)

INTRODUCTION

APL has a long and rich history of successful developments in electronic packaging. At its inception, the Laboratory's success with the proximity fuze was due to our ability to engineer, design, and package fuze electronics within the confines of an artillery shell capable of withstanding the artillery launch environment. Although this early package consisted merely of a few vacuum tubes, a handful of resistors and capacitors, an antenna, a battery, and hundreds of mechanical components, it represented a remarkable accomplishment in electronic packaging. Present-day APL electronic package designs contain thousands of integrated circuits (ICs), thousands of resistors and capacitors, and many other miscellaneous discrete components such as transistors, diodes, relays, transformers, connectors, etc. The ICs themselves often include as many as 20 million semiconductor devices (transistors or diodes) within a single chip.

The VT fuze accomplishment was especially significant since, at the time, electronic packaging had not yet developed as an engineering discipline. This effort was the culmination of a team of electrical engineers,

physicists, mechanical engineers, metallurgists, manufacturing engineers, and scientists working together for a solution to a critical World War II problem. Since the early 1940s, we have progressed from packaging a few active circuits in the nose of an artillery shell to placing more than 118 complex circuit boards in the Near Earth Asteroid Rendezvous (NEAR) spacecraft, where each board often contains millions of active circuits. The actual packaging density has been increased more than 1 million times during the intervening 56 years.

VT FUZE

The success of the VT fuze is well documented in World War II history.[1] It represents an early APL effort to create better, faster, cheaper, and smaller electronic packages.

At the start, the problem of devising circuits to detect the proximity of objects was fairly simple. The challenge was to make circuits small enough to be contained in a projectile and rugged enough to withstand firing from a gun. The development of miniature, rugged vacuum tubes was considered to be the most difficult problem.[2]

The environmental requirements for the fuze dictated many of the package constraints. The design had to withstand a launch environment of up to 20,000 G due to linear forces, occasional larger side slap forces in the gun barrel, and centrifugal forces due to spin rates of up to 400 revolutions per second. Temperature, humidity, and atmospheric pressure changes experienced in an airborne, shipboard, or battlefield environment were of concern as well. APL engineers worked feverishly under wartime pressures with many contractors (e.g., Hytron, Raytheon, RCA, Western Electric, Sylvania, and Bell Laboratories) to develop vacuum tubes that were sufficiently rugged and reliable to meet the fuze requirements.

APL, working with the National Carbon Company, developed batteries known as “reserve cells.” These batteries used an electrolyte stored in a glass container (ampule). The shock of the gun firing would shatter the ampule, and the shell spin would distribute the electrolyte uniformly throughout the battery plates. The batteries, with zinc plates on one side and carbon plates on the other, became active in about 0.1 s and functioned throughout the typical 2-min flight. They had to supply three voltages for the tubes: 1.5 V for the filament, 97 V for the plate, and 7.5 V for the grid bias.

The electronic circuitry, which consisted typically of 4 vacuum tubes, 11 resistors, 8 capacitors, 2 inductors, and an antenna, was packaged in a cordwood hand-wired style. Parts were packed vertically in a cylindrical shape on a socket/pin header that was hand soldered and wired into the nose cone. A special custom-made cylindrical capacitor surrounded the electronics and provided the charge for detonation. This capacitor used a vinyl carbazole–treated cellophane dielectric film to achieve the required capacitance. Special care was given to the vacuum tubes, which were protected with a rubber casing that further isolated them from vibration and avoided microphonics.

Other mechanical components like safety devices that were activated from shell spin or launch acceleration were also built into the package. Materials such as newly developed plastics had an important role in the success of the VT fuzes since the sensor nose cone needed to be radio-wave transparent.[3] Encapsulation of the package was accomplished using a microcrystalline wax in a pressure cooker to ensure full encapsulation of the sensitive parts. An exploded view and a cross section of a completed VT fuze are shown in Fig. 1.

Under the first production contracts, the cost per fuze averaged about $40. Subsequent improvements in design and production reduced unit costs to $16 to $23, depending on fuze type.[4] In 1997 dollars, this would equate to $130 to $186 per unit.

EARLY MISSILE PACKAGES

APL entered into packaging electronics for guided missiles in the late 1940s and early 1950s. Several atmospheric experiments were launched using V2 rockets confiscated from the Germans following World War II or later using Aerobee rockets.[5] Figure 2 illustrates an early analog guided missile computer using vacuum tube circuitry. Vacuum tubes and ancillary parts were mounted in an aluminum sheet metal housing configured to fit the missile. Tubes were socket mounted and hand wired into aluminum chassis. Small components (e.g., carbon resistors) were solder mounted on terminal boards or to insulated terminals. Larger components like paper capacitors were clamped and riveted or bolted to the chassis. Hand wiring typically involved bus wire that was covered with fabric insulation tubing often called “spaghetti.”

WELDING AND CONNECTORS

Early reliability studies, developed by the APL Space Department’s Reliability Group under the direction of R. W. Cole, indicated that in order to meet the Transit satellite mission goal of a 5-year orbit life, some extraordinary changes would be necessary. In addition to requiring very high-reliability components (transistors, diodes, resistors, capacitors, etc.), parts screening and qualification procedures, careful design rules, fabrication quality, workmanship standards, and reliability had to be built in. Richard Kershner observed that the largest single contributor to the reliability equation would be the interconnections. At the time, the reliability numbers for soldered joints and connectors were relatively low.

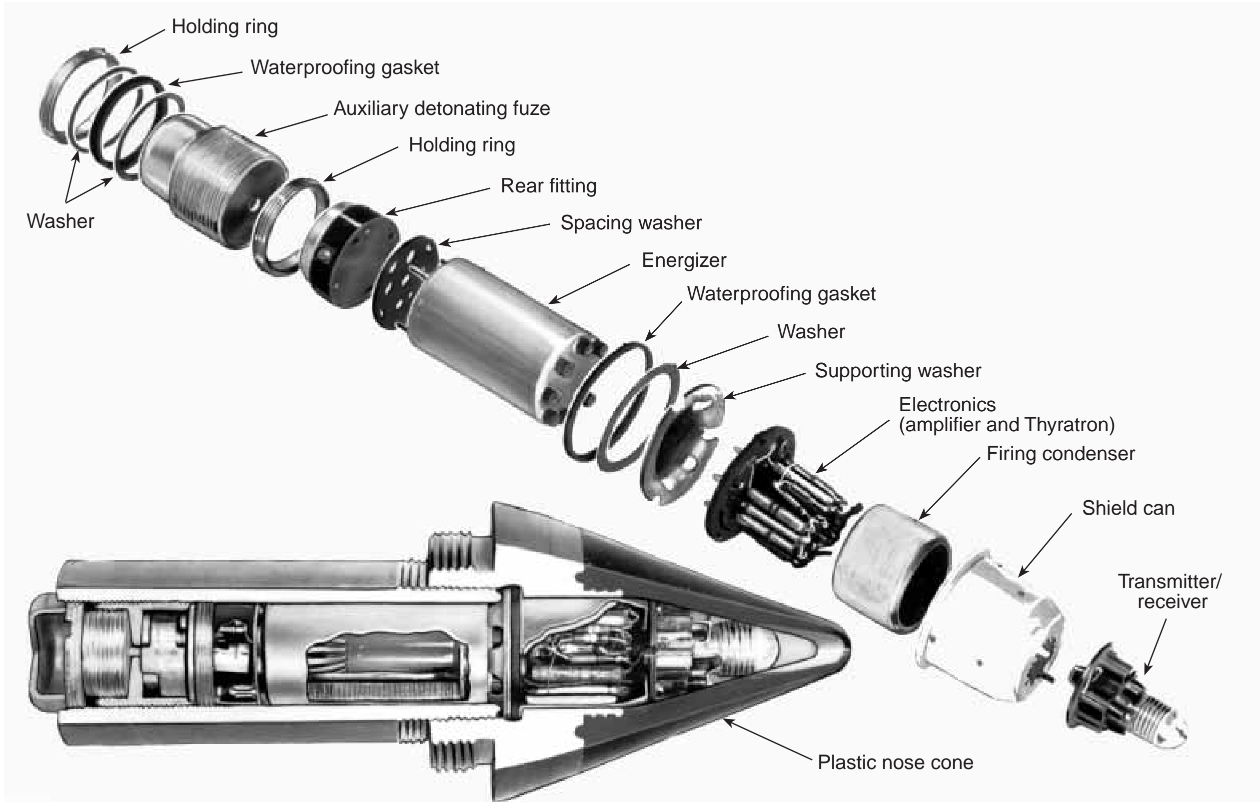


Figure 1. Exploded view and cross section of a VT fuze assembly.

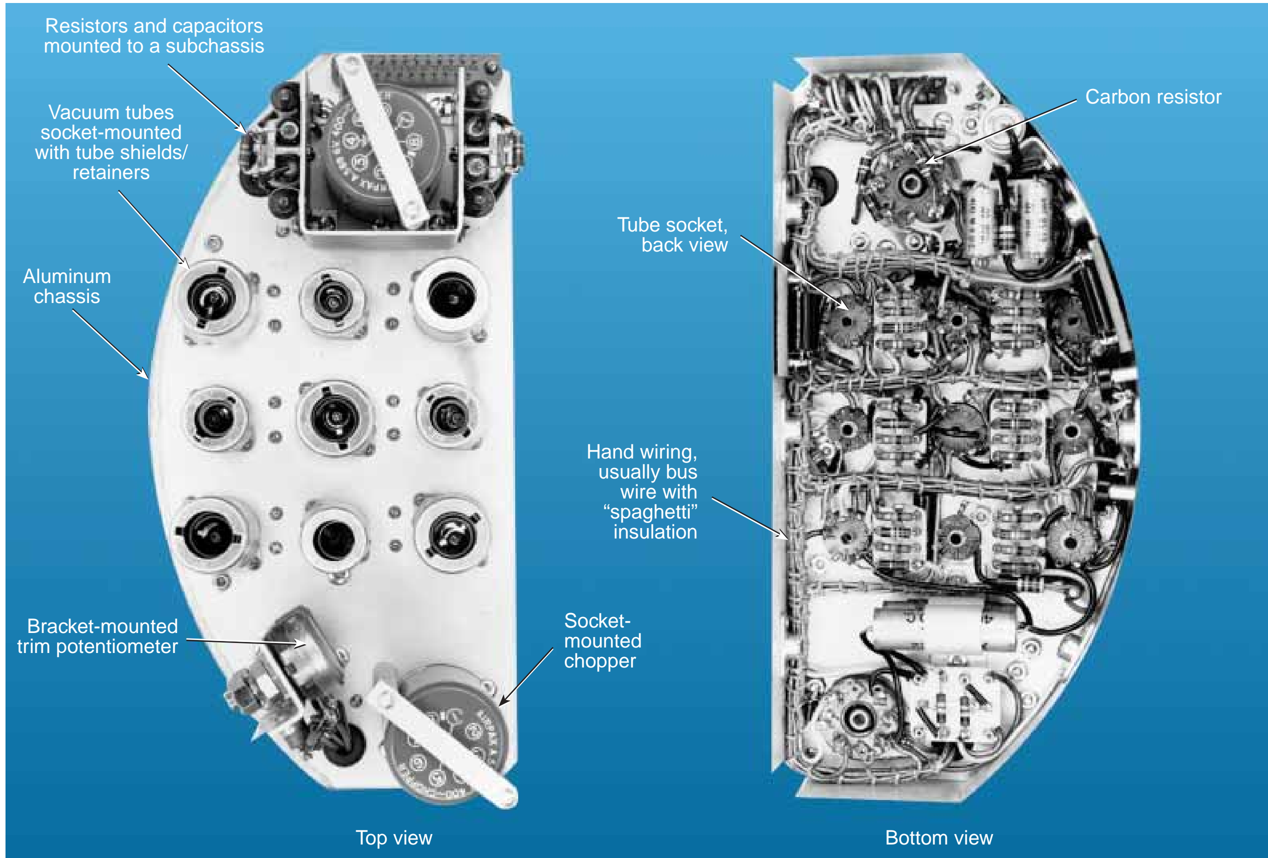


Figure 2. Guidance computer for the Tartar missile.

The military reliability handbook, MIL-HDBK-217A (Dec 1965), regarding connections stated, "The relative reliabilities of the various connection techniques in order of decreasing failure rate are as follows: (1) hand solder, (2) slip fit, (3) crimp, (4) machine solder, (5) weld, (6) wire wrap." More specifically, later editions of the handbook from the 1960s and early 1970s cite the failure rates (failures/10^6 h) as follows: soldered joints (hand), 0.0026; soldered joints (machine), 0.00029; welded connections, 0.00005; and wire wrap connections, 0.0000025.

On the basis of these data, welded connections were clearly preferred over soldered connections. Wire wrap connections were also preferred over slip fit connectors whenever modules had to be connected or reconnected for testing, evaluation, installation, or removal. Since Transit was expected to require as many as 40,000 connections, the Space Department dictated welding processes whenever possible and developed a cable and harness technique that depended on wire wrap instead of the usual military-style connectors.

To further ensure the 5-year lifetime for Navy satellites, welding processes had to be fine-tuned. These processes were investigated by APL's Richard C. Evans. Working with Algimatis Dargis, Evans developed a modified welder that used a reproducible square pulse, controllable in both amplitude and width.[6,7] The square pulse improved the quality of the metallurgical weld connection compared with welds made with traditional capacitor discharge welders, which used a less predictable exponential pulse. Welding current was programmed by adding high-current power driver boards in parallel. Each board was capable of about 80 A, and with 20 boards in parallel, about 1600-A square pulses were possible. Pulse width was controlled via a one-shot multivibrator adjustable over a range of 2 to 20 ms.

Printed Wiring Boards

Many of the Laboratory's circuits have relied on printed wiring boards (PWBs) for electronic interconnection. Early efforts with PWBs in the 1950s used single-sided through-hole circuit boards, usually with a design rule of 100-mil lines and 100-mil spaces. Processing started with artwork, which was often generated with India ink on paper or linen substrates, then photoreplicated and etched with ferric chloride on phenolic boards. In miniature applications, e.g., later VT fuze designs or early missile designs, subminiature tubes and other components were mounted using hand solder techniques. The tubes were often inserted into an aluminum heat sink and mounted on the board. Some of the larger tubes were plugged into 8-pin "octal" sockets and held in place with spring retainer clips. These sockets were usually mounted on a chassis where components were attached between the sockets and terminals or were directly wired terminal-to-terminal. In later designs, these sockets were mounted directly on epoxy glass PWBs.

With improvements in photolithographic tools and technology, line widths and spaces have incrementally decreased from 100 mils to the current capability of 5-mil lines/5-mil spaces. Numerous other changes have been incorporated over the years, for example,

- Boards went from single-sided to two-sided to the present multilayer type, which can have as many as 20 conductor layers.
- Board materials have evolved from basic phenolic to a wide variety of materials including epoxy glass, Teflon/glass, Teflon/ceramic, polyimide, and Kapton to serve the need for different dielectric constants and various structures.
- Originally, component attachment using eyelets and standoff terminals was the norm. Z wires replaced eyelets, only to be replaced with plated through-holes. Terminals have been replaced by through-hole mounting, which is being superseded by surface mount technology (SMT), with components mounted on both sides of the board. Direct chip-on-board (COB) technology is under development.

As the need for higher density has grown, PWB technology has responded with still further advancements. Figure 3 depicts some of the evolutionary techniques that have been used for vias in circuit boards. Figure 4 is an example of the circuit boards developed and packaged for Transit 3B, which was built and launched in February 1961. The boards were packaged using two-sided PWBs with eyelets and included a digital clock system and a memory of 384 bits consisting of square-loop magnetic core switches connected as a serial shift register. (Note the absence of connectors in Fig. 4.)

Over the span of 56 years, APL has literally designed and developed tens of thousands of PWBs using these techniques. Figure 5 illustrates two of APL's recent PWBs as examples of modern circuit board technologies. The NEAR spacecraft board in Fig. 5a is a 8.00 × 8.75 in. multilayer polyimide board using a design rule of 10-mil lines/10-mil spaces. It has 201 components, 3457 circuit traces, and 2076 plated through-hole vias and includes three ground planes, three power distribution layers, and six signal routing layers. The "rigid flex" board (Fig. 5b) was designed and fabricated for the NEAR Infrared Spectrograph. The three rigid boards plus the flexible wiring were fabricated as a single board. After final component attachment and testing, the boards were folded up into a compact, integral assembly.

Welded Cordwood

In the early 1960s, APL engineers, in collaboration with Autonetics, Convair, General Electric, Hughes

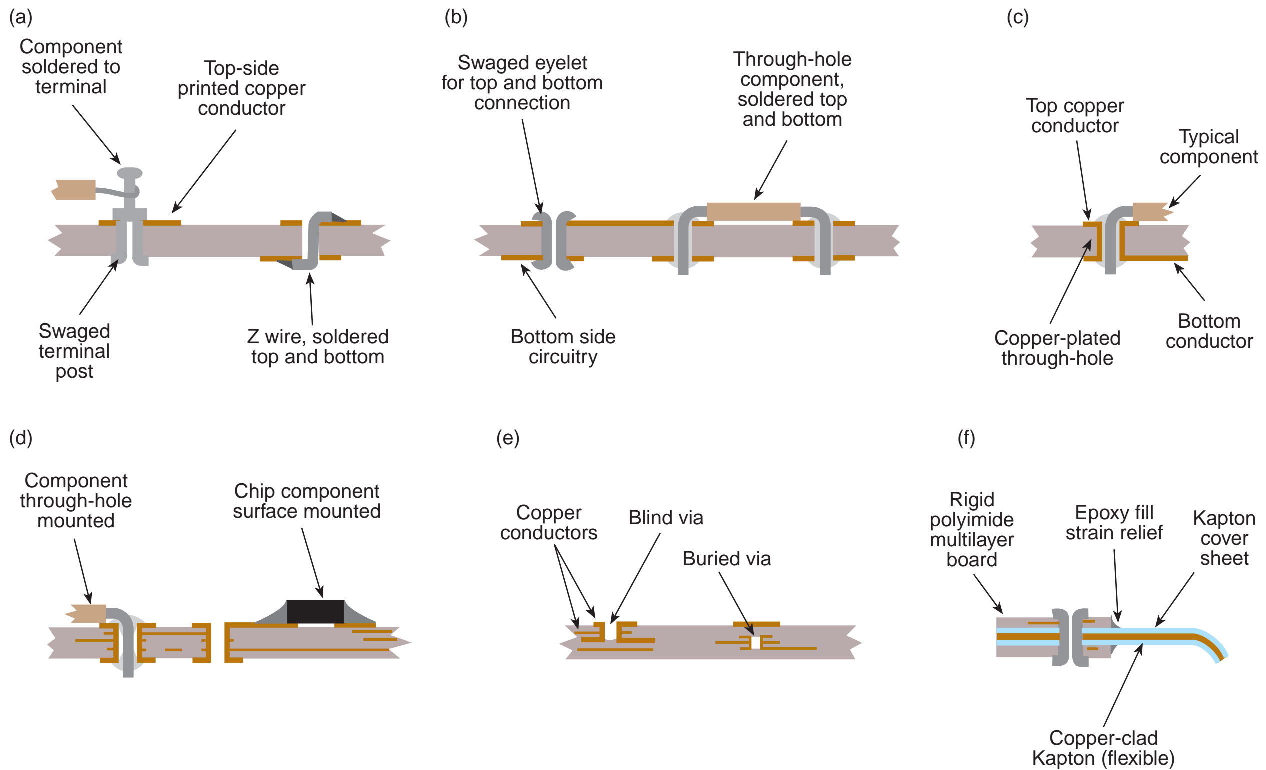


Figure 3. Some evolutionary steps in APL's printed wiring board development: (a) early use of Z wires and terminals, (b) eyelets or components for vias, (c) two-sided board with plated through-hole, (d) multilayer board with plated through-hole, (e) multilayer board with blind/buried vias, and (f) multilayer board with rigid flex.

Aircraft, Sippican Corp., Weldmatic, and WEMS, Inc., developed a three-dimensional welded cordwood packaging technique. The technique was intended to exploit the reliability of welded connections and to reduce weight and volume using a dense, three-dimensional packaging technique.

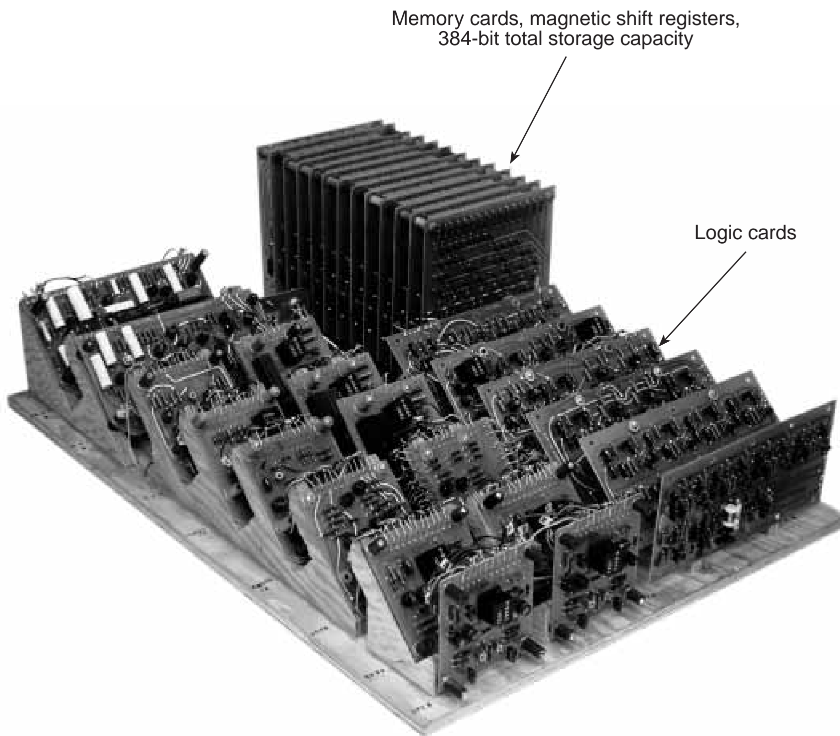
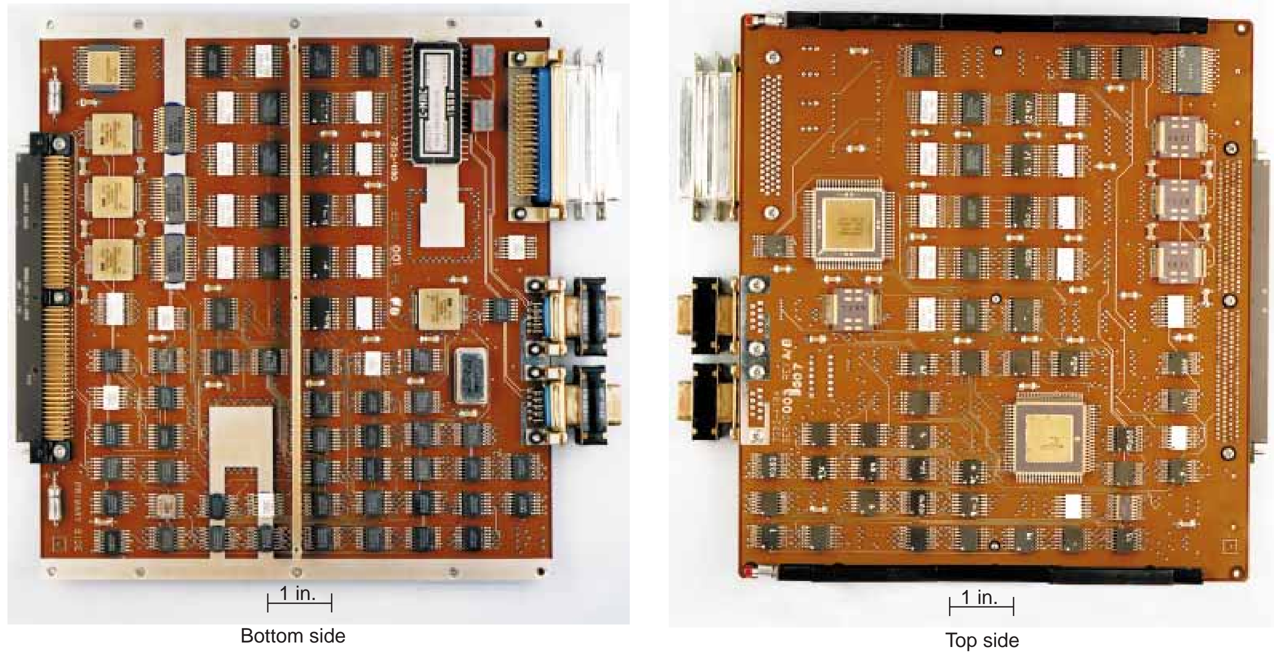


Figure 4. Circuit boards for Transit 3B memory system mounted on a test fixture, circa 1961.

A similar cordwood style of packaging using soldering techniques had become popular with the introduction of the commercial transistor radio sets of the time. Welded modules promised improved quality and reliability suitable for packaging satellite modules. Early welded cordwood modules used flat nickel wire, later replaced by round nickel wire. An article in the *Technical Digest* in late 1961 was entitled "Welded Cordwood—Last Step in Conventional Circuits?"[8] This title proved to be premature in that electronic packaging at APL has made great strides since, and continues to be a rapidly changing field.

Welded cordwood was further developed by the Space Department for their early satellites. Figure 6a illustrates the construction of three-dimensional cordwood modules as designed for Transit. Following the development of the

(a)



(b)

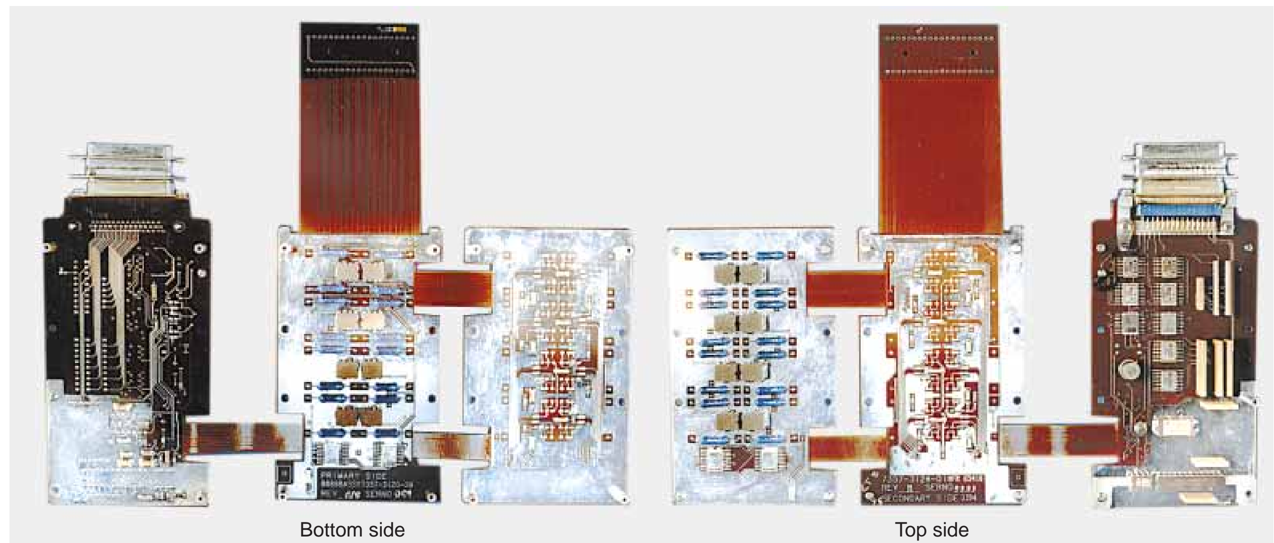


Figure 5. Modern circuit board technologies developed at APL. (a) Multilayer processor board used on NEAR and the Advanced Composition Explorer. (b) Rigid flex board for the NEAR Infrared Spectrograph.

circuit design and a schematic diagram, the cordwood module design started with a layout of the components in a cordwood fashion. The designer then proceeded to create the interconnections for the top and bottom Mylar films using an orthogonal matrix welded pattern. The wiring pattern was printed on a Mylar film to aid the welding assemblers. Holes were punched in the film to allow the wire to be interleaved with it to hold the wires in place, and to give the matrix some stability. Larger punched holes served as vent ports to allow penetration of the final foam encapsulation. The components were welded into the assembly next, followed by the addition of the wire wrap header. Modules were then tested, reworked if necessary, and finally encapsulated, usually using a lightweight but rigid Eccofoam.[9] The resultant solid module was subsequently tested, qualified, and wire wrapped into the next assembly level, known as a book.

Books were larger assemblies of systems or subsystems. They usually were about 7.0 × 7.5 × 1.5 in. and machined from aluminum or magnesium (Fig. 7). Often the base contained a two-sided PWB (a motherboard)

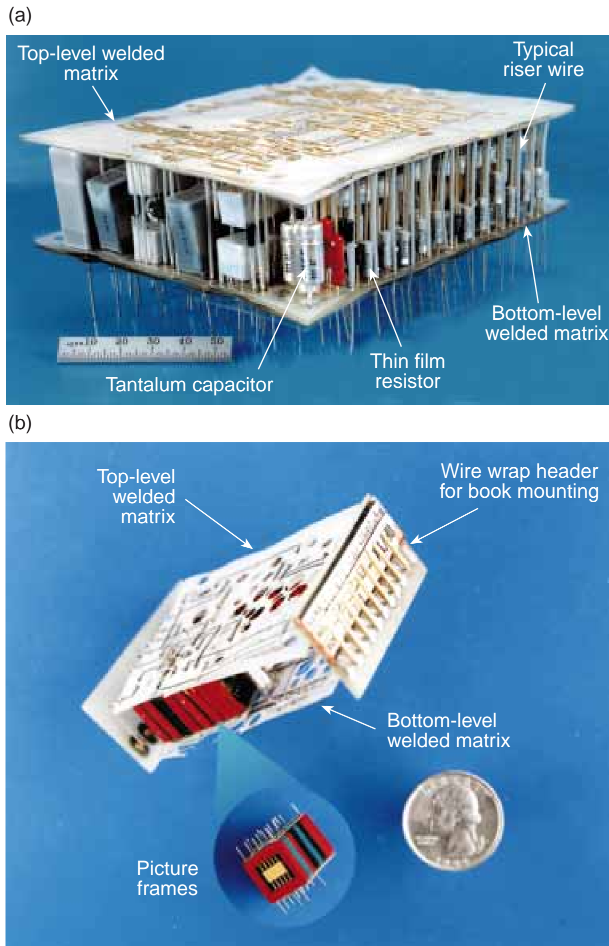


Figure 6. Cordwood modules (a) designed for Transit in the early 1960s and (b) illustrating mounting in a picture frame.

that served as an interconnection for the individual modules. The motherboard also included wire wrap pins for connections such that each module could be installed or removed by wire wrap connections. These books were eventually stacked together (like books) and fastened to the satellite structure with long 3/16-in.-dia. bolts. Harnesses were developed to interconnect the books with the satellite. Wire wrap fanning strips on the harness allowed for appropriate wire wrap assembly and disassembly throughout the testing and debugging process.

The Introduction of Integrated Circuits

ICs had been developed in the late 1950s for the Minuteman Missile Program by Texas Instruments. Originally these parts were only available for selected high-priority military missions. By the early 1960s, they became more widely available.

Early satellites had been developed using square-loop ferrites (Fig. 7) as logic/switching and memory elements. These circuits consisted mostly of copper magnet wire, the ferrite toroid cores, and a few transistor clock driver circuits mounted on a PWB. The circuits were small since the logic cores were typically 0.200 in. in diameter, and the memory cores were as small as 0.007 to 0.025 in. in diameter.

Since these magnetic logic and memory parts were essentially passive, they consumed little power and were reliable and radiation hard. Unfortunately, they were also difficult to build and test. The wire size of AWG 39 (5.2-mil dia.) or AWG 40 (4.8-mil dia.) was hard to handle, and keeping track of the number of primary and secondary turns was burdensome. The resultant circuit structures were also fragile and difficult to troubleshoot during the test phase. Repairs, especially after encapsulation, were even more arduous or often impossible. ICs appeared to offer a better solution.

George J. Veth of the Microelectronics Group developed an early packaging scheme for ICs using solder preforms assembled with infrared soldering to create a cordwood-style package.[10] These modules were expected to be highly reliable, and were inexpensive enough to be considered as “throwaways.” The basic module consisted of three parts: the ICs packaged in flat pack form, top and bottom PWBs for the circuit interconnections, and riser wires to transport signal and power between the top and bottom conductor planes.

The first APL application of ICs into a satellite was due to the efforts of Richard S. Cooperman and G. Donald Wagner for the Geos A and Geos B missions. These NASA satellites used Texas Instruments Series 51 RCTL (resistor coupled transistor logic) “solid logic” circuits. Simple logic functions such as dual flip flops, NOR gates, NAND gates, and exclusive OR gates were available in 1/4 × 1/8 in. flat packs. The Minuteman ICBM Missile Program had used these same packages, soldered or parallel gap–welded to conventional PWBs.

APL satellite package designers, lacking confidence in soldering or in parallel gap welding to copper-clad boards, subsequently developed a scheme suitable for three-dimensional welded cordwood known as the “picture frame.” Flat packs were welded into epoxy molded (picture) frames that expanded the tiny 1/4 × 1/8 in. flat pack into a larger package suitable for welding into cordwood modules.[11] Figure 6b illustrates a cordwood module made of the IC flat packages mounted in picture frames.

Some of the picture frames performed other functions, e.g., the black frames were simply “feed thru” frames and carried the riser wires between the top and bottom of the module. Wiring complexity often demanded several layers of Mylar welded matrix interconnection on the top and bottom. Following test, evaluation, and any necessary rework, they were similarly encapsulated in Eccofoam. This packaging style was used extensively for the Geos A, Geos B, and early Small Astronomy Satellite series. The encapsulated modules shown in Fig. 7 typify satellite packaging during the late 1960s.

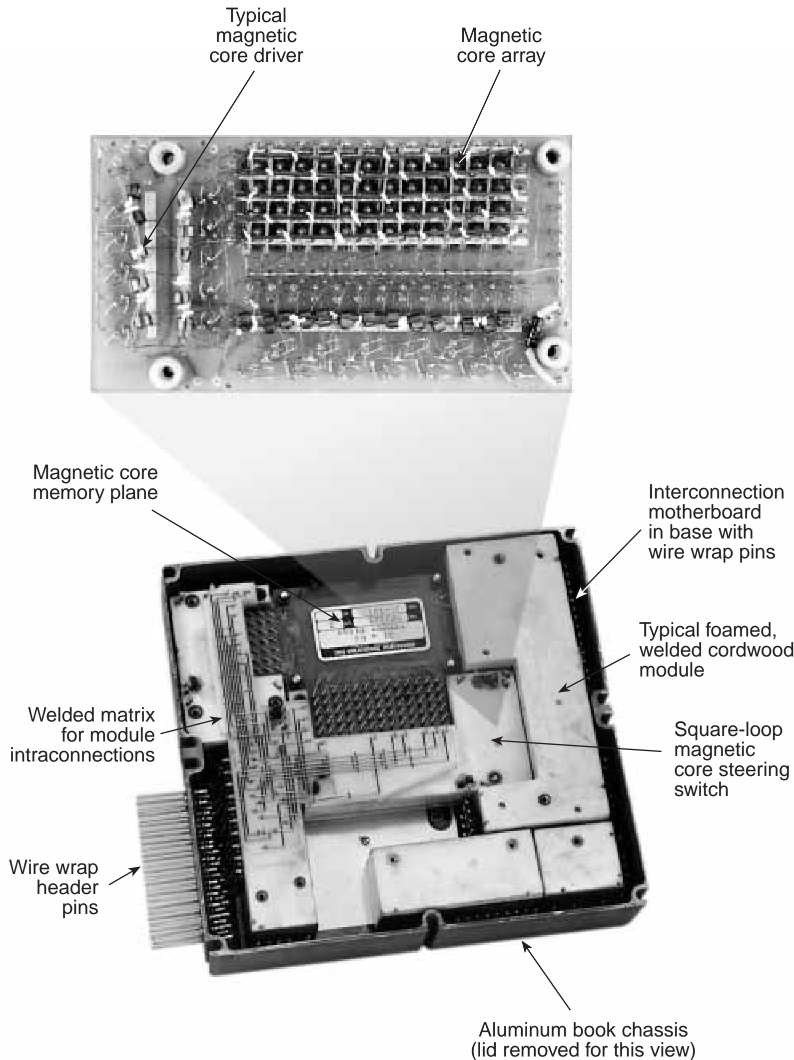


Figure 7. Assembled satellite book for Geos A, with an expanded view of the underside of the square-loop magnetic core current switch before encapsulation.

Ministick

The picture frame concept had several undesirable features. It did not take advantage of the small flat pack size, it simply made bigger packages to be used cordwood style; it made replacement of defective ICs difficult; it doubled the number of connections; and it was hard to test. Rework after encapsulation was especially tedious and often impractical.

These drawbacks were recognized by Carlton F. Noyes and Robert E. Hicks, who developed a weldable IC package scheme which they labeled ministick.[12] Ministick was basically a weldable multilayer technique (see Ref. 12 for detailed photos). A multilayer substrate was created using layers of glass cloth impregnated with epoxy resin (B-stage cured) and overlaid with photo-etched Kovar conductors; the entire structure was then laminated in a press at 330°C. The buildup of many of these layers resulted in a rugged board capable of packaging about 4 ICs/in^2 on a substrate about 0.250 in. thick. ICs were mounted onto the stick above the routing channels using an adhesive. The Kovar tabs that extended from the routing channels into the open area would then be gently bent upward to meet the IC lead and were welded using a slightly modified APL resistance welder. The assembled circuit boards were interconnected using a flexible ribbon cable.

This technique reduced the weight and volume of the Transit satellite by approximately 66%. Because of its structural integrity, it was not necessary to encapsulate these ministick modules; and, with all test points accessible, voltage waveforms were easily monitored and the test or repair time was reduced by a factor of 3. Reliability was also improved since the number of interconnections was reduced from about 30,000 to 10,000. Figure 8 is a photograph of the Transit satellite 16-bit computer system packaged using the ministick scheme.

The routing design of the ministicks was a particularly interesting and challenging task. It was prone to human error, and design changes often meant that the entire board would have to be scrapped, or an occasional bad net could be disabled and replaced by a magnet wire (usually green) fix. To improve the routing process, Robert C. Moore developed a computer-aided layout program.[13] Although crude compared with today's computer-aided design routers for circuit board layout or chip design, the program was effective for improving the design integrity of the ministick boards.

Hybrid Circuits

Engineers were excited about using ICs, but ICs could not do everything; for example, the designers often wanted higher-speed transistors capable of higher current, voltage, or frequency, or special components or tolerances. These demands spawned the need for a hybrid, that is, a circuit that used miniature discrete components (resistors, capacitors, transistors, diodes, ICs, etc.) in chip form, but intraconnected on a common substrate, often using IC-like processes and IC-like

packages. APL's Microelectronics Group, originally organized in 1960 to develop monolithic microelectronics, redirected its efforts to focus on hybrid circuit development and fabrication.[14] Since its inception, the Microelectronics Group has designed, developed, fabricated, and tested thousands of hybrids for missiles, radars, satellites, instrumentation, and biomedical applications.[15]

Thin film hybrid circuits had been developed using ceramic (Al_2O_3) substrates, aluminum (Al) or gold (Au) conductors, and chromium (Cr) or nichrome (NiCr) resistors; active silicon components were soldered or later epoxy-attached and wire bonded using 1-mil Al or Au wires. These substrates were then attached (using solder or epoxy) into a package, wire bonded to the lead frame, and then hermetically sealed.

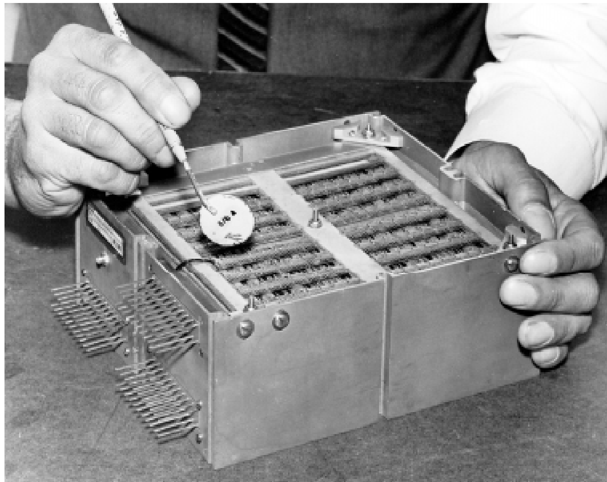


Figure 8. Transit computer book illustrating ministick packaging.

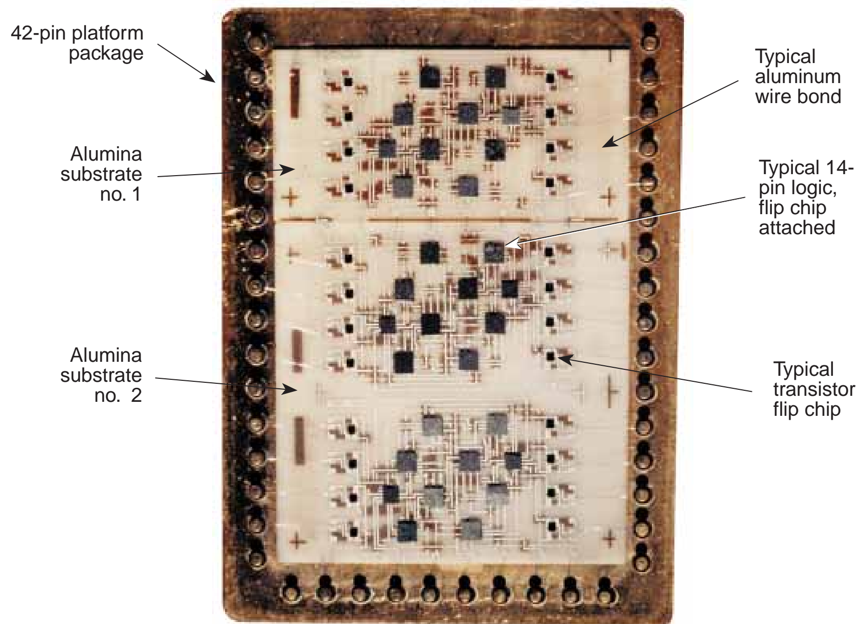


Figure 9. Flip-chip PRN (pseudorandom number) Generator hybrid, circa 1969.

If a high-reliability application was needed, these hybrids were then fully tested, burned in, and screened to meet military standards (typically MIL 883).

One of the Microelectronics Group's earliest hybrids was the "source-sink driver" circuit designed by Jim Perschy for the Transit memory system. Ninety-six of these circuits were used in each satellite; no known in-orbit failures occurred in the history of Transit.

Another interesting experimental hybrid developed in 1969 used flip-chip technology. The circuitry for this hybrid PRN (pseudorandom noise) Generator (Fig. 9) is similar to the one described in Ref. 16, but instead of using conventional chip-attach die bonding and wire bonding methods, these chips were purchased with special solder-bumped pads. They were then flipped and ultrasonically bonded to the specially developed substrate. The result was a simultaneous chip-attach and connection process that was attractive because of its low cost and simplicity at the assembly level.

Unfortunately, the semiconductor suppliers stopped producing these "bumped chips," and we were unable to fully exploit the technology. Recent advances in solder bumping and the need to further reduce costs and gain improved high-speed performance have created a renewed interest in flip chips (see the article by Bevan and Romenesko in this issue).

Some other examples of APL circuit designs are shown in Figs. 10 and 11. The thin film hybrid in Fig. 10 is a 4-channel 24-bit accumulator used on the Galileo satellite. The package included four custom-designed radiation-hardened chips fabricated by the Sandia National Laboratories and represented APL's first endeavor with standard cell custom chip design. These chips were epoxy-attached to an Al_2O_3 substrate with vacuum-deposited aluminum conductors and thermosonically gold wire bonded. The brown areas on the substrate are vacuum-deposited SiO (silicon monoxide), which was used as an insulator in case the wire bonds should sag and short to the aluminum conductors.

The thick film hybrid shown in Fig. 11 represents one of our most complex hybrids. Built in 1984, it included 36 silicon chips, mostly of the medium-scale integration level, in a 30-pin flat pack measuring $1.750 \times 0.875 \times 0.200$ in. The six-layer thick film substrate used a 7-mil line/7-mil spacing design rule with about 540 total wire bonds required. This pulse generator was one of three complex hybrids for a biomedical implant device used to stimulate nerves and reduce the

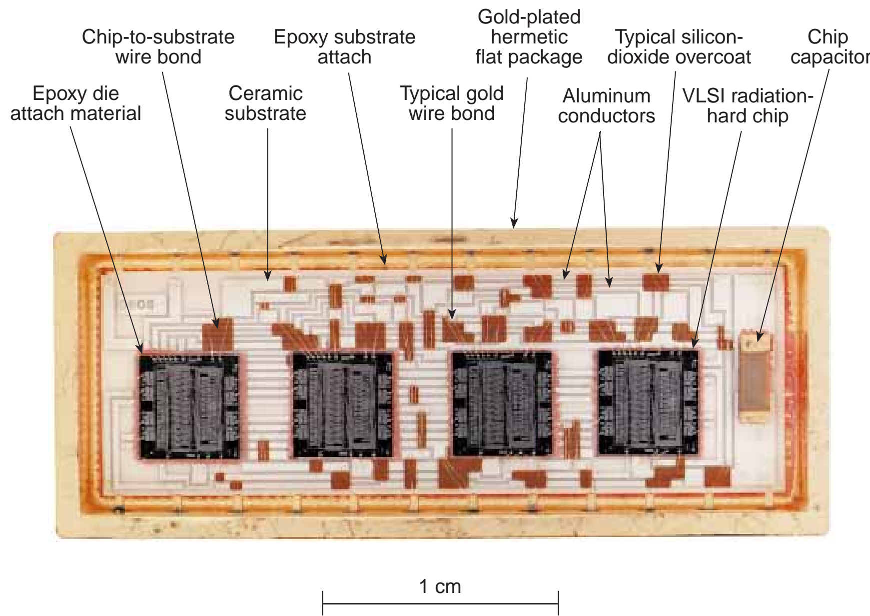


Figure 10. Hybrid accumulator for Galileo, circa 1980 (VLSI = very large scale integrated).

effects of chronic pain. Such dense hybrids often required extensive rework, resulting in low yields.

Point-to-Point Welding and Stitch Welding

Although the picture frame and ministick methods served their purposes, APL engineers were still not satisfied with the repairability and density of their electronic packages. This dissatisfaction led to a new generation of packages using a point-to-point welding process. Point-to-point welded wire boards had many advantages: they could be easily repaired, parts could readily be removed and replaced readily, and wiring changes could be incorporated using the reliable APL resistance welder.

A unique feature of this technique was the wire-to-pin weld. The wire was compressed on the pin by the welder pincers, followed by initiation of the welding pulse. The pulse energy simultaneously melted the insulation on the wire and welded it to the pin. The operator manually performed wire routing using a wire run list developed by the designers. Initially, Teflon-coated nickel wire was used, but an occasional short circuit was observed during testing at the sharp corners of the pins. Replacement of the Teflon-coated wire with the more robust Durad-coated Teflon wire eliminated this problem.

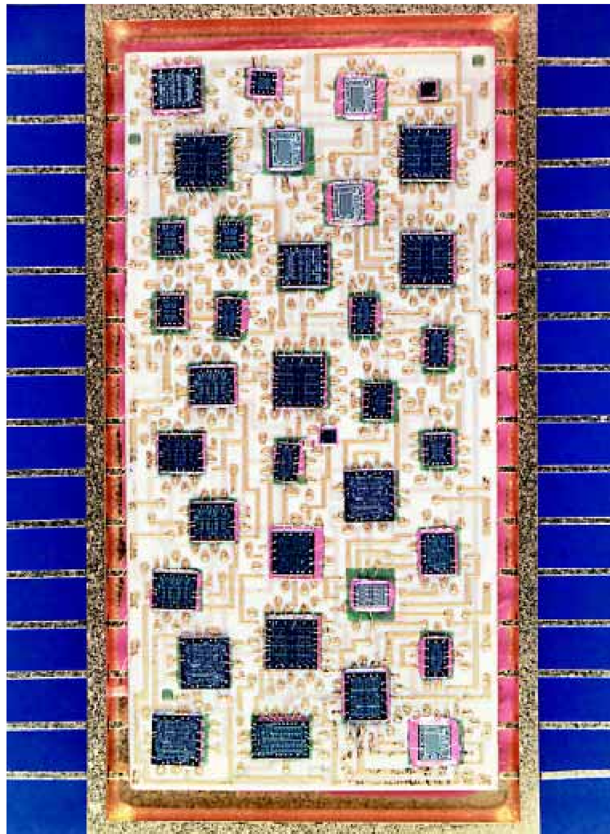


Figure 11. Pulse generator for the Human Tissue Generator, circa 1984.

Figure 12 shows the Triad processor boards developed in 1971 using point-to-point welded wire techniques. On such a complex system, the back side point-to-point interconnection became very dense and could be difficult to troubleshoot and repair. Triad represented an early application of a fully programmable general-purpose computer into a satellite system. The package weighed 4.5 lb in a volume of 95 in^3. It was a 16-bit processor, used a magnetic core memory, and consumed 0.75 W in standby and 62 W in a sprint mode.

As board complexity increased, package engineers continued to search for better, denser, and lower-cost techniques. Although multilayer board techniques with plated through-holes were in vogue at many other facilities, APL's quality assurance engineers remained concerned about the reliability of a plated through-hole. Thus, the point-to-point technique was replaced by a "stitch weld" system.

Stitch weld was an evolution of point-to-point welding and was performed on a semiautomatic machine.[17] Computer software was used to generate a

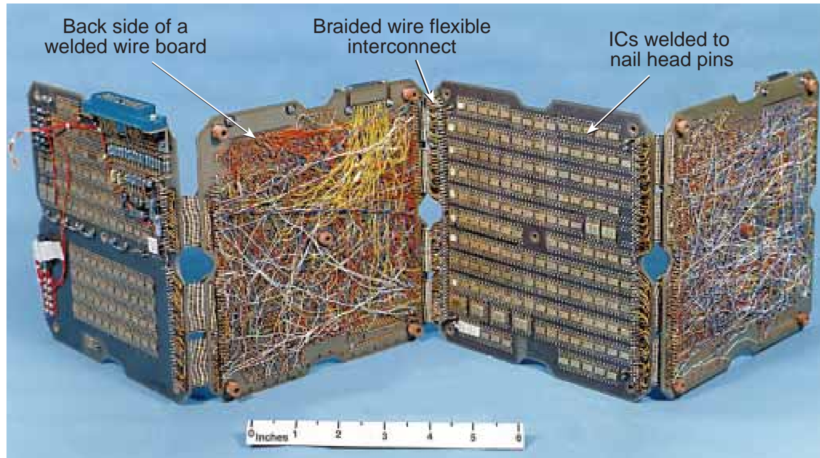


Figure 12. Triad computer system boards, circa 1971.

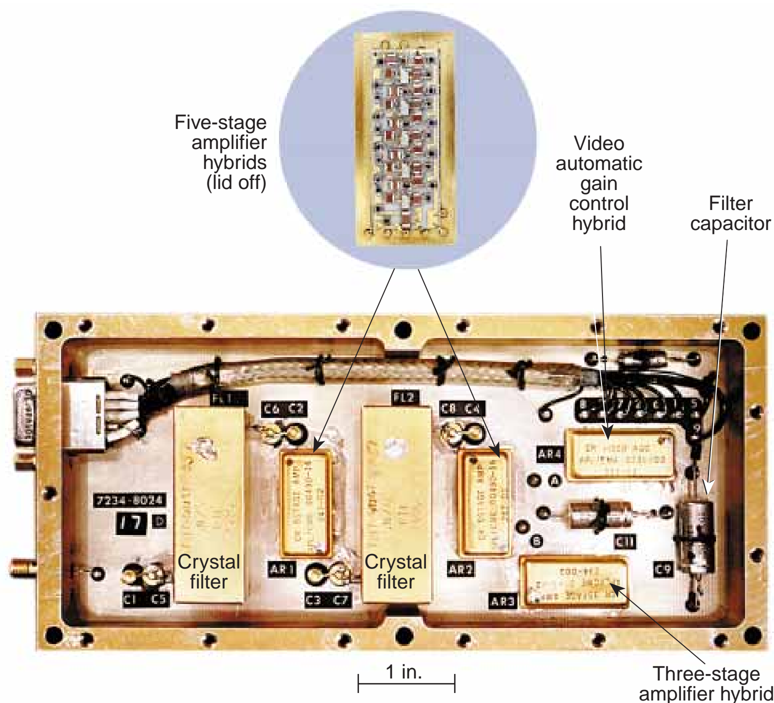


Figure 13. Command receiver assembly.

routing list and to punch a computer numerically controlled (CNC) tape. Routing was limited to serial strings (daisy chains), since only one weld was allowed per pin. Stitch weld was used on AMPTE (Active Magnetospheric Particle Trace Explorer), Geosat, HUT (Hopkins Ultraviolet Telescope), Polar BEAR (Polar Beacon Experiment and Auroral Research), and COBE (Cosmic Background Explorer) satellite programs. The early boards were custom-made at APL, but later boards used a standard Augat format with dual in-line IC sockets on the component side. A density of 40 to 50 interconnections/in^2 was typical, and occasionally more than 100/in^2 was achieved.

Surface Mount Technology

The development of SMT started at APL in the late 1960s and was expected to result in still higher interconnection densities, but at lower costs.[18] One early product was a tuned radio-frequency satellite receiver consisting of a narrow-band crystal filter, 2 five-stage amplifier hybrids, a three-stage amplifier hybrid, and a video amplifier/automatic gain control circuit hybrid. The hybrids used chip resistors, chip capacitors, and leadless inverted devices containing the active transistors, diodes, or ICs (see Fig. 13, inset). These devices were all reflow-soldered to a ceramic substrate. The substrate was patterned with Au-plated Cr/Cu conductors. Figure 13 is a photograph of the completed command receiver for Geos C, illustrating how these early SMT hybrids were soldered onto a motherboard and assembled into the receiver subsystem. This package design technique was extremely rugged and proved useful on many programs for satellites, missiles, and underwater applications.

SMT also began to be used on nonhermetic PWBs as well as hermetically sealed hybrids. Figure 14 illustrates the flexibility of the SMT to use both through-hole techniques and SMT. Similar boards were used on the Red-Eye missile program in the early 1970s and demonstrated their ability to survive high G loads. Various board materials have been used including epoxy glass (FR-4 or G-10), ceramics, Teflon/glass, and polyimide. For space applications, polyimide is most often selected because of its low thermal expansion properties. Figure 15 is another example of how SMT technology has been used in an APL underwater system.

Chemically Milled Chassis

While most of APL's earlier chassis were made of sheet metal (usually aluminum) or machined blocks of aluminum, chemical milling of beryllium copper (BeCu) was used in the late 1960s.[19] BeCu was strong

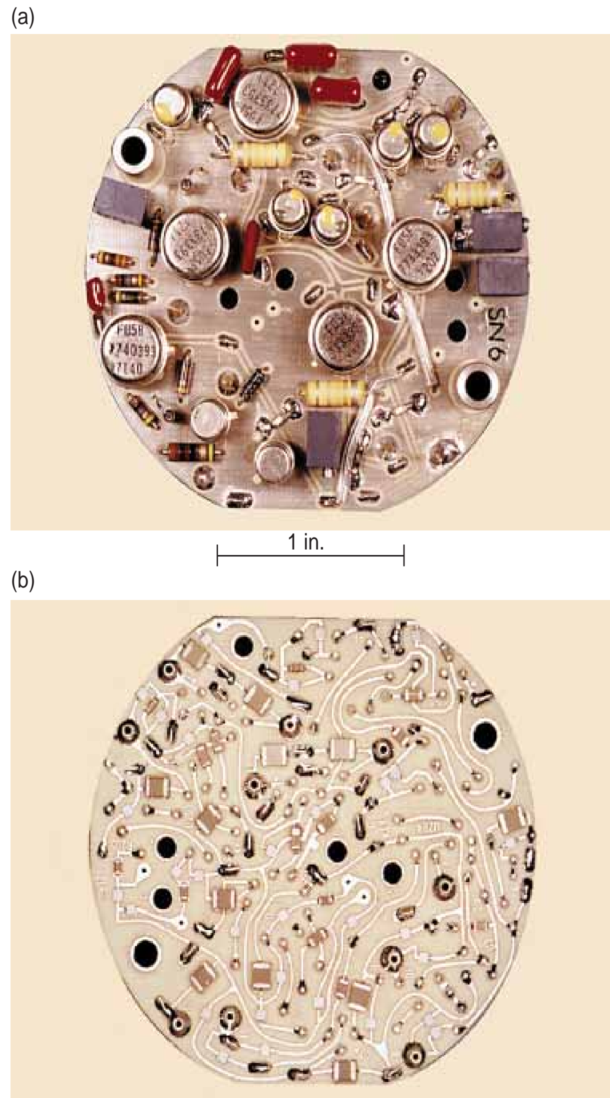


Figure 14. Missile board (early 1970s) illustrating (a) through-hole techniques on the top side and (b) SMT on the bottom side.

and lightweight; had good electromagnetic shielding properties; and was easily soldered, formed, and patterned using chemical etchants. Figure 16 is a photograph of some of the "chem-milled" chassis fabricated in 1974 for the SATRACK translator. They were built from 10-mil BeCu sheets, photolithographically patterned, etched from one side for the fold lines, and etched from both sides for the perimeter pattern.

Etching was performed in a ferric chloride bath. Since both sides had been photo-patterned and etching took place from each side simultaneously, the time in the bath was easily determined when the perimeter was etched through. This also ensured that the fold lines were only etched halfway through. Following the etch, the boxes were folded and formed. Edges were soldered or tabs twisted to firm up the chassis. Sturdy, square BeCu blocks were sometimes soldered into etched holes to allow for screw mounting or as fastening nodes for other modules. Finally, to prevent oxidation, the packages were usually gold plated. The technique was especially attractive for RF and microwave applications, but has seen little use since the 1980s, probably because of shape limitations and some of the manual steps required in the fabrication processes. CNC-machined chassis seem to be preferred today.

Figure 17 shows how this technique was used in a 1.575-GHz amplifier. Most of the circuitry was built on separate ceramic substrates using Cr/Au conductors. Components were added using surface-mount techniques. For operation at 1.575 GHz, microstrip techniques were necessary. The interconnect substrate was Epsilam 10, a Teflon-ceramic–impregnated, two-sided PWB with copper-clad conductors. All connections were hand wired and soldered. Epsilam 10 substrate material was chosen for its microwave properties, low losses, and dielectric constant (ϵ_r) of 10, making it suitable for microstrip lines and compatible with the Al_2O_3 substrates, also with an ϵ_r=10. Other examples of microwave electronics packaging are described in the article by Kopp, Moore, and Coffman, this issue, and in Refs. 20–22.

Biomedical Applications

In the late 1960s, Robert E. Fischell became interested in applying space technology to biomedical applications. As a result, a fixed-rate rechargeable cardiac pacemaker was developed using a rechargeable nickel-cadmium (NiCd) cell.[23] Previous pacemaker technology was limited by battery size and capacity. Through the use of a rechargeable NiCd battery and improved

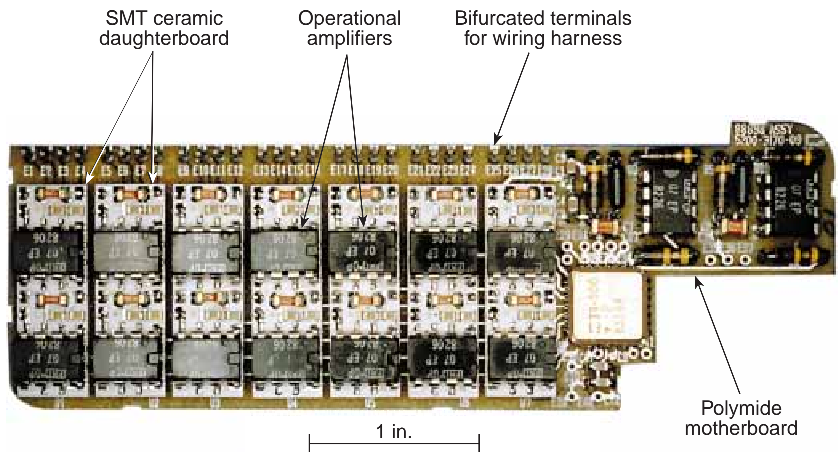


Figure 15. Recent multilayer board design for a nonacoustic sensor.

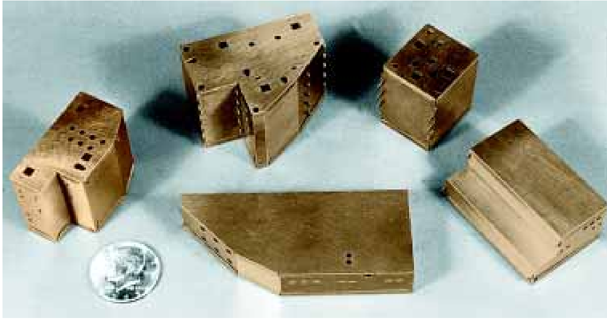


Figure 16. Chemically milled chassis for SATRACK, circa 1974.

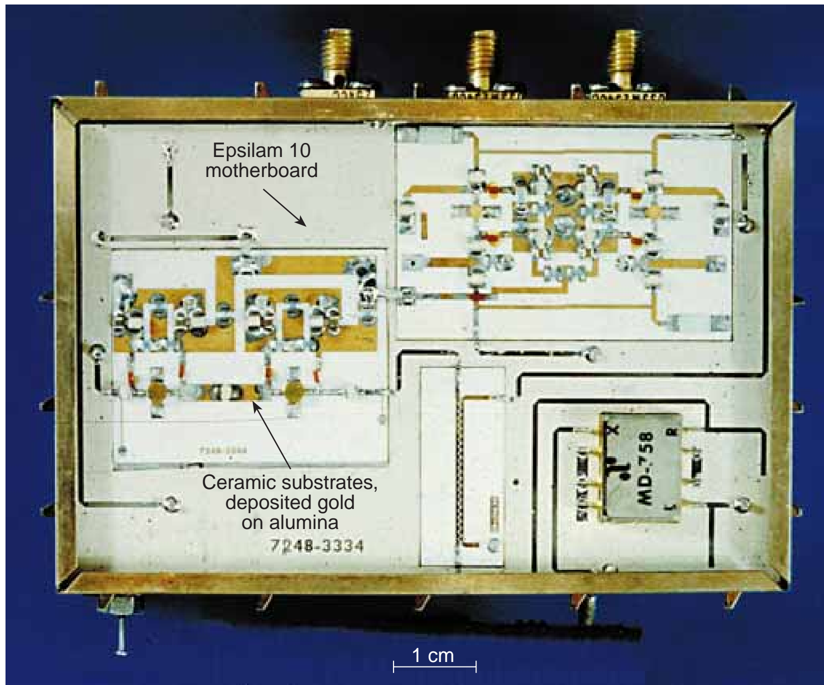


Figure 17. A 1.575-GHz amplifier for Transat, circa 1974.

packaging, the pacemaker volume was reduced from 88 to 22 cm^3, weight was reduced from 178 to 63 g, and the implanted lifetime was extended from 22 to 120 months.

Early pacemaker hybrids used vacuum-deposited Cr/Au conductors on an Al_2O_3 substrate. Precision nichrome resistors deposited on silicon chips were separately attached to Cr/Au pads using insulating epoxies. Chip capacitors, transistors, and diodes were solder-attached using SN62 (tin/lead/silver) solder. Chip resistors were redundantly wire bonded to the substrate using 1-mil Au wire. Substrate-to-the-platform–style package pin connections were made with 10-mil Al ribbon bonds to accommodate peak currents and to gain improved reliability. An Au-plated Kovar lid was perimeter-soldered to the platform base to ensure a hermetically sealed package.

The Programmable Implantable Medication System

Whereas the early fuzes, missiles, and spacecraft required significant levels of microminiaturization and reliability, implantable biomedical electronics required further reductions in size. The Programmable Implantable Medication System (PIMS) pushed microelectronic package engineers to develop new levels of packaging density.

An implantable programmable infusion pump, developed in 1980, served as part of PIMS.[24] The pump included state-of-the-art IC chips, an 1802 eight-bit microprocessor, a universal asynchronous receiver/transmitter, electronically programmable read-only memory, two random-access memory chips, and several Laboratory-designed custom gate arrays. These semiconductor devices were housed in ceramic chip carrier packages and were surface mounted to a custom-designed multilayer thick film substrate. The electronics package also included a number of discrete electrical components along with two thick film hybrid circuits mounted on both sides of the PWB. The entire electronics package was assembled in a hermetically sealed titanium case, which was 8.1 cm in diameter and 1.8 cm thick and weighed 0.38 lb. Also inside the package was a lithium battery, a refillable insulin reservoir, a refill port, a solenoid pump, an antenna, and a flow-smoothing network.

The system was externally commandable for programming the drug dosage and dose rates. Telemetry was provided for system status and monitoring of actual performance. Numerous safety features were built in to ensure reliability and safe drug dose levels. The system consumed a minimum amount of power, less than 8 μW, and a 5-year or more battery life was anticipated.

Multichip Modules

As the demand for higher packaging density has continued to grow, the traditional thick or thin film chip and wire hybrid circuit has evolved into a still more complex package known as the multichip module (MCM). An MCM might have more than 300 interconnections, more than a dozen chips, and typically greater than 25 inputs/outputs (I/Os). MCMs can be fabricated on laminate substrates (MCM-L) or co-fired ceramic substrates (MCM-C), or by using deposited

films on a smooth (usually silicon) substrate (MCM-D).

Figure 18 is an early example (1976) of APL's use of a two-conductor–level silicon substrate, which was processed like an IC. An aluminum conductor layer was deposited on Si and photolithographically patterned and etched. Next, silicon dioxide (SiO_2) was deposited and via holes were etched, followed by a second Al deposition and photolith etch. A SiO_2 deposition for passivation was applied, followed by an oxide etch to open access to the top metal layer for wire bonding. The resultant substrate had two dielectrically isolated metal layers with 50-μm lines/ 50-μm spaces.

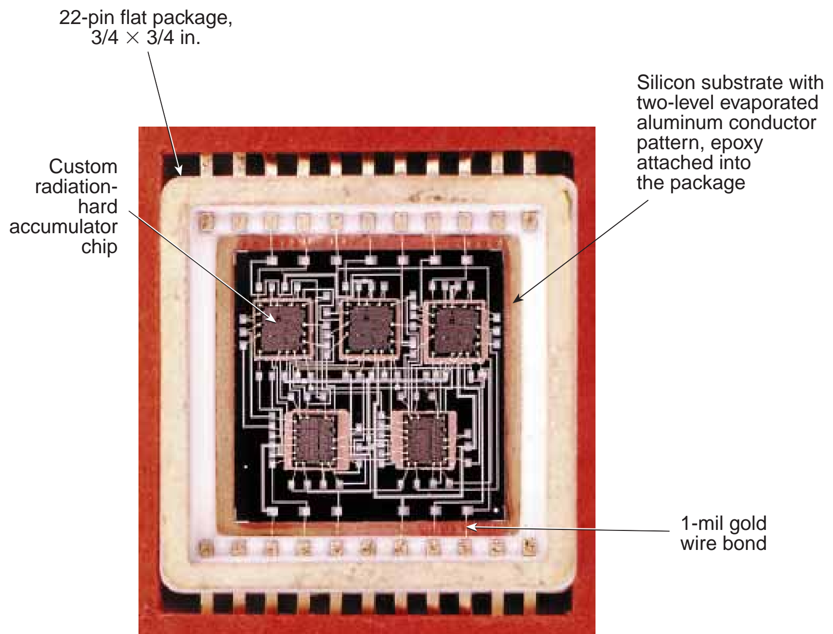


Figure 18. Hybrid using a multilevel conductor system deposited on a silicon substrate, circa 1976.

Figure 19 is an example of an MCM-C developed for the MSX (Midcourse Space Experiment) satellite. Known as the direct digital synthesizer, it served as a programmable RF source. It used GaAs chips clocked at 600 MHz to achieve output frequencies as high as 240 MHz.[25] Co-fired ceramic technology was chosen to meet the need for multilayer construction, high wiring density, good high-frequency performance, ability to build 50-Ω lines, and excellent heat transfer performance. A Dupont Type 848A4 low dielectric constant ($\epsilon_r = 4.8$), low-temperature, co-fired ceramic (LTCC) 4.2 mil thick was used. The resultant substrate had 10 conductor layers deposited on the 10 layers of LTCC material.

The MCM-D (Fig. 20) is an extremely dense circuit that has been recently processed at APL. This 2-in^2 substrate includes three levels of metal conductors, two copper layers with a gold layer on top. Line spaces/ widths are nominally 20 μm on the Cu layers and slightly larger on the top Au layer for compatibility with thermosonic wire bonding. When completed, this substrate includes 280 nets, 1089 bonding pads, 156 I/O pads, and approximately 1000 vias and accommodates 15 additional very large scale integrated chips. This final assembly results in a 2.375 × 2.375 × 0.180 in. hermetic package of extraordinary complexity (see the article by Blum, Charles, and Francomacaro, this issue).

CONCLUSIONS

I've been able to describe only a few of the many interesting electronic packaging applications developed by APL over its 56-year history. Our archives are full of hundreds more, including artillery shells, guided missiles, underwater instrumentation, sonar, radar, communications, space applications, biomedical applications, bird-borne instruments, ground support, aircraft support, and shipboard support equipment. Demand for sophisticated electronics will continue to provide packaging engineers with new challenges: higher performance for higher densities, lower costs, better heat transfer, new environmental requirements, more repairability, etc. These challenges are being met with new materials, new process technologies, new components, greater innovation, and new ideas. Systems engineers can expect to use and hear about some

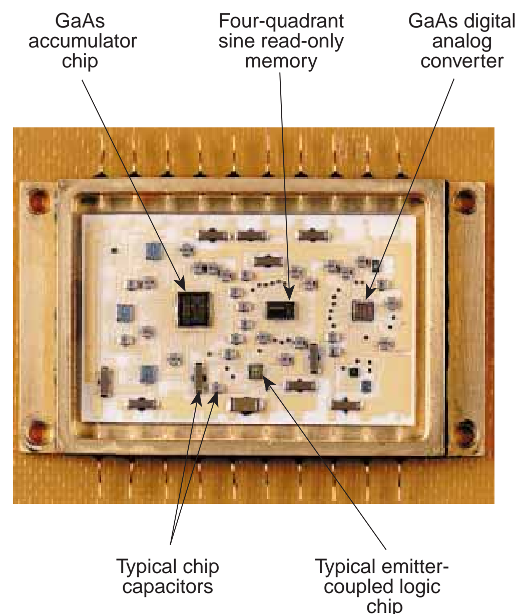


Figure 19. Direct digital synthesizer (example of an MCM-C).

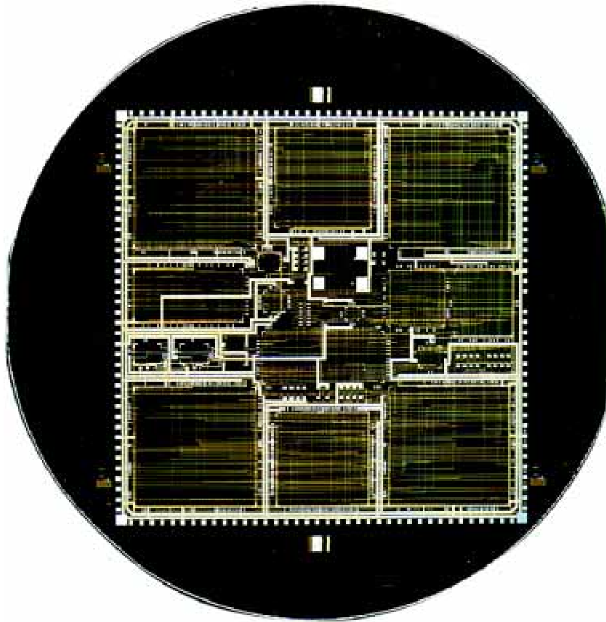


Figure 20. Modern MCM-D multilevel silicon substrate.

of these new developments soon with advanced MCMs, COBs, chip-scale packages, ball-grid arrays, flip COBs, three-dimensional packages, and various flip-chip techniques.

In the 1940s the vacuum tube was the basic electronic element. Today, a single IC containing perhaps as many as 100 million transistors has become the fundamental electronic element. Within the volume of the early proximity fuze, it is now possible to package hundreds of ICs, or, in terms of active devices, more than 1 billion transistors. The semiconductor industry's road map[26] for chip development has projected as many as 1.4 billion transistors on a single microprocessor chip, with up to 2700 I/Os per chip by the year 2012. These devices are expected to operate at clock frequencies of 1.5 GHz and dissipate as much as 175 W. These kinds of future chip developments will certainly keep APL package engineers well challenged in the future.

REFERENCES

[1] Baldwin, R. B., *The Deadly Fuze: The Secret Weapon of World War II*, Presidio Press, San Rafael, CA (1980).

[2] *The World War II Proximity Fuze*, Technical Monograph #140, JHU/APL, Laurel, MD (1950).

[3] Kleiderer, C. W., *The Role of Plastics Used in Project "A"—The World War II Proximity Fuze*, JHU/APL, Laurel, MD (1995).

[4] *The Development and Use of the Proximity or VT Fuze*, Department of the Navy, Washington, DC (20 Nov 1945).

[5] DeVorlien, D. H., *Science with a Vengeance. How the Military Created the U.S. Space Sciences After World War II*, Springer Verlag, New York (1992).

[6] Evans, R. C., and Dargis, A., *The APL Resistance Welder*, TG687, JHU/APL, Laurel, MD (1965).

[7] Evans, R. C., "The APL Resistance Welder and Its Role in Satellite Reliability," *APL Tech. Dig.* 5(1), 2–7 (1965).

[8] "Welded Cordwood—Last Step in Conventional Circuits?" *APL Tech. Dig.* 1(1), 20 (1961).

[9] *Plastic and Ceramic Foams*, ECE 86-058, Emerson and Cummings, Canton, MA (Mar 1980).

[10] Veth, G. J., "Optical Soldering and Microelectronic Interconnections," *APL Tech. Dig.* 3(3), 9–14 (1964).

[11] "Engineering," Chap. 6, in *History of the Space Department, The Applied Physics Laboratory 1958–1978*, SDO-5278, JHU/APL, Laurel, MD (1978).

[12] Noyes, C. F., "Ministick Packaging: A Further Aid to Satellite Reliability," *APL Tech. Dig.* 5(3), 2–10 (1966).

[13] Moore, R. C., "Computer-Aided Layout of Ministick Artwork," *APL Tech. Dig.* 6(3), 9–16 (1967).

[14] Charles, Jr., H. K., and Wagner, G. D., "Microelectronics at APL: The First Quarter Century," *Johns Hopkins APL Tech. Dig.* 6(2), 130–145 (1985).

[15] Charles, Jr., H. K., Wagner, G. D., and Abita, J. L., "Microelectronics at APL: 30 Years of Service," *Johns Hopkins APL Tech. Dig.* 11(1,2), 123–126 (1990).

[16] Prozeller, E. F., and Schwab, V., "The Triad PRN Navigation Experiments," *APL Tech. Dig.* 13(2), 12–21 (1974).

[17] Strider, R. S., and Wagner, G. D., "Computer Aided Manufacturing for Electronic Board Fabrication," *Johns Hopkins APL Tech. Dig.* 7(3), 267–269 (1986).

[18] Muccino, F. R., "Simplified Method of Microcircuit Fabrication," *APL Tech. Dig.* 9(4), 14 (1970).

[19] Hicks, R. E., "Chemical Milling of Space Flight Hardware," *APL Tech. Dig.* 6(4), 11–16 (1967).

[20] Abita, J. A., "Microwave/Millimeter Wave Technology," *Johns Hopkins APL Tech. Dig.* 9(3), 200–211 (1988).

[21] Sloan, R. F., Bokulic, R. S., and Sinsky, J. H., "An X-Band Telecommunications Transmitter for the Mid-Course Space Experiment," *Johns Hopkins APL Tech. Dig.* 14(4), 317–323 (1993).

[22] Kopp, B. A., and Barnett, S. C., "C-Band Receive Module for Phased-Array Antenna Applications Using Commercially Available Monolithic Integrated Circuits," *Johns Hopkins APL Tech. Dig.* 14(4), 333–338 (1993).

[23] Barnhart, P. W., Fischell, R. E., Lewis, K. B., and Radford, W. E., "A Fixed Rate Rechargeable Cardiac Pacemaker," *APL Tech. Dig.*, 2(9) (Jan–Feb 1970).

[24] Fischell, R. E., "Microcomputer-Controlled Devices for Human Implantation," *APL Tech. Dig.* 4(2), 96–103 (1983).

[25] Dennisen, R. A., McCarty, T. A., Clatterbaugh, G. V., Chao, K., Mobley, S. J., et al., "A GaAs DDS System for Space Applications," in *Government Microcircuit Applications Conference 1991 Digest of Papers*, Vol. XVII, pp. 601–604 (1991).

[26] *The National Technology Roadmap for Semiconductors*, Semiconductor Industry Association, San Jose, CA (1997).

THE AUTHOR

G. DONALD WAGNER recently retired from APL after 35 years of service as both an engineer and a technical manager. He was a member of the APL Principal Professional Staff and most recently served as Manager of Engineering, Design, and Fabrication Resources in APL's Technical Services Department (TSD). Mr. Wagner had previously held positions as lead engineer on several satellite subsystems and scientific instruments in APL's Space Department. He also served as Group Supervisor of TSD's Microelectronics Group and Assistant Branch Supervisor of the Engineering and Fabrication Branch. In these various positions, he often had the opportunity to engineer, design, lead, and observe many of APL's interesting and unique electronic packaging developments over the years. His e-mail address is don.wagner@worldnet.att.net.