Electronic Packaging Research and Education: A Model for the 21st Century

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Next-generation electronic packaging must be consistent with both semiconductors and systems. The packages of the past have been mostly passive containers for semiconductors. Given the need for extremely compact, ultra-low-cost electronic systems for the 21st century, and given that a wafer fabrication plant can cost $1 to $5 billion, what should packaging be in the future? Any packaging technology should also be built upon a knowledge of state-of-the-art packaging. This article proposes highly integrated and low-cost packaging that can improve performance and reduce cost and size by about a factor of 10. It also presents an overview of the next generation in electronic packaging education, called "globally competitive education."
(Keywords: Integrated packaging, Low-cost packaging, Microelectronics, Packaging, Packaging education.)

INTRODUCTION

Dramatic changes are under way in the computer, telecommunications, automotive, and consumer electronics industries. Computing power is doubling every 15 months and will reach 1 billion instructions per second within the next 5 years. In addition, the cost per unit of computing has dropped from $100,000 per million instructions per second (MIPS) with mainframes to less than $10/MIPS with PCs and some workstations. Besides improved performance, computing is increasingly being done with hand-held computers. A similar trend exists in the telecommunications industry (Fig. 1); portable products with voice, image, video, text, and other functions are likely to be commonplace within the next decade. Major changes are expected in the automotive industry as well, both in the electronics content of all automobiles and in the functions needed to support intelligent vehicle highway systems. The common requirements for all of these electronics technologies are (1) ultra-low cost; (2) thin, light, and portable construction; (3) very high performance; and (4) the ability to perform diverse functions using a variety of semiconductor chips.[1]

TRENDS IN SEMICONDUCTOR TECHNOLOGY

Next-generation packaging must be consistent with these needs and with a semiconductor "roadmap" that projects future chip-level developments. This roadmap, which is much more clearly visible than in the past, is directed almost totally toward complementary metal-oxide semiconductor (CMOS) technology. Past

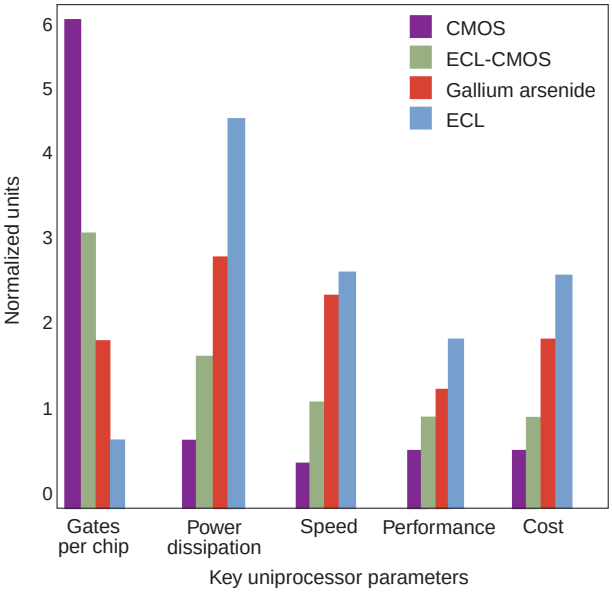

Figure 1. Comparison of semiconductor technologies. (CMOS = complementary metal-oxide semiconductor; ECL = emitter coupled logic.)

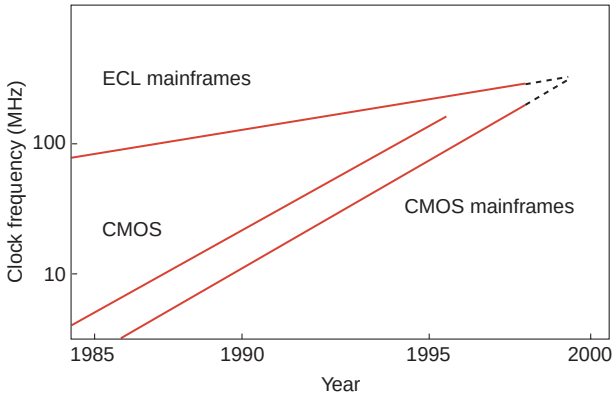

Figure 2. Comparison of the performance of CMOS and ECL technologies, showing how clock speeds of the lower-cost CMOS technology are beginning to approach the levels possible with ECL technology.

practice, in contrast, was generally to use CMOS technology for low-performance applications and emitter coupled logic (ECL) technology for high-performance applications. The reasons for this paradigm shift are illustrated in Fig. 1, which shows how cost and integration are the basis for the use of CMOS technology, and in Fig. 2, which shows how the performance of CMOS integrated circuits (ICs) is beginning to approach that of ECL technology.[2] Figure 3 outlines the trends in semiconductor technology through the year 2000. Similar changes are expected to extend into the next decade. Such a roadmap to the future appears to be technically achievable, although economics is a major concern.

The key question for next-generation packaging is whether it can fill its traditional role of interconnecting, powering, cooling, and protecting semiconductor ICs while also addressing the economic concerns of higher costs for wafer fabrication and for large and fine-line ICs. (Fabrication techniques for large and fine-line ICs invariably produce low yield as well as high cost.) In addition, can the next generation of packaging address tomorrow's needs for ultracompact, portable ICs? This article discusses how some of these challenges are being addressed.

PACKAGING EVOLUTION

Single-Chip Packaging

The overall packaging trend is indicated in Table 1. Packaging has evolved during the last 3 decades, starting with dual-inline packages (DIPs) and wire bond in the 1970s, quad flat packs (QFPs) and surface-mount technologies (SMT) in the 1980s, and ball-grid arrays (BGAs) in the 1990s. There is similar progress in the miniaturization of passive components (Fig. 4) and in organic board fabrication using advances in traditional drilling and lamination technologies, as described later in this article. All of these technologies, however, provide a silicon packaging efficiency of only about

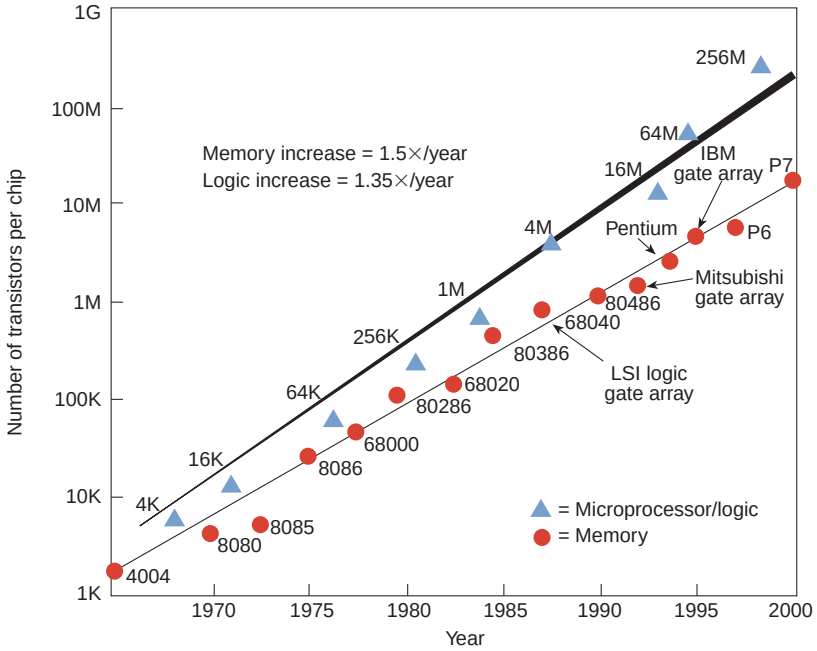

Figure 3. Trends in densities of integrated chips since 1965. Over the next decade, next-generation packaging will support a continuation of the trends shown.

Table 1. Packaging evolution.

	Past		Current		Future
Package	1970s	1980s	1990s	2000	2005
Chip connection	Wire bond	Wire bond	Wire bond	Flip chip	Low cost High I/O Flip chip
Package	DIP	P-QFP	P/C-BGA	CSP	No package
Package assembly	PTH	SMT	BGA–SMT	BGA–SMT DCA-PWB	Direct to board
Passive components	C-discretes	C-discretes	C-discretes	C-discretes	Integrated
Board	Organic	Organic	Organic	Micro-via board	SLIM
Number of levels	3	3	3	1	1
Number of component types	5–10	5–10	5–10	5–10	1
Silicon packaging efficiency, %	2	7	10	25	>75

Note: CSP = chip-scale package; DCA = direct chip attach; DIP = dual-inline package; P/C-BGA = plastic/ceramic ball-grid array; P-QFP = plastic-quad flat pack; PTH = plated through-hole; PWB = printed wiring board; SLIM = single-level integrated module; and SMT = surface-mount technology.

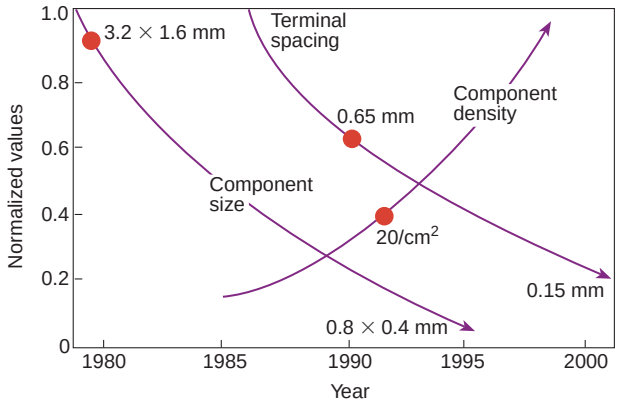

Figure 4. Progress in miniaturization of portable electronic components (source, Hitachi).

10%—a factor of 10 below the theoretically possible on-chip limit. The use of chip-scale packaging (CSP), with packaging no bigger than an IC itself, as well as the use of bare-chip multichip module (MCM) packaging, will raise this efficiency to about 40%, still far from the goal of 100% efficiency.

Table 1 shows that the next generation of packaging is direct chip attachment to an organic board. This technology will use fine-line photolithographically defined wiring and integration of passive and optoelectronic components. These developments are aimed at reducing the number of packaging levels from the current 3 to 1, reducing as many as 5 to 10 types of active and passive components to 1 type, and simultaneously reducing size or improving silicon efficiency by a factor of 5 to 10 (Fig. 5).

Multichip Packaging

Multichip technologies are generally divided into three groups based on ceramic, thin film, and printed wiring board (PWB) technologies. As illustrated in Fig. 6, the wiring density per layer or input/output (I/O) connection density is highest for thin film technology, followed by ceramic, and least for PWB technology. The cost per I/O connection in Fig. 6 is not consistent,

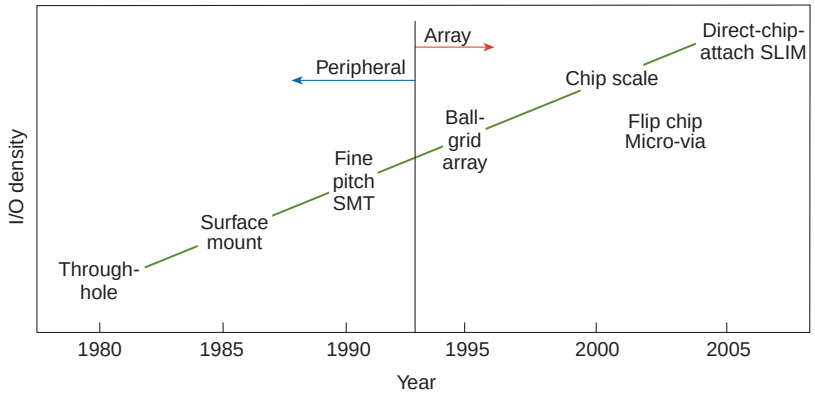

Figure 5. Overall packaging evolution. (Source, Motorola; SMT = surface-mount technology; SLIM = single-level integrated module.)

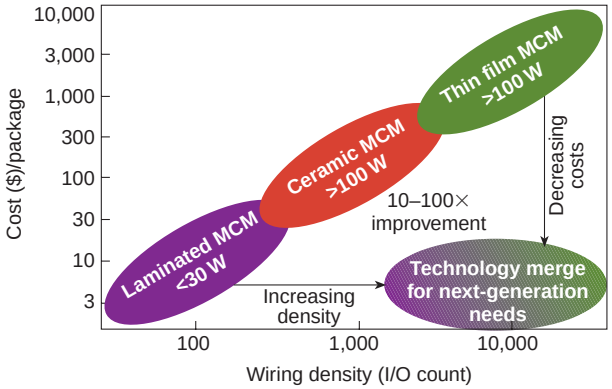

Figure 6. Multichip module (MCM) options, cost per input/output (I/O) connection, and next-generation needs.

however, with the wiring density; cost per I/O connection favors PWB technology as the most appropriate MCM technology. It appears that this technology can be extended with thin films based on large-area processing, combining the best aspects of each into one MCM technology.

NEXT-GENERATION PACKAGING CHALLENGES

The continued progression toward better, cheaper, and faster semiconductors has been most visible in the computer industry. To capitalize on these device advances, a number of packaging limitations are being addressed, at the Georgia Institute of Technology Packaging Research Center (PRC), at other universities, and in industry. This section presents a sampling of the more significant issues. The PRC at Georgia Tech foresees overcoming these challenges with a technical vision for next-generation packaging similar to the vision that has driven the development of ICs: continued integration to ever-higher transistor density while maintaining manufacturing cost at about $4.0/cm^2. This technical vision is illustrated in Fig. 7, which compares next-generation packaging with the current industry standard—QFP to which the IC is wire bonded and the board is surface mounted. The ceramic discrete passive components (called "discretes") are surface mounted to the board as well.

For such applications as cellular telephones, camcorders, or magnetic disk drives, the packaging efficiency (defined as the ratio of the area of all silicon and other ICs to the area of PWBs) is about 8% with this technology. The technical vision of integrating all of these packaging levels into one level with dielectric components, conductors, capacitors, resistors, inductors, and optoelectronics (as waveguides) is projected to raise this efficiency to about 80% (Fig. 8). This improvement is due primarily to two factors: (1) discretes, optoelectronic, and RF components are now embedded in the board and thus take up no additional surface area, and (2) all of the integration and extensive thin film wiring allow ICs to be flip-chip bonded "wall-to-wall" on the board. This integrated board or module can be a single-chip integrated module (SCIM) no

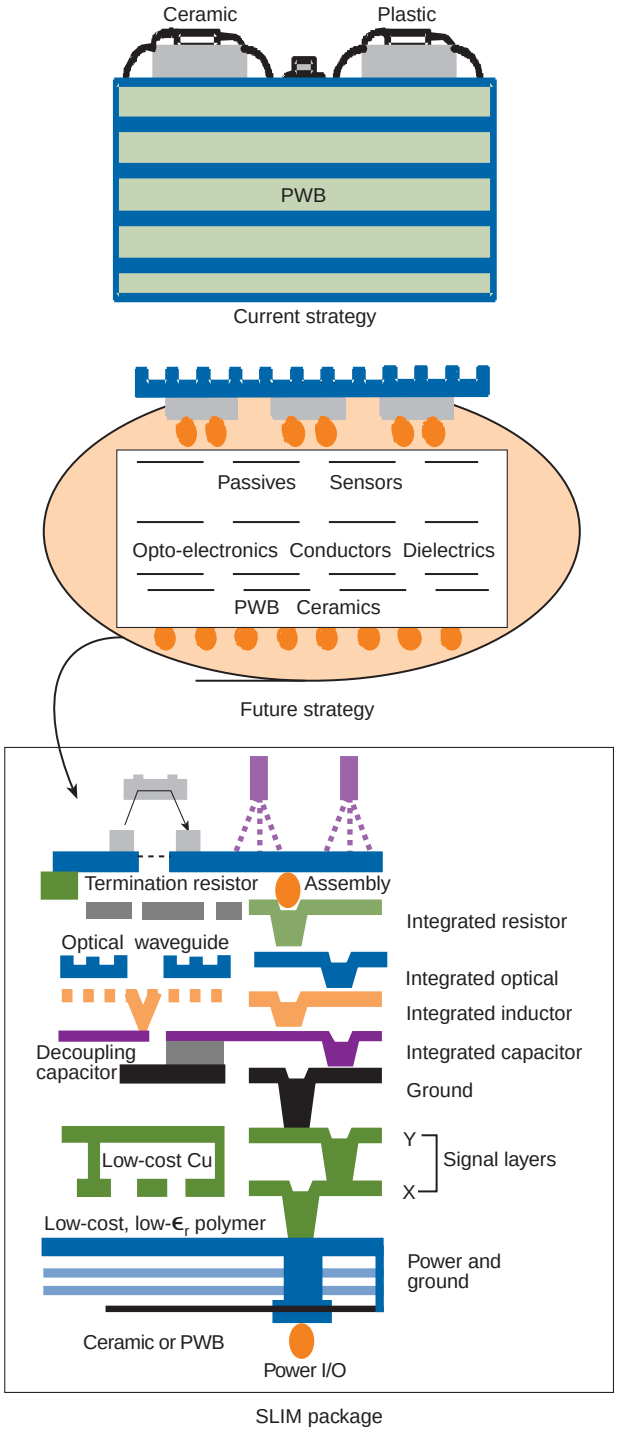

Figure 7. Current packaging technology compared with next-generation packaging. (PWB = printed wiring board; I/O = input/output; ε_r = relative dielectric constant.)

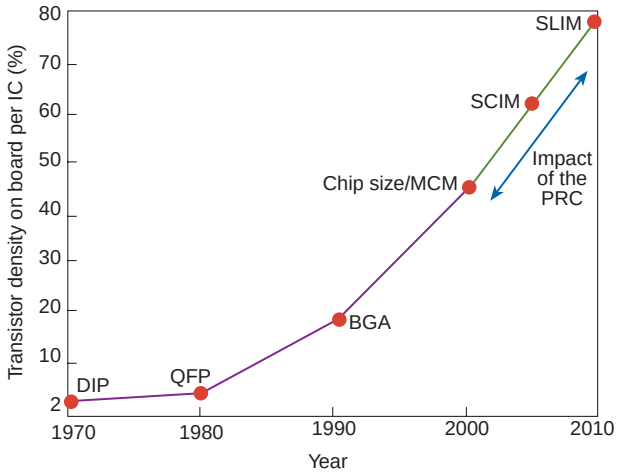

Figure 8. Efficiency of various packaging technologies, showing the goals through 2010. (BGA = ball-grid array; DIP = dual-inline package; MCM = multichip module; PRC = Packaging Research Center of Georgia Tech; QFP = quad flat pack; SCIM = single-chip integrated module; SLIM = single-level integrated module.)

bigger than the IC itself with as many as 5000 I/O connections, or it can be an integrated MCM called a single-level integrated module (SLIM).

Table 2 compares the expected impact of the vision with current packaging, showing its effect on several important technical and financial parameters and highlighting the goal of a 10-fold improvement in size, cost, and performance during the next decade. Table 3 lists the four key system barriers (reliability, integration, cost, and performance) that require major technical breakthroughs and illustrates how PRC expects to address these barriers. The reliability and integration barriers are being overcome by improving packaging efficiency from 8% currently at the single-chip level to 80% with the PRC strategy just described, and by eliminating surface-mounted discrete passive components and integrating optoelectronics (both as waveguides and chip-to-chip free-space interconnections). The cost barrier is being overcome primarily by large-area processing, use of low-cost materials, wet processing, low-cost area array assembly, and low-cost electrical testing. The performance barrier is being overcome by improving the transistor packaging density (as measured by the number of transistors packaged per unit area on the system-level board) as well as by using improved conductors and dielectrics. Diverse functions are handled by custom thin film and passive integration and by local "cooling on demand" with a variety of ICs.

Table 2. Packaging improvements over time.

Variable	Today	6-year goal	11-year goal
Efficiency (Silicon)	8%	40%	80%
Package cost			
Substrate per I/O connection	$0.015	5×	10×
Board (6-layer) per in^2	$1.000	5×	10×
Assembly	$0.020	5×	10×
Test	$0.010	5×	10×
Package performance			
Circuit packaged per cm^2	200	5×	10×
Interconnection delay	Al, Cu high	5×	10×
Memory access	100 MHz	5×	10×
Wireless	900 MHz	5×	10×
Data rate	100 MB/s	5×	10×

Note: × denotes improvement multiple.

Table 3. Strategic research areas for next-generation packaging.

System barriers	Technology barriers	Research areas
Reliability	Thin film, flip-chip/BGA, high-flux air cooling	Low-cost MCM Assembly Thermal management RF research
Integration	Capacitors Optoelectronics Inductors Resistors	Integrated substrate Optoelectronics
Cost	Large-area processing	Intelligent large-area manufacturing
	Low-cost materials/processes	Low-cost MCM
	Low-cost assembly	Assembly
	System-level design/tool	Design, system integration
	Low-cost testing	Testing
Performance	Number of circuits packaged	Design, system integration
	Memory access	System integration
	Bandwidth/data rate	Optoelectronics

Note: BGA = ball-grid array; MCM = microchip module.

RESEARCH ADVANCES

Important advances in packaging have been made in industry and in Georgia Tech's PRC. Examples of significant advances are described in this section.

Thermal Management

With the concentration of heat in highly integrated packages, new ways of managing thermal energy are needed. The PRC's Thermal Management Thrust Group has developed a radically new and highly efficient cooling technology suitable for "on the spot" and "on demand" use on individual chips, MCMs, and electronic packages.[3] This technology is based on dynamic manipulation of miniature single-phase jets using piezoelectric actuators (Fig. 9). The capability to dynamically alter the direction and momentum of these jets promises to supply an effective means for convective cooling of heated surfaces by controlled jet impingement, thereby achieving the ability to remove as much as 10 to 20 W/cm^2, a 5-fold improvement over state-of-the-art capability.

Electrical Testing

To build any circuit in a cost-competitive manner, culling defective parts before expending resources on further integration is crucial to establishing a consistently high final circuit yield. This manufacturing yield enhancement must be reflected in all levels from components to the final circuit or system; thus, testing of all subsystems or parts is particularly important.

One challenge of electronic packaging is that high-density substrates require electrical testing of interconnections before die attachment. Such testing, although currently expensive and at times inaccurate, is needed to examine miniature geometries that may contain hidden defects. The PRC team has invented a new method to test substrates for latent problems such as open and short circuits.[4] This new technique, which uses a coaxial high-quality factor resonator to modulate the response of interconnections, produces a variation in the magnitude and phase of the injected signal on the basis of the defect size and type. This resonator, which is available commercially, helps magnify the response of defects near its resonant frequency, thus allowing the defects to be detected easily. In the past, methods such as capacitance, resistance, electron-beam, electrical module testing, and time domain network analysis were used, but they were either limited in defect detection capability or required expensive hardware. The new method is expected to require small costs in hardware and to increase resolution by an order of magnitude compared with the commonly used capacitance method.

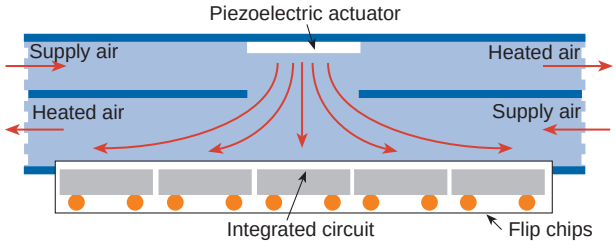

Figure 9. Microject cooling based on dynamic manipulation of miniature single-phase jets using piezoelectric actuators.

Integrated Optoelectronics and Systems Integration

Packaging is a critical factor affecting cost in optoelectronic systems. Currently, submicrometer tolerances on optical fiber and optical free space components are common, resulting in high manufacturing costs. The design of optoelectronic systems that are more tolerant of alignment variances can significantly reduce the overall cost of the system by relaxing the packaging tolerances. Leveraging research supported by the Manufacturing Research Center on such an alignment-tolerant optical interconnection for automotive, avionics, and communications applications, a multidisciplinary team from PRC's System Integration and Low Cost Optoelectronics Thrust Areas has collaborated on a scheme to increase the alignment tolerance of optoelectronic systems through the use of silicon electronics for "smart" optoelectronic interconnections.[5]

The alignment tolerance of the optical package can be optimized by understanding and using the trade-offs that occur in link speed, emitter/detector design and wavelength, interconnection media (plastic versus glass fiber and core diameter), optical loss, amplifier gain, and error correction coding. This technology offers several advantages over wire-based interconnections, including reduced electromagnetic interference emission and susceptibility; reduced weight, size, and operating power; and improved design flexibility. Georgia Tech is among the research centers working on practical, tolerant optical interconnections under both internal and federal funding.

Wireless Electronics

The field of wireless electronics is visible and economically significant. Progress depends heavily on advances in packaging materials and test methods, particularly those that address heat management and effective and practical high-frequency test methods, all within an environment that is literally shrinking. A Georgia Tech team is working toward developing a nondestructive technique for characterizing materials and buried structure. This team has created a prototype probe[6] (Fig. 10) in collaboration with Cascade Microtech, a commercial electrical test hardware vendor. The

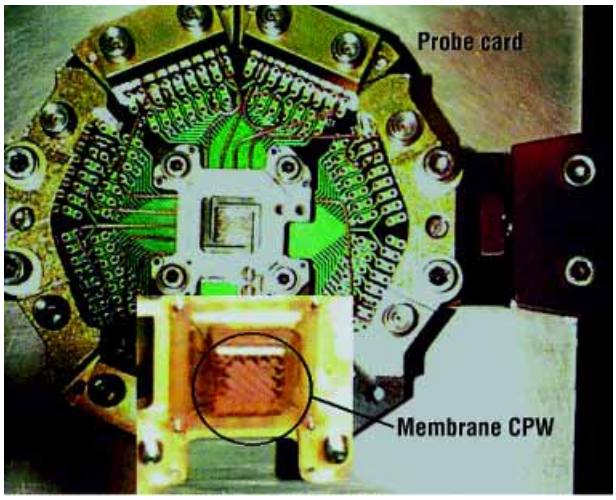

Figure 10. Prototype membrane probe for nondestructive characterization of materials and buried structure (CPW = coplanar waveguide).

probe is currently being tested for potential market use. This team also is helping to develop membrane probe technology,[6] a rapidly growing application area that represents a potentially significant breakthrough in the nondestructive characterization of thin film material structures. No alternative exists today, and this technology may be applicable to electronic materials as well as to packages.

Low-Cost MCM Technology

Crucial to the acceptance of advanced electronics technologies is the development of novel materials that are better and cheaper than those they replace. In partnership with BF Goodrich, a Georgia Tech Low-Cost MCM Research Team is developing a new class of packaging materials derived from polymers of cyclic olefins. These polymers have unique properties. They are characterized by glass transition temperatures greater than 350°C, a dielectric constant of about 2.5, characteristically low moisture absorption of 0.1%, and good ductility.[7] They have been modified to have excellent adhesion to common substrate materials such as silica and aluminum; they fuse well with copper and noble metals such as gold and silver; and they have been shown to adhere without an adhesion promoter or adhesion layer (e.g., titanium, tantalum, or chromium), thus remaining adherent films even after being placed in boiling water for 2 h. These materials are expected to demonstrate utility for both semiconductors and packaging by offering superior performance over traditional materials while reducing the device manufacturing cost.

Intelligent Large-Area Manufacturing

The primary goal of PRC's Intelligent Large-Area Manufacturing Research Team is to achieve high-yield manufacturing on large integrated substrates consistent with a 10- to 100-fold cost reduction. Maximizing yield involves monitoring, modeling, and controlling each of the key integrated fabrication steps: polymer deposition, formation of vias, photolithography, and metallization. During PRC's first year, this research team developed a real-time, neural network–based feedback control scheme for a general class of manufacturing processes. This approach involves process modeling with neural networks, control schemes based on parameter estimation by means of Kalman filtering, nonlinear function inversion based on reverse neural network structures, and block-form prediction. This scheme will be applied to the control of polymer deposition by extrusion or meniscus coating and reactive ion etching (RIE) in MCM via formation. It will control the process during a given run, a significant contribution to the state of the art.

The efficacy of this approach has been demonstrated: experimental I/O data from an RIE process were used to examine the run-by-run control of a multiple-input, single-output system, and real-time, block-predictive control of a dynamic process reflecting typical RIE behavior was achieved. This work is based on recent breakthroughs in nonlinear filtering that make it possible to consider neural network models of manufacturing processes.[8]

Integrated Passive Parts

Passive parts—inductors, capacitors, and resistors—have long consumed a substantial percentage of the area needed for building a circuit. Capacitors in particular typically consume considerable area. A major technical breakthrough was achieved in polymer–ceramic composite films for capacitor applications for MCM-L. Based on a dielectric constant of 65 and a dissipation factor below 0.05, specific capacitance as high as 22 nF/cm^2 has been attained (Fig. 11). This achievement is being explored for incorporation into wireless products. The polymer used in these composites is typically polyimide or BCB (benzo-cyclo-butene) epoxy, and the ceramic is either lead–magnesium niobate or barium–strontium titanate.[9]

ELECTRONIC PACKAGING EDUCATION IN THE 21ST CENTURY

Clearly, the economic and technical importance of electronic packaging has greatly increased. Up to now, technical professionals working in packaging have "grown up" in the field by learning on the job. Such a means of developing professional expertise is no longer adequate. Packaging draws from the fields of electrical engineering, materials, mechanics, physics, and chemistry, and it requires that these disciplines be

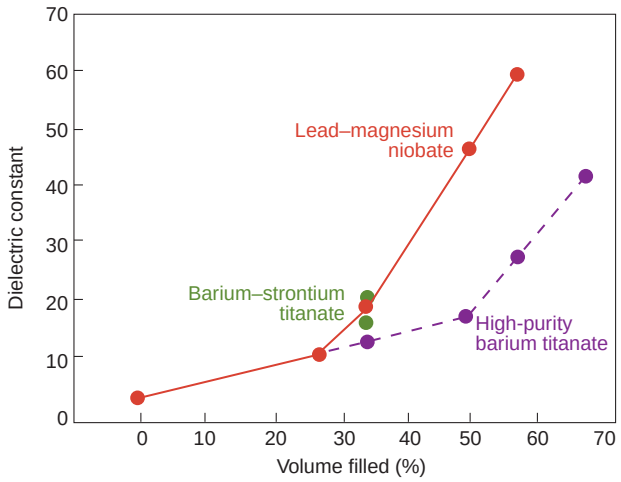

Figure 11. Dielectric constant of polymer–ceramic composites.

integrated to address specific system needs methodically. Haphazard preparation for such endeavors is simply inadequate. As part of the answer to this dilemma, Georgia Tech is among the first institutions to address systematic training of personnel for professions across the various fields of electronic packaging. This section illustrates the motivation and methods being implemented at Georgia Tech's PRC to address training of multidisciplinary packaging professionals.

The Educational Need

Dramatic changes are required in both technology and human skills to support the expected growth of the electronics industry from $800 billion today to $2 trillion in 2004. The U.S. market share of this total is likely to be only 40%; significant fractions of future growth are expected from overseas, making globally competitive education in the 21st century a necessity. Figure 12 illustrates some of the critical elements of this global education identified in a PRC survey of its industry members.

The Educational Vision of PRC

The vision of PRC is to be the recognized leader in electronic packaging education and to have a national impact on both the number of people educated and the global quality of their education. To achieve this vision, PRC involves undergraduate and graduate students, as well as industry professionals, in setting up a pipeline of top-notch electronic packaging students. PRC is also embarking on precollege education of students and teachers. To have a national impact, PRC involves undergraduate and graduate students from other universities, as well as selected unique faculty from the United States and abroad. As part of PRC's outreach beyond the university environment, professional engineers from throughout the industry actively participate in advanced technology workshops where emerging next-generation technologies are debated and discussed and problems are resolved.

Educational Strategy

The strategy to achieve the vision is indicated in Fig. 13, which shows four broad categories: precollege, undergraduate, graduate, and industry professionals. The strategic elements that PRC has chosen to focus on in each of these four categories are identified in this figure. The accomplishments to date and strategy for the next 5 years are described in the following paragraphs.

Undergraduate and Graduate Education

A pyramid approach to education for both graduate and undergraduate students is being pursued (Fig. 14). It involves numerous fundamental courses related to packaging that are offered by each of seven participating schools. These courses, typically discipline oriented, form the base of the pyramid, and most of them existed at the start of the PRC. To transfer the latest PRC research into education, numerous courses, covering every PRC thrust, were either newly developed or significantly modified. Since every thrust is cross-disciplinary, involving science and engineering and drawing on faculty from more than one school, these are cross-disciplinary courses. The courses (more than 20 undergraduate and 20 graduate) form the middle of

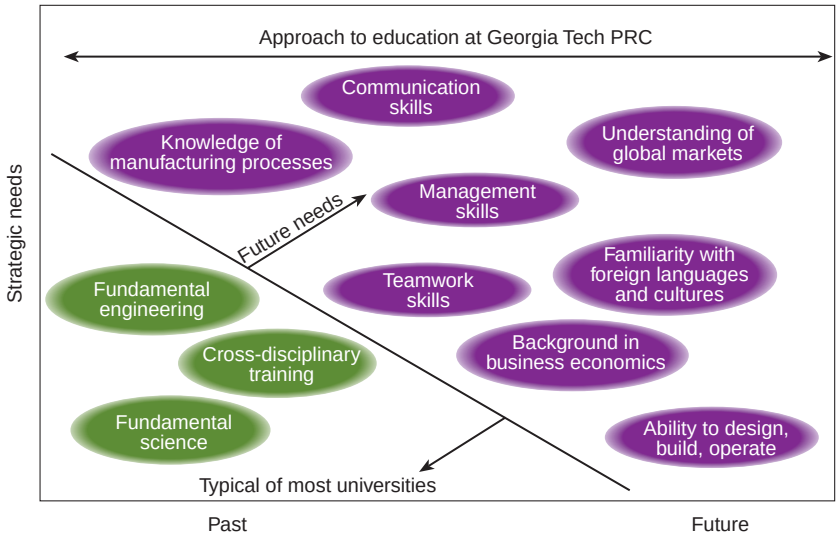

Figure 12. Educational needs of the electronic packaging engineer in the 21st century.

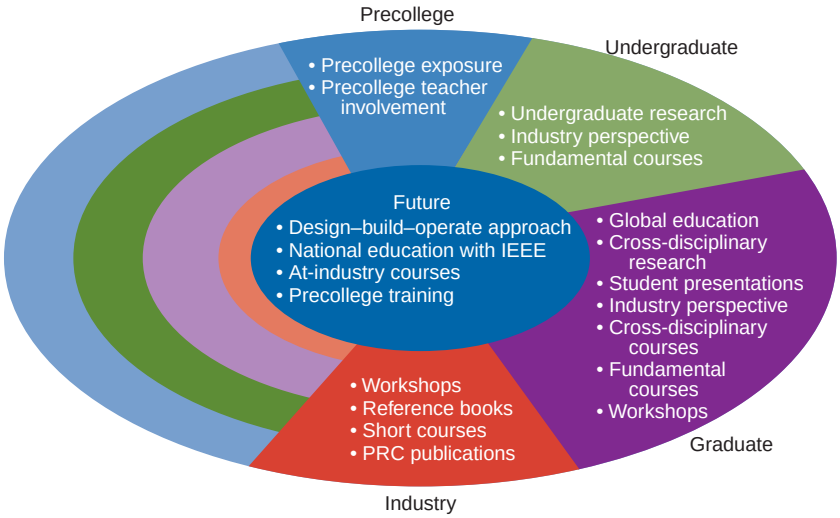

Figure 13. Educational strategy of the PRC at Georgia Tech.

the pyramid. For the pyramid's apex, system-level courses involving most or all PRC areas were developed. One undergraduate course (Electronic packaging systems) and two graduate courses (Industry needs vs. technology challenges and Low-cost integrated packaging) fall into this category.

Industry perspective for undergraduates. Providing an early career industry perspective for undergraduates is a high priority in professional development. Students can achieve this perspective by serving as industry interns, working in cooperative programs, and serving as research students with a mentor from industry, either on campus or at a company. At PRC in recent years, five undergraduates participated in co-op programs, four served as interns, and six had on-campus industry mentors.

Undergraduate research. Because of the PRC focus on undergraduate research, the number of undergraduates involved in research has jumped to 114 students, in addition to 9 undergraduates from other universities. Every PRC faculty member has one or more undergraduates involved as part of the research team, with graduate students directing undergraduates. In some instances industry engineers provide the direction. To pick those students having the needed cross-disciplinary interests, the education committee has implemented a systematic and effective process for the selection of undergraduates for research involvement.

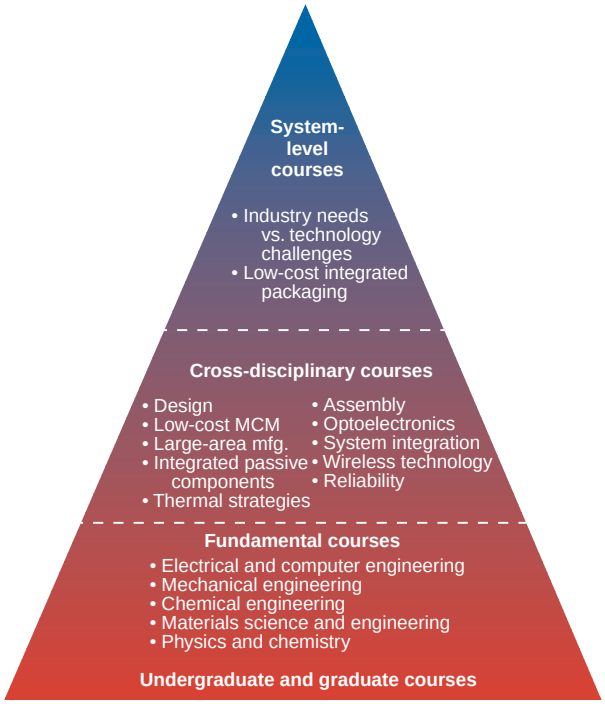

Figure 14. Undergraduate and graduate course strategies for electronic packaging education.

Graduate education. The focus of graduate education at PRC includes fundamental, cross-disciplinary, and system-level courses; advanced technology workshops where students are exposed to an industry perspective; internships and co-ops; a Distinguished Industry Lecture Seminar; and global education through the Global Innovation for Engineers (GIE) Program.

Industry perspective for graduate students. Georgia Tech has long had an outstanding program that incorporates students' industry co-op experiences as an essential element of engineering education. PRC has sought to build upon its experience to maintain the close coupling of classroom work and industry work by developing both co-op and internship opportunities for PRC graduate students. An additional aspect of this area is the establishment of co-op positions on campus, in which the student works on a member company's research and reports to the company staff. The graduate internship and co-op program has grown substantially: 5 students in the first year, 19 in the second year, and 54 in the third year. The Distinguished Industry Lecture Seminar series also emphasizes the industry perspective.

Global education. The pioneering GIE Program was started by Georgia Tech to provide global education. Its mission is to educate engineers and computer scientists in the 21st century to thrive in global electronics companies. This program combines a master's degree in engineering or computer science with an expanded minor in management and international studies, including foreign language, and a 6-month internship at an international site. A special curriculum has been created to train engineers in business economics

and management, as well as in engineering. The first class is currently engaged in their internships. The following companies support these interns in Europe and Asia:

ALCATEL, Toulouse, France
Ericsson, Stockholm, Sweden
Frauenhofer Institut, Germany
Motorola, Germany
Motorola, Sichuan, China
Proctor & Gamble, Rome, Italy
Schlumberger, Munich, Germany
Schlumberger, Paris, France
Silicon Graphics, Switzerland
Telecommunications Co., Lorraine, France

Cross-disciplinary research and student presentations. Cross-disciplinary education at PRC is being achieved by two other means. Eleven cross-disciplinary teams involving two or more graduate and undergraduate students are learning across their disciplines by means of research activities. In addition, monthly student presentations provide a forum for student teams to present their research to each other and to discuss their findings and the relationship of those findings to PRC research overall.

Education and Advanced Professional Development for Packaging Professionals

The ever-increasing rate of technological advance in the electronic packaging field makes life-long learning a necessity for the practicing engineer. PRC is supporting the engineering community through a variety of activities targeted at both member and nonmember companies to achieve life-long learning. These activities include PRC publications, advanced technology workshops, and short courses.

To reach packaging professionals in more advanced career stages, members of PRC either have taken a leading role or are participating in a number of national and international workshops, conferences, and global education courses. Examples of topics include the many issues involved in the development of SLIM technology. The base substrate was addressed in a PRC-created materials conference with the Institute of Electrical and Electronics Engineers (IEEE), the International Microelectronics and Packaging Society (IMAPS), and four other materials societies; MCM dielectrics and conductors were addressed in the workshops with IMAPS on low-cost packaging and on MCM-L/D. Workshops have also been held on integrated passive components, next-generation flip-chip technology, next-generation design, and next-generation RF, electrical testing, and thermal technologies. Each workshop lasts 2.5 days, and attendance is typically 70 industry professionals and faculty members from throughout the United States, the Far East, and Europe.

Publications

Indisputably, access to and dissemination of information are increasingly crucial to career-long professionals in packaging, as in most engineering fields. PRC believes that publishing the findings of research is a major means of educating the community of practicing engineers. Over the 3 years of PRC's existence, the faculty has produced 479 articles in refereed journals and proceedings, making the Georgia Tech PRC the largest producer of publications on electronic packaging in the United States. In addition, 14 faculty members contributed chapters to or authored books in areas associated with packaging. These books and articles serve as the state-of-the-art reference material in electronic packaging and are a valuable aid in educating industry and graduate students. The opportunity to publish their work and to participate in professional societies continues to be a necessary part of student professional development.

In addition, the author and 9 members of the PRC faculty, together with 61 other authors from around the world, recently produced a comprehensive, three-volume work on state-of-the-art electronic packaging, *The Microelectronics Packaging Handbook*.[10] It provides the latest information on all aspects of system-level packaging.

Finally, PRC has been active in disseminating its findings using short courses, such as those previously noted, conducted in conjunction with major conferences and meetings. These short courses, conducted by PRC faculty and attended by both industry and academic professionals, have covered almost all of the research areas involved in the development of SLIM technology and have drawn more than 750 attendees. Such short courses are an integral part of continuing education in packaging.

Future Vision for Learning

With the field of packaging changing so quickly, training methods must similarly change to reflect the way packaging engineers learn and function. This means moving from individual and local efforts to the globally oriented team efforts needed in the current and future electronics economy. As in other technological professions, learning will continue throughout the professional life through formal education, topical workshops, publications, and the like. Formal education has been restructured at Georgia Tech to conform to this need. Plans are being implemented that will continue adapting education to the broad and global roles of future packaging professionals. For example, few research universities have considered venturing into the realm of developing system-level prototypes, an area that has traditionally been the sole responsibility of private industry. Thus, while universities have concentrated on novel

concepts, explored technologies, and published journal papers, companies have done their own exploration and subsequently focused on manufacturing. There has been a major gap between the two and, for the most part, the novel concepts of universities have not ended up in the marketplace.

PRC aims to correct both technology and education deficiencies by a revolutionary new approach: design–build–operate (DBO) research and education. The planned project involves two fronts: (1) research advances toward the next generation of highly integrated single-level packaging (SLIM technology); and (2) education of teams of students, both graduate and undergraduate, in cross-disciplinary, system-level, next-generation prototypes from concept to design, development, test, and operation of systems. PRC expects to achieve both of these advances in the two advanced packaging system prototype facilities recently completed at a total cost of $28M; one will be for large-area (300-mm) integrated substrates and the other for interconnect test, flip-chip assembly, underfill processing, thermal management, and reliability. The DBO approach to education, accordingly, will involve a hands-on course on next-generation substrates that will include electrical design; fabrication of substrates consisting of conductors, dielectric components, resistors, capacitors, and inductors; and electrical testing of these products. We expect about 30 students to be involved annually. The program will have a separate hands-on course in next-generation module technology involving flip-chip assembly, functional testing, reliability, and thermal management.

As the field and profession change, learning is also changing. Without bold, unique advances in education, packaging professionals will be unprepared to capitalize on rapid advances in electronics technology. With such innovation in both the technology and the process of learning and communicating the technology, our society will be able to reap the benefits from development of these next-generation technologies.

SUMMARY

A technical vision for next-generation electronic packaging that reaches beyond MCM, flip-chip, and chip-scale packaging is proposed. This vision is based on highly integrated single-level packaging that offers 10-fold improvements in the cost, size, performance, and reliability of electronics products. A similar vision for educating students as globally competitive engineers is proposed, with strong fundamental science and cross-disciplinary engineering knowledge as well as system-level training in manufacturing, business economics, and foreign language and culture.

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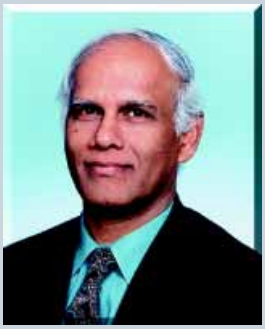

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