System-Level Packaging: Putting It All Together

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Electronic packaging at APL is radically different today than it was in the past. Limited funding, shorter schedules, packaging densities, and higher power requirements place an entirely new set of criteria on the packaging designs. New processes and fabrication techniques are evolving faster than the established reliability framework can support. Electronic packaging design involves many separate elements and disciplines. Streamlining the design process requires that these separate disciplines be integrated into a common effort via concurrent engineering.
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INTRODUCTION

APL continues to meet the challenges imposed by its customers through the creation of innovative solutions to complex problems. Many of these solutions involve the development of highly complex electronic systems. The Laboratory designs, fabricates, assembles, and tests much of the hardware it uses internally. This internal production capability gives us a significant advantage in how we can approach problems. Proven and reliable processes exist, as well as newer and developmental ones. Having a greater flexibility in the design and fabrication process will let us adapt quickly to evolving aerospace hardware requirements while maintaining our traditional quality.

At the heart of an electronic system is the design process that creates it. This process consists of a variety of engineering disciplines that design, fabricate, and assemble the unit. As electronic designs become more complex, the implementation of these designs is tied more closely to the fabrication system. Software, equipment, and processes are coupled to produce reliable products within the limits of the system.

Continuous development of new technologies and processes is required to maintain our competitive advantage. Many of the advances in electronics involve new types of packages. The development of chip-scale packages, multichip modules (MCM), and chip-on-board (COB) packaging is aimed at miniaturizing the overall system.[1] The use of ball-grid array devices and plastic-encapsulated parts promises the availability of a wider variety of components for space and military use. These new parts provide more flexibility in the electronic design, but place more requirements on the packaging design. All these new devices present design and fabrication process challenges.

At APL, the electromechanical package design staff is responsible for developing new, complex electronic

systems. Included in this responsibility is the need to understand our existing capabilities and to prepare for those of the future. Integrating new technologies, new package types, and new processes into our existing system requires a clear view of where we are going and how we expect to get there.

DESIGN

Overview

The electromechanical packaging effort encompasses many disciplines throughout the design and fabrication process, from initial design through delivery of the electronic systems. Functional responsibilities include both design of flight hardware and development of reliable processes. Although the design, fabrication, and assembly of modern electronics require continuous innovation, the design of reliable systems also requires practice and repetition. It is the overall goal of the electromechanical design effort to implement new technologies to retain the historic quality of APL electronic systems.

The package engineering function has evolved from the need for combining new design and fabrication tools into the development of modern electronics systems. Design and manufacturing processes are becoming more specialized and complex. Interactive software systems connect different steps in the process, and miniaturization drives process developments that are specific to certain technologies. Although an organization cannot be expert in every technology, it must incorporate appropriate new ideas to maintain its competitiveness. Packaging engineering is becoming an essential element in APL's development of these many new electronic technologies and directions.

System Partitioning

Both the electrical and mechanical designs must be addressed in the initial stages of development. System partitioning defines the general mechanical configuration. Important factors in this partitioning are the relative compatibility and physical layout of the subassemblies. Power distribution, signal flow, and electromagnetic compatibility are major drivers in the electrical system layout. Weight, size, connector type, connector location, and board mounting are the major drivers for the mechanical system.

Appropriate partitioning is critical in meeting the overall performance requirements. Systems are divided into the functional blocks that become the electrical subassemblies. The system partitioning for the IR&D Integrated Electronics Module (IEM) demonstration effort is shown in Fig. 1.[2,3] Whereas the different blocks do not necessarily represent different hardware components, they do represent different functions. It is to be expected that functional differences play an important part in the physical layout of the system.

Packaging

Fabrication, assembly, maintainability, quality, and reliability assurance constraints all have to be integrated into the package design. The first step in the electromechanical package design effort is choosing the proper technology for the project. Constraints are imposed based on the cost, schedule, and hardware requirements of the program. Various configurations are available to meet the given problem. The selection and application of appropriate technologies are fundamental to meeting the system specifications.

Because of the complexity of electromechanical packaging technology, it is usually broken down into five hierarchical levels. These levels range from integrated circuits (level 0) to the units or subassemblies such as the chassis enclosure, module, or housing (level 4). Understanding the various levels of electromechanical packaging allows the system hardware designer to apply the proper technology to satisfy the given performance criteria. System performance ultimately depends on the ability of the hardware to operate in the defined environment. Structural, thermal, and radiation environments may be defined. Electromagnetic interference may be self-induced or come from neighboring systems. Mean-time-to-failure requirements are driven by end-item system expectations.

The various "breadboards" or the initial circuit design schematics must be integrated with the associated hardware. After initial partitioning is determined by the system or subsystem engineer, the packaging engineer will start the hardware definition and documentation trees associated with the final version. The work breakdown structure is defined, and all the components, substrates, interconnects, housings, chassis, etc., are identified.

Electromechanical packaging also involves system hardware integration on the platform where it is mounted. Weight and size parameters must be considered. Selecting the appropriate packaging technology to apply at this stage is vital in the design. The simplest electronic circuit requiring resistors and capacitors, to the very complex application-specific integrated circuits (ASIC) with their fine pitch interconnects, can present a packaging challenge.

Mechanical Design

The mechanical design effort defines the overall system packaging. System requirements are important in the early stage of the design process. Size, shape,

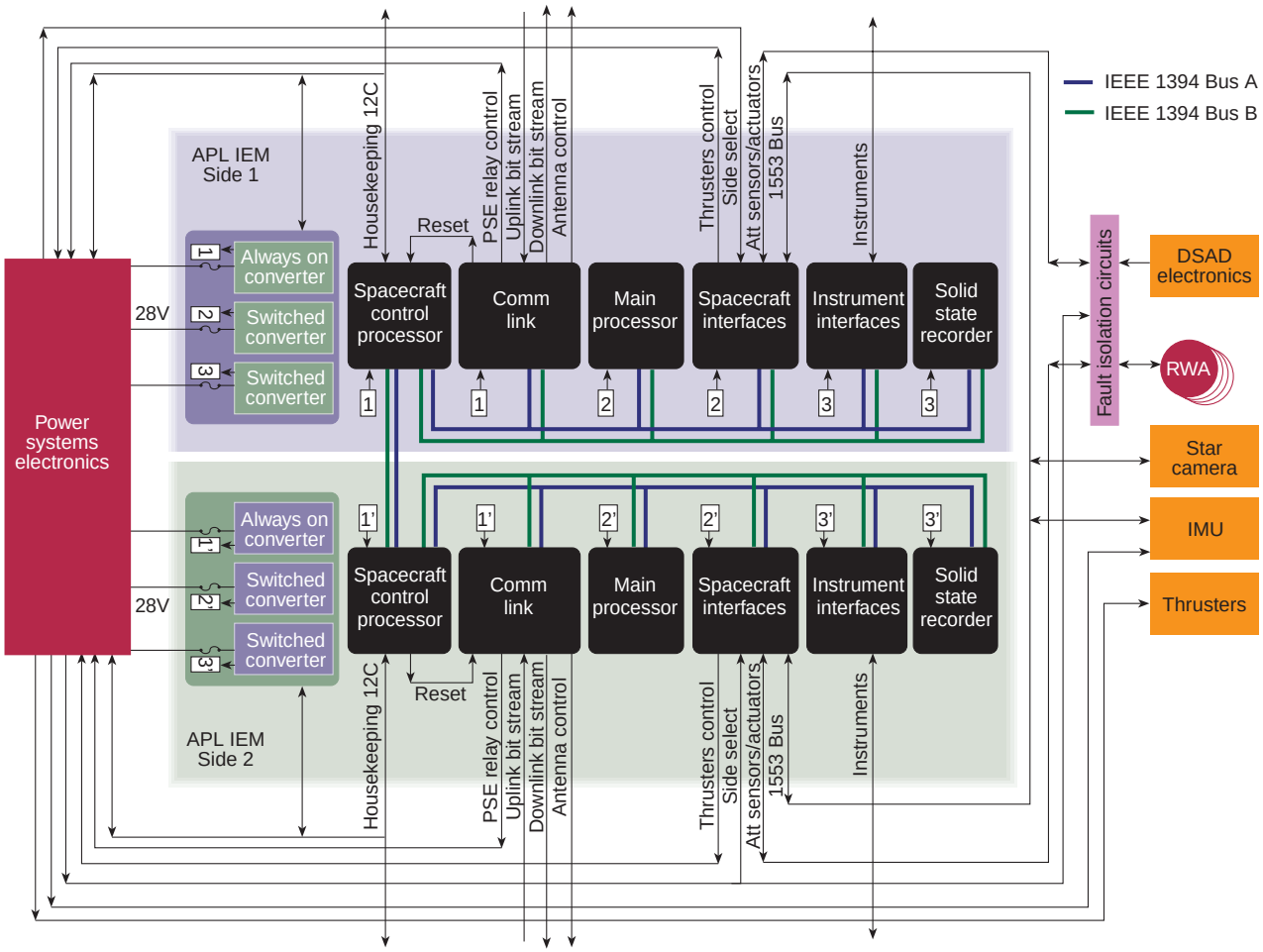


Figure 1. Integrated Electronics Module (IEM) block diagram (PSE = power switching electronics, DSAD = digital solar attitude detector, RWA = reaction wheel assembly, IMU = inertial measurement unit).

weight, cost, and schedule are all involved in the decisions about what technology to use and how to implement it. Performance requirements can constrain the placement of components, but the pieces still need to fit together. Many later design requirements result from how the system is mechanically partitioned.

Mechanical partitioning drives the designs for units and subassemblies. Unit envelopes and initial layouts are developed first. The detailed packaging effort begins after envelope definition and subassembly identification. Once the envelope is defined, the packaging engineer works to use the space available for the electronics while keeping in mind maintainability, modularity, and assembly. Next, interface control drawings (ICDs) are created to communicate outlines and interface requirements to the circuit board designer and the unit's system engineer. The mechanical partitioning of the Near Earth Asteroid Rendezvous (NEAR) Command and Telemetry Processor Unit is shown in Fig. 9 of the article by Bevan and Romenesko, this issue. Note that the mechanical layout determines circuit board size, interconnections, connector placement, as well as the overall footprint of the system.

Several design software packages are used for modeling, simulation, and mechanical detailing of these units. The mechanical design package used at APL is called Pro-Engineer (Pro-E), a product of Parametric Technology. Pro-E is a three-dimensional solid modeling tool that is used to develop the mechanical structure of the units and their related subassemblies. This software contains various programming tools that are used throughout the design and fabrication process. These tools support structural and thermal analyses from the mechanical database and provide the programming support needed for numerically controlled machining. The design database is associative, that is, modifications made to either the assembly model or to a component part drawing automatically update the entire associated documentation package. Database transfer capability has proven to be successful in developing the numerical control programming associated with machining and forming processes.

Electrical Design

The electrical design team is responsible for the design and fabrication of the printed wiring boards (PWBs). The design process for an electrical subassembly, such as a PWB, requires both electrical and mechanical inputs. Mechanical inputs are provided through an ICD that defines outlines, associated keepout areas, tooling holes, stiffeners, and connector interfaces. The electrical design inputs are provided through the preliminary electrical parts list (PEPL) and detailed electrical schematics. The PEPL defines which parts are to be used. The technology associated with the chosen parts must be compatible with the overall program requirements. Parts types and technologies are also reflected in the schematic. Once the preliminary schematic has been developed, the design process begins.

As with the mechanical effort, many software packages are used in the electrical design process. The electrical design package most widely used at APL is Board Station, supplied by Mentor Graphics. This software is used to lay out the printed circuits and components of the PWB. It incorporates an extensive standardized library of electrical parts, which includes the part numbers, symbols, and geometric shapes that are used in an electrical schematic. Mentor Graphics software also allows the circuit engineers to simulate the performance of their designs. In addition, it supports the use of hybrid packages, MCMs, and COB designs with additional modular tools.

The electrical designers work with the circuit engineers to develop the final schematic and fabrication drawings. First, a comprehensive parts list is generated from the PEPL. Working with the circuit engineer, the designer then creates the PWB database by calling the required parts from the library. The electrical parts list (EPL) is automatically generated for the circuit schematic by the software. The circuit engineer then checks the schematic and EPL. After any modifications are incorporated and final approval is given, the layout designer starts component placement on the substrate. An initial area study is done to establish functional groupings. The structural and thermal considerations are incorporated into the design process at this stage. These considerations are made based on power dissipation estimates and component package styles.

Typical design layout and assembly drawings that were developed for the NEAR/RTX PWB are shown in Figs. 2a and b, respectively. Figure 2a shows the electrical connections that are important in determining the component placement. The board design is checked at this stage for compliance with the governing military or other standards. The final PWB configuration (Fig. 2b) is used in board stress and thermal analyses and to generate the fabrication control files. Those files are verified for their compatibility with fabrication processes at APL. The fabrication file generates the drill-and-trim database and the material deposition thicknesses for plating.

DESIGN REVIEW PROCESS

The design process requires formal checks at critical points of the engineering and fabrication efforts. These checks are required by the program office as well as the Technical Services Department's Engineering Design and Fabrication (EDF) facility.[4] Typically, preliminary design reviews and critical design reviews are required by the sponsoring organization. The EDF

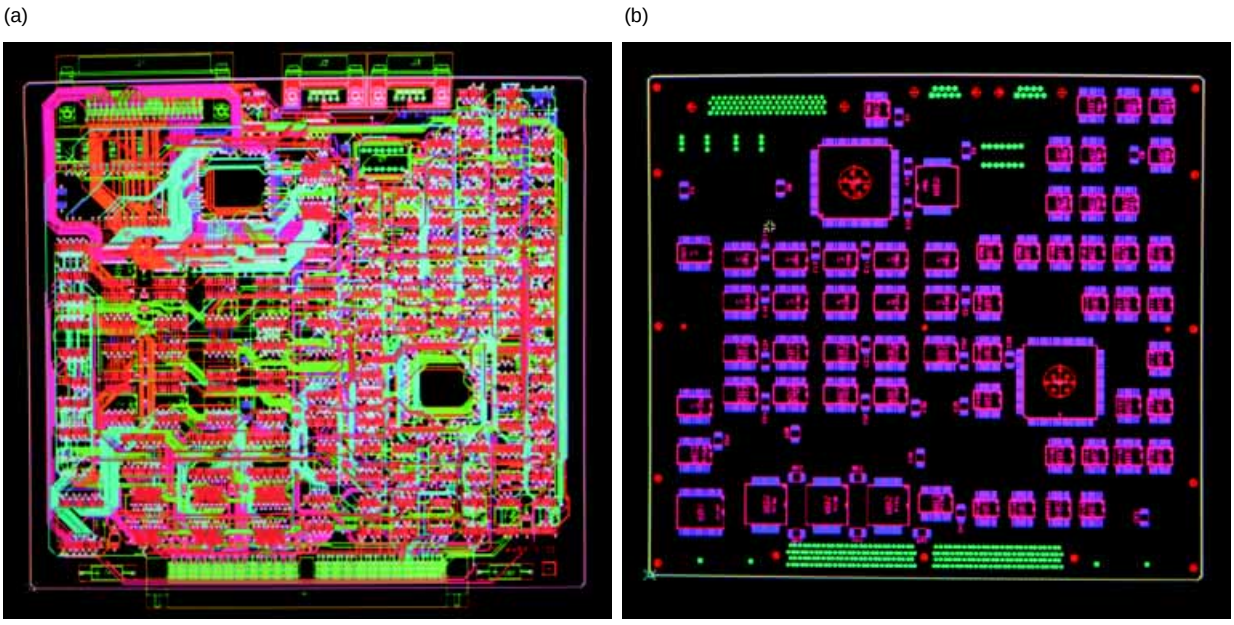


Figure 2. NEAR/RTX processor PWB (a) circuit layout drawing and (b) assembly drawing.

facility also uses internal reviews at specific points in the fabrication and assembly flow. Usually, two reviews are performed in the process of approving a design for fabrication: the interim fabrication feasibility review (IFFR) and the fabrication feasibility review (FFR).

Interim Fabrication Feasibility Review

The IFFR is used to assess the conceptual design in terms of the complete design, fabrication, and assembly process. Before the detailed work begins, the packaging engineer presents the project concept to a team of people from the diverse technical disciplines required by the design. Typically, this team consists of engineers representing thermal design, mechanical design, packaging design, substrate fabrication, assembly, and reliability. In addition, the layout designer and electronic circuit engineer attend the review. If possible, a parts procurement representative will also attend. Clearly, all these disciplines contribute to making successful design possible. For instance, the availability of parts in proper packages may significantly impact the design and schedule.

The initial concept usually remains intact, with specific additions and subtractions recommended by reviewers from their particular areas of responsibility. However, sometimes engineers from different disciplines will disagree on a design concept. For example, thermal constraints may require that high-powered parts be located near the edge of the assembly, while performance constraints dictate their position be in the center. The design may result in a PWB fabrication that will not meet the standards imposed on it by the sponsor.

Other similar difficulties commonly arise. One discipline's efforts to correct a problem can create new difficulties in another, e.g., moving the hot part to the edge of the board may create a signal flow issue for the layout designer or the electronic circuit engineer. Therefore, the entire team is required to resolve the difficulty. The solution may still be problematic for one or more of the disciplines. If the perceived difficulty is resolvable by experimentation or invention within cost and schedule boundaries, the team may elect to take the risk and proceed.

Several notable new processes have been developed after engineering teams decided that some risk was necessary to meet the requirements of specific projects or systems. For example, when it became obvious that considerable increases in circuit density were required, a process for fabricating multilayer PWBs that met the military specification for high-reliability applications was developed. In another instance, the Midcourse Space Experiment program had a requirement to dissipate large quantities of heat via conduction from PWB-mounted components to the walls of the chassis. All existing methods proved inadequate, so a process for laminating metal heat sinks to PWBs was developed and proven. This heat sink design was used for all ensuing spacecraft projects as well.

Because of ever-increasing density requirements and parts availability issues, processes are being developed to perform high-reliability mass reflow soldering of double-sided assemblies laminated onto thick metal heat sinks. Precision forming and trimming of the leads of surface-mounted integrated circuit packages were needed to provide the required densities on several recent programs.

Fabrication Feasibility Review

The FFR is a structured review held when the subassembly is near the end of the design phase and entering the documentation phase. Typically, this review is held just before the start of fabrication and involves all the disciplines mentioned for the IFFR. It includes the final design drawings and verifies that the actions from the IFFR are addressed and discrepancies are resolved. Although the FFR serves as a review of the previous IFFR, more formal documentation is presented. The PWB is given a design rule check (DRC) where the database is reviewed via software for compliance with various standards and requirements of the government, sponsor, or in-house fabrication processes.

Final Review

During the final review, the fabrication drawings presented during the FFR are approved and documentation is signed. The formal release of the drawings initiates the fabrication and assembly phase. The release signature on the documentation designates responsibility for the various engineering disciplines required. In most cases, at drawing sign-off, the documentation control phase of the program begins, as addressed in the Technical Services Department's (TSD's) Standard Specification No. 400.1, Rev. 2. The drawings are then released so that the fabrication process can begin.

FABRICATION

By this stage, the TSD Electronic Services Group has established a team consisting of representatives of the disciplines involved in hardware production. These project teams meet regularly, and include the electronic circuit engineer and a mechanical design representative. In many cases, the systems engineer and program manager attend these meetings. Discussions include the status, quantity requirements, and schedule for the various subassemblies. Process planning, timely rescheduling, and maximization of the various scenarios

for the customer's benefit are ongoing throughout the program. The team leader provides the customer and program office with updates on status, schedule adjustments, work requests, and other program elements.

Panelization, Lamination, and Drilling

The PWB fabrication area receives documentation from electrical design by the release mechanism, and various electronic databases by the network for the fabrication. The DRC is used again to verify the PWB's compliance with the various standards. Panelization or duplication of the PWB onto a standard PWB panel (typically 12 × 18 in. or 18 × 24 in.) is performed. When possible, at least two PWBs are placed on a panel along with cross-section test coupons. These coupons are used to verify the process and quality of the PWB. Photoplotting is generated via the database from the computer-aided manufacturing software. These photoplots are used in the layup of the layers that comprise the multilayered PWB.

Photolithography, the process of transferring the film's image from the emulsions to the PWB panel, is accomplished via photoresist or photosensitive material. The image is then laminated to the panel with heat and pressure, with targets for registration between layers.

Databases for the drill-and-trim effort are also automated via database transfer on the network. Accurate and rapid drilling with improved registration of the multilayered PWB is made possible with the new drill/router.

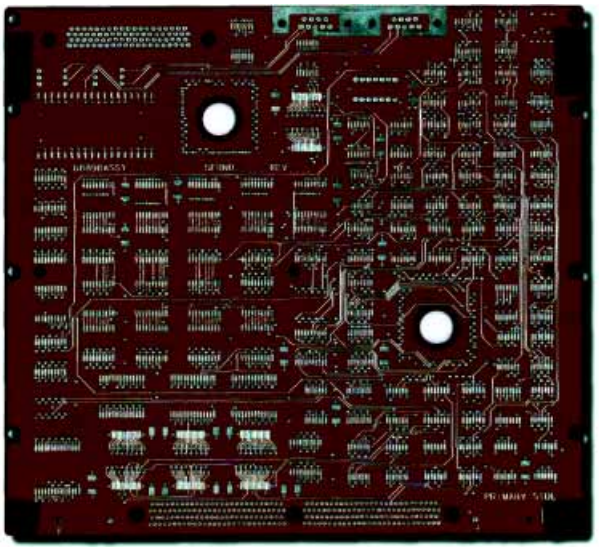
Typical PWB materials are polyimide or FR4, fire-resistive epoxy-glass. Once the lamination, drilling, routing, and plating processes are completed, the PWB is quality tested before the start of the assembly process using an automated continuity probe-checker. This continuity check, performed by tester files that are derived from Mentor Graphics software database capabilities, verifies that the PWB is routed and the registration is consistent with that of the design and its associated schematic. Coupon testing or cross-sectioning is also performed prior to placement and assembly of expensive parts. The bare PWB board, generated from the drawings shown in Figs. 2a and b, is pictured in Fig. 3a. The PWB is a product of the design efforts, internal reviews, and fabrication processes discussed in the previous sections. It represents a reliable, quality product that is ready for assembly.

Assembly

As the last phase of the hardware fabrication effort, the assembly process combines the product design, fabricated parts, and electrical components into a completed subsystem. The actual assembly process flow is established during the IFFRs. Typically, assembly-level products are delivered to the customer for integration into larger systems.

The assembly facility is divided into several parts. All are electrostatic-discharge protected and temperature and humidity controlled. Hardware assembly, which does not require high reliability, is performed in an area that has no controls over airborne particulates beyond what is present in the rest of the building. Typically, this area is clean to about the level of 300,000 particles of 0.5 μm or larger per cubic foot of air, but it is not monitored continuously. The areas where soldering is the prime assembly technology are controlled and monitored to be within the specifications of a 100,000 level clean room. The area where bare integrated circuit chips are attached and the wire bonds are affixed is controlled to the 10,000 level clean room with the additional gowning and material control

(a)



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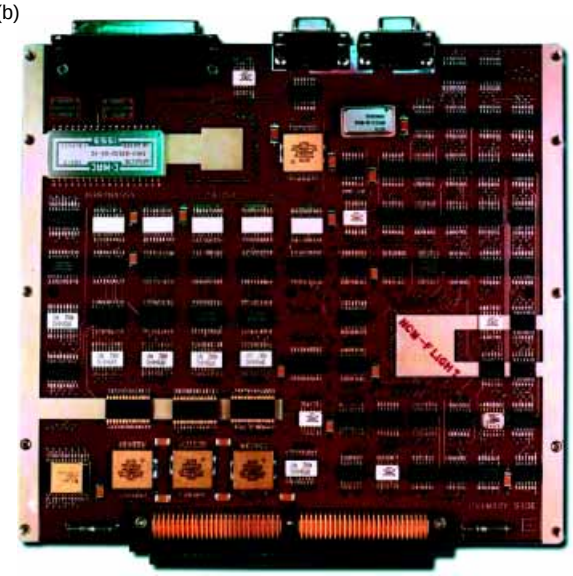

Figure 3. NEAR/RTX printed wiring board: (a) finished product and (b) assembled board.

requirements. In each case, the level of cleanliness is determined by what is considered prudent to maintain high yields.

Peripheral to the assembly facilities are two areas used for preparing the kits of parts that move to the proper assembly area. One preparation area is adjacent to the 10,000 level clean room assembly area and is used for kits that contain bare die, i.e., COBs and MCMs.

The quality and reliability assurance inspection tests as well as electrical testing are conducted at various assembly stages. Prior to the final conformal coating of the board, each subassembly goes through an exhaustive inspection to ensure that workmanship, documentation, and other qualification steps are met.

The NEAR/ RTX PWB, shown earlier in the different stages of design and fabrication, is shown fully assembled and ready for delivery in Fig. 3b. The NEAR IR Spectrograph board uses flex-circuit interconnections (see Fig. 5 in the article by Wagner, this issue). Figure 4 shows an RF power amplifier. RF circuits require special practices and materials throughout the design and fabrication process because of their sensitivity to circuit line lengths and board configuration.

The top assembly is a process that places all the subassemblies together after their respective inspections and electrical tests. Then the unit is ready for system integration, performance, environmental, and qualification testing. At that level, performance testing ensures that the system's functional requirements are met.

FUTURE INITIATIVES

In the future, there will be significant changes to the way electronic systems are designed and packaged. A variety of new options are available in the areas of system architecture, housing material, and component selection. Novel procedures will have to be developed to allow the creative use of these new options. The use of historical industry experience as the dominant guideline for high reliability will have to evolve into a set of internally defined practices based on research, analysis, and testing. To be competitive in the future marketplace, the Laboratory must be a leader in the design and fabrication of advanced electronic systems.

The Integrated Electronics Module and Remote Input/Output Projects

A critical focus for new electronic systems is the need to increase capability while reducing size and weight. Two programs that exemplify this effort are the IEM and Remote Input/Output (RIO) projects. Both of these programs have required the development of new packaging concepts.

The IEM project is developing a set of core spacecraft electronics within a scalable system architecture that will decrease the size and number of electronic packages required in a satellite. However, the functional capabilities of the new system will not decrease, and its hardware can be reused between programs.

The IEM's multicard arrangement on a common backplane, which combines digital, analog, and RF systems, does not fit into the traditional design guidelines. Typically, these systems are isolated from each other to reduce interference. The reduction of a box-level electronic system to a single PC board is accomplished by increasing the capabilities of individual components and fitting more components into a given area.

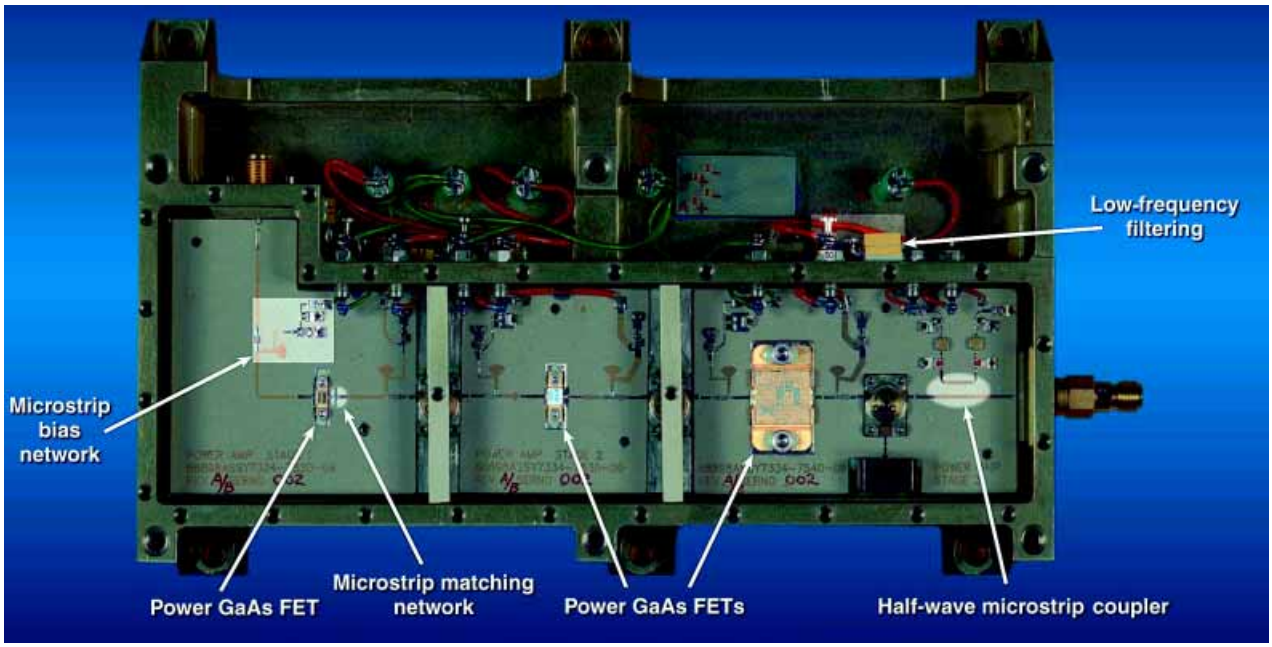

Figure 4. A 5-W X-band power amplifier assembly (length ≈ 18.4 cm; GaAs = gallium arsenide, FET = field effect transistor).

The RIO project is developing a remote interface chip for spacecraft telemetry. Presently, electrical currents, temperature, and voltages must be fed in directly to the telemetry system, resulting in a large and complex spacecraft harness. The RIO chip will read these values locally and send the data to the telemetry system over the spacecraft electrical bus.

These ASIC chips simplify and standardize the input to a spacecraft data handling system. However, the cost of these packages needs to be less than the circuitry they are replacing. The unit consists of a single ASIC chip mounted to a small PC board with a few discrete components and room for the connector attachments. Five to 20 identical versions of these assemblies would be used on a single spacecraft project.

The fabrication of this assembly must be approached as a production issue. Standardizing the packaging technique will reduce the cost per unit and discourage arbitrary changes to the unit. Figure 5 shows the packaging concept for the RIO. Incorporating the practices associated with production-line quantities will support the reuse of hardware among different programs. Reuse and standardization of common functions, while also promoting flexibility and growth in those mission-specific areas, will provide a better overall product at a lower price.

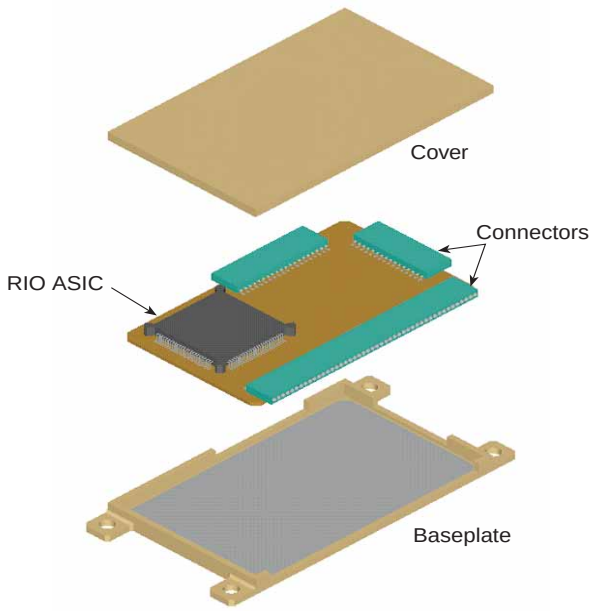

Figure 5. Remote Input/Output application-specific integrated circuit (RIO ASIC) implementation.

New Packaging Considerations and Requirements

The integration of greater functionality into single electronic components introduces new packaging complications. These parts require both heat sinking and a reliable mounting interface. Analytical and test techniques must be developed in parallel with these new technologies to ensure their effectiveness and reliability in unconventional configurations. The composite electronics enclosure developed by the IEM team is shown in Fig. 6.

Traditional practices require stress relief in the leads of all components. Packages with ball-grid array, pin-grid array, or J-lead configurations do not allow stress relief in the leads. Heat sinking a device of this type by bonding it to the PC board ties the electrical and mechanical joints together in a manner that was unthinkable several years ago (see the article by Bevan and Romenesko, this issue). Clearly, we do not have any historical background to use in deciding the reliability of these joints. The proof of these new mounting configurations rests primarily on analysis. However, the numerous variations in soldered joints, bonded joints, coefficient of thermal expansion (CTE) mismatches, and material variations preclude easy solutions. Alternatively, increasing the complexity of the thermal analysis of these parts can help determine the heat loss through the leads, which reduces the need for more heat sinking. Again, the variations in board layout, trace geometry, and board construction do not lend themselves to general guidelines.

Further impediments to the use of high-density circuits are the restrictions placed on the circuit board design by the design and fabrication areas. Design requirements are no longer imposed externally on our programs. Track size and spacing can be reduced past the point where they impact the reliability of the circuit. How much reduction should occur requires a trade-off between the design and fabrication disciplines. Included in this decision has to be ongoing analysis and testing to judge the functionality of the track density on typical circuits. Our production runs are far too small to let us learn by our mistakes.

Commercial Plastic-Packaged Parts

Being a leader in the development of new technology requires the Laboratory to be a master of our existing technologies. One of the areas where we have limited experience is in the use of commercial plastic-packaged parts. Traditional military specifications require the use of high-reliability ceramic electronic components. Existing reliability de-rating decisions assume ceramic parts, where the largest failure mechanism is shortened life caused by high-temperature operation. The use of plastic parts involves considerable uncertainties. For example, the manufacturer-specified limits for plastic parts are smaller than those for high-reliability parts: typically, 0 to 70°C ambient temperature, compared to −55 to 125°C, respectively.

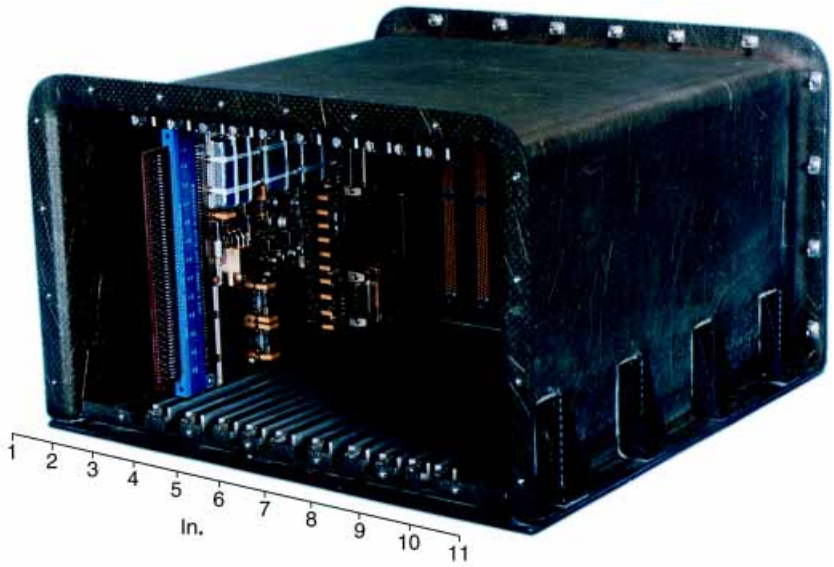

Figure 6. Integrated Electronics Module electronics enclosure.

Failure mechanisms for plastic packages are less understood, so de-rating and design guidelines are difficult to generate.

The incorporation of commercial parts and plastic packages into high-reliability systems raises new design issues. Commercial electrical components are not produced to fixed standards. Limited manufacturer data may be available. No test and certification data like those that come with military-grade parts are available. The die temperature sensitivity is the same for commercial and high-reliability parts, but the different packaging introduces new failure mechanisms. The adhesive system holding the die to the carrier is typically the limiting item on the hot end, while CTE differences between materials can cause wire bond failure on the cold end. Upgrade screening, like that normally done on ceramic parts, could actually use up part of the useful life of a commercial part. Again, reliability decisions on these subjects require a new approach (see Moor et al., this issue).

The importance of commercial parts in high-reliability systems is driven by availability, not cost. Some of the parts necessary in complex military and space electronics are not fabricated in high-reliability packages. The choice is not whether to use these parts, but how best to incorporate them. Traditional temperature requirements for military and space hardware are determined, not by their predicted environment, but by the capability of the parts themselves. In most cases, design temperature limits are chosen to match the component requirements, with margin added for internal temperature drops. Incorporating commercial parts should involve a review of the present design guidelines and how they should be modified to support our new goals.

CONCLUSION

APL is meeting the challenges of its DoD and civilian customers by producing new, highly advanced, and integrated electronic systems. As electronic design requirements increase, the reliance on developments in the supporting analytical, design, and fabrication disciplines will also increase. The development and implementation of new technologies are playing more prominent roles. Miniaturization and integration are creating new opportunities, but also new problems. Coupling the design software and fabrication processes continues to be a crucial step in the overall process. However, a more fundamental change is also under way. Electrical and mechanical disciplines are being tied together as never before. In the future, how we produce hardware will be as important as the hardware itself.

The inclusion of the commercial sector into the aerospace market has increased the emphasis on quality, cost, and schedule. The days of the highly reliable yet highly expensive product are waning rapidly. The Laboratory must continue to produce innovative solutions to evolving problems, and new design and production processes are needed to implement these solutions.

Electronic design and fabrication are critical areas in the development of APL's new electronic systems. The importance of our ability to design, fabricate, and assemble these systems in a reliable and reproducible manner is increasing. TSD is pivotal in producing the Laboratory's traditional high-quality electronic and mechanical systems. As new technology developments require more emphasis on the production process, TSD will play an important role in the choice and implementation of these technologies.

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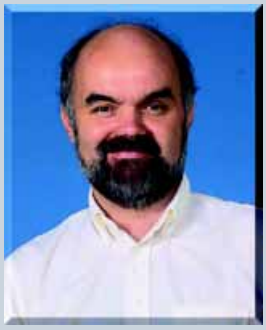

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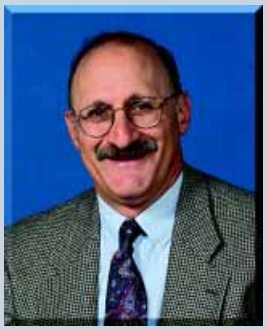

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