Multichip Module Substrates

Norman A. Blum, Harry K. Charles, Jr., and A. Shaun Francomacaro

The three major technologies used to fabricate substrates for multichip modules (MCMs) are described. These are MCM-L, composed of metal traces on stacked organic laminate sheets; MCM-C, metal patterned and interconnected on co-fired ceramic layers; and MCM-D, vapor-deposited, patterned metal layers alternating sequentially with spun-on or vapor-deposited dielectric thin films. Examples of circuits fabricated at APL using each of these MCM technologies are presented.
(Keywords: Electronic packaging, Multichip modules, Substrates, Thin films.)

OVERVIEW

Multichip packaging of bare electronic integrated circuits (ICs)[1] represents a rapidly growing technology that is revolutionizing the electronics industry. This technology eliminates the discrete packaging of individual IC elements, and replaces the interconnection of packages that are much larger than the chips they enclose with monolithic structures that interconnect two or more bare (unpackaged) chips. At the heart of this packaging revolution is the replacement of the multilayer printed wiring board (PWB) that connects individually packaged components by a substrate having sufficiently small features as well as the high wiring density needed to interconnect the bare chips. Elimination of a separate enclosure for each chip results in a smaller, lighter package that often may exhibit enhanced performance when compared with a conventionally assembled circuit; significant cost savings may also be realized in high-volume production.[2]

This article describes and compares the three principal technologies used at APL for fabricating multichip module (MCM) substrates: MCM-L, MCM-C, and MCM-D (Fig. 1). In their respective construction, they use organic laminates (similar to conventional PWBs), ceramic structures and dielectrics (similar to thick film circuits), and vapor-deposited metal and spun-on or vapor-deposited dielectric layers (similar to ICs). Other organizations have developed variations of these technologies and use alternative substrate materials that are beyond the scope of this review.[3]

Recent advances in technology have enabled the IC's interconnection density and the speed at which it functions to outstrip the capacity of conventional PWBs. Although PWBs have adapted well over the years by adding layers to provide increased wiring complexity, modifying dielectric characteristics to accommodate higher speed circuits, and reducing feature size to allow for improved packing density, the new requirements far exceed the capabilities of today's standard PWB technology.

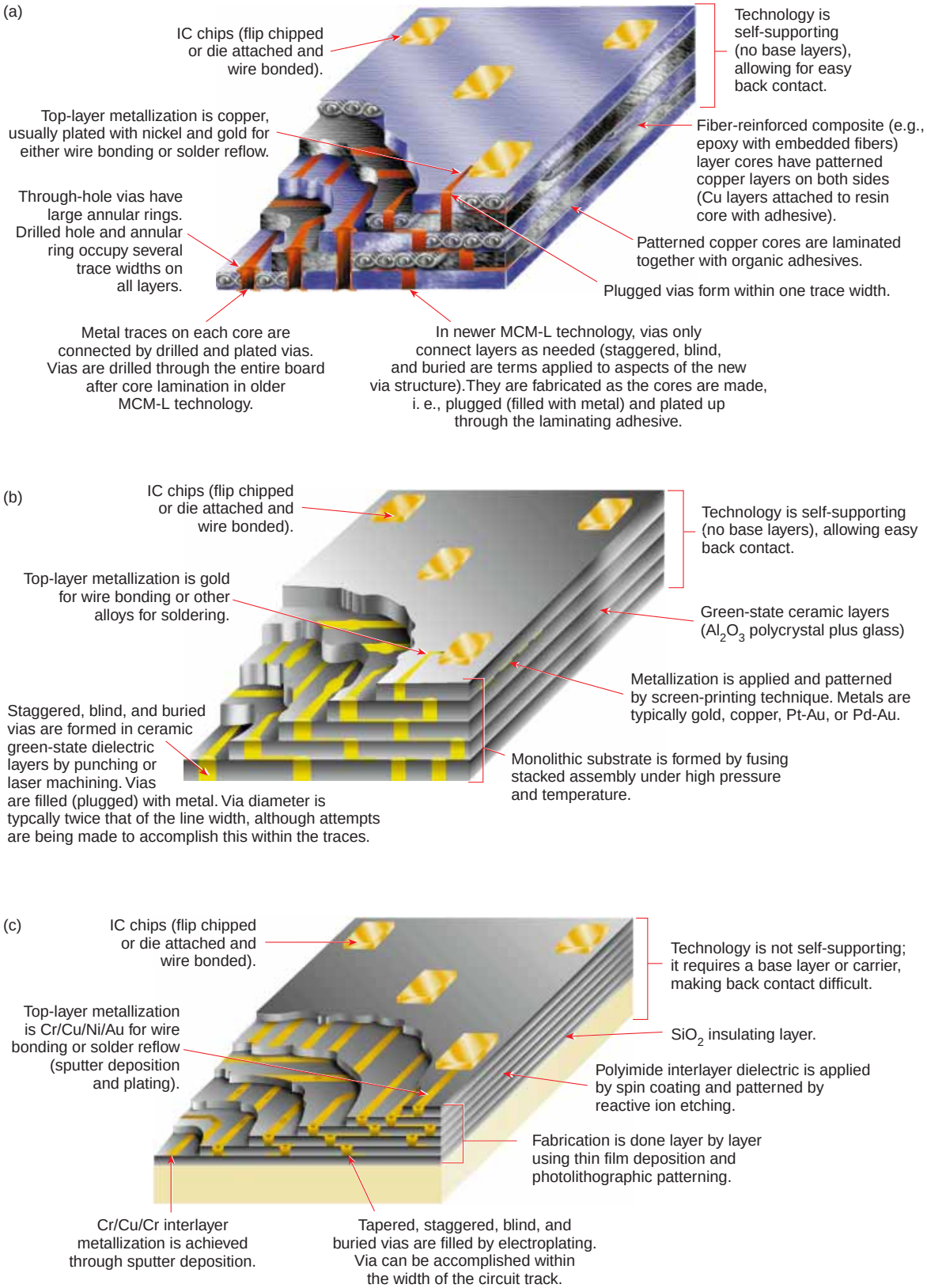


Figure 1. Substrate technologies (vertical dimensions not to scale for clarity): (a) MCM-L, (b) MCM-C, and (c) MCM-D.

MCMs were invented to replace the standard organic PWBs in circuits that require interconnecting many high-density ICs along with other components. In addition, since those circuits had to be compact, lightweight, and operable at sufficiently high speed, MCMs were developed to reduce concerns about delay times on the board and crosstalk between components and signal traces. As an approximate rule of thumb, an electronic circuit is considered to be an MCM if more than half of its area is covered with active devices, although some circuits adapt more readily to this definition than others.[4]

Each type of MCM has its place in the technological hierarchy. MCM-L is derived from conventional PWB technology and makes use of enhanced materials and processes, high-definition photolithographic techniques, and strict quality control to provide smaller features and more accurate placement than are customary with standard PWBs. MCM-L component assembly procedures differ dramatically from PWB assembly practices, most notably in replacing standard package soldering processes associated with PWB manufacture with wire bonding or flip-chip[5] processes. In this respect, MCM-L is similar to what once was called "hybrid electronic circuits," with two notable exceptions: (1) MCM-Ls typically contain no packaged parts, and (2) the module package need not be hermetically sealed. MCM-L provides the lowest density of the three MCM technologies and is usually the least expensive to implement. MCM-L, also known as chip-on-board (some authors make a technical distinction between the two), is discussed in greater detail by Le et al. elsewhere in this issue.

MCM-C is similar to the older ceramic, thick film hybrid circuit,[6] with some notable improvements. In conventional ceramic hybrids, the multilayer circuitry is screen-printed onto a rigid ceramic substrate (usually alumina). Printed layers alternate between metal traces and dielectric, with metal-filled "vias" to connect one layer to the next. The ceramic layers usually have a dielectric constant greater than 5. A true MCM has only bare ICs, although occasionally packaged parts may be incorporated into the circuit. The packaging density is proportional to the fraction of the substrate surface area occupied by components of the circuit, but is limited by via size and alignment difficulties when screening several layers, which become less planar as the number of layers increases.

A particularly interesting MCM-C substrate approach is that offered by low-temperature co-fired ceramic (LTCC). This fused ceramic technology can be processed at conventional thick film temperatures (800–1000°C) rather than the normal co-fired temperatures of up to 1400°C.[7] To fire at the low temperatures, glass is incorporated with the ceramic. This not only reduces the fusing point but also lowers the relative dielectric constant, thereby improving circuit performance at high frequencies.

In the LTCC process, each layer is screen-printed on a flexible, unfired ceramic tape.[7] Layers have laser-drilled via holes that are filled with an appropriate conductor by a screen printing or analogous stencil masking process. The layers are subsequently aligned and subjected to high-pressure consolidation before being fired together once. The small laser-drilled vias and the planarity of each screened layer serve to increase the wiring density over the conventional "print, dry, fire" multilayer thick film process.

The LTCC process adapts well to the incorporation of blind vias (those that do not extend completely through the substrate) and also permits the fabrication of precisely dimensioned cavities that have found applications in microwave circuitry. Additional recent modifications in this technology will allow somewhat higher packaging density to be achieved through the use of photosensitive materials that are lithographically defined (rather than printed). Further details and examples of circuits using the LTCC process will be described later.

The various MCM-D processes yield the highest-density circuitry while being the most labor-intensive and expensive of the three MCM technologies.[2] Here, both the metal and dielectric layers are sequentially deposited in the form of thin films and patterned by photolithographic transfer processes. The substrate can be any very flat, smooth surface. Metal plates, ceramic, glass, and other materials have been used. At APL, we have mostly used silicon wafers as base substrates because they are readily available, very smooth, and flat; most importantly, they match the coefficient of thermal expansion of the low-stress polyimide layers and, of course, the silicon die. In today's MCM-Ds, the silicon base is merely a platform for the circuit constructed upon it; the semiconducting properties of silicon play no role (as they do in ICs). In the future, active circuits may be integrated into this base or support layer.[8] Features (width of conducting traces, spaces, and vias) can be smaller than 25 μm. A detailed description of a typical MCM-D process and some examples of completed circuits will be given. A brief comparison of various features of the three types of MCM circuits as developed at APL is presented in Table 1.

MCM-L

This technology is derived from organic PWB fabrication and uses copper metal traces etched onto reinforced organic laminates, with plated through-holes or vias interconnecting the layers. Compared with conventional PWBs, advanced processing techniques result in smaller features and allow incorporation of

Table 1. Comparison of MCM features.

Design parameters	MCM-L	MCM-C (LTCC)	MCM-D
Feature size (line/space) (mm)	125/125	100/125	20/20[a]
Via size (μm)	250	200	20
Critical dimension uniformity +/− (μm)	12	25[b]	5
Number of levels	10	20+	5+
Dielectric constant	3.5 to 4.5	5.2 to 7.8	2.9
Dielectric thickness (μm)	112	100	1 to 10
Cutouts/cavities	Yes	Yes	No
Integrated resistors/capacitors	No[c]	Yes	Yes

[a]Smaller lines and gaps can be defined, subject to circuit impedance and delay requirements.

[b]Even though line widths are smaller for MCM-C (LTCC) than MCM-L, critical dimension uniformity is greater because of firing shrinkage.

[c]Integrated capacitors and resistors are being developed in several laboratories.

vias that extend only part way through the board (blind vias) as well as those that connect between layers entirely within the board (buried vias). These blind and buried vias greatly increase the wiring density of components that can be connected on the board.

MCM-L refers specifically to the technology used to manufacture the wiring platform. The platform may be used to interconnect a few ICs in a pure, standalone MCM or to build up a complex circuit board that contains many components and incorporates various schemes to protect the bonding wires and components (e.g., "glob top" or hermetic encapsulation).[9] These complex boards may even have other MCMs attached to them and are typically called chip-on-board circuitry.

MCM-C

The middle rung on the three-step MCM classification ladder uses ceramic-based substrates. These MCM-C substrates have evolved from traditional thick film fabrication techniques[6] in response to the need for increased packaging density and enhanced performance. Density was increased by shrinking the size of features such as the vias used for interconnecting substrate layers, the conductor traces used for signal routing, and the gaps between different traces or vias. In the traditional thick film process, these features are created by screen printing, in which the screen mesh geometry limits the achievable line widths and spaces. Several parameters determine the resolution of printed elements in addition to the screen itself: the viscosity of the thick film paste, the ability of the emulsion to form a good gasket with the substrate, and the squeegee speed and pressure. Combining and optimizing all of these elements results in a process that can produce 200-μm vias and 125-μm lines or spaces. This significant reduction in feature size was made possible about 10 years ago by DuPont's LTCC thick film process and by the use of thick film materials produced by other vendors.

The main difference between conventional thick film and LTCC processes is the nature of the dielectric. In the thick film process, the dielectric layers are screen-printed, as are the conductor layers, by screening the appropriate paste onto the ceramic carrier substrate (usually with the via holes delineated and aligned with the metal pattern), and then fired. Subsequent layers are built on top of the previous layers like a stack of bricks set on a foundation.

With the LTCC process, the dielectric layers are sheets of unfired ceramic. Each sheet is separately patterned with its metal conductor traces, and then collated and stacked together like pages in a book. The sheets also have vias filled with conducting metal that interconnect the different patterned layers. The LTCC process can produce 200-μm or smaller vias because they are either mechanically punched or lased into each individual unfired ceramic layer instead of being screen printed. The vias are filled by extruding the conducting paste into the via holes through a stencil made from either thin brass or a polyimide sheet. The reduction in line and space sizes with LTCC results chiefly from being able to print each conductor layer on its own slice of unfired ceramic. The surface is significantly smoother than thick film ceramic and essentially flat, which allows the screen emulsion to seal against the surface during the printing process, thus ensuring high pattern integrity. Finally, since all of the circuit features during LTCC production are created on unfired ceramic, they undergo identical shrinkage of about 20% when fired (i.e., all the layers are fired at once, hence the use of the word "co-fired" in describing this technology). The firing process takes place at about 900°C. Cross-sectional diagrams of the various process stages are shown in Fig. 2.

Computer-aided design tools can be used to create an LTCC substrate layout from a circuit schematic. In addition to a set of design rules (feature sizes, etc.) customized for each process, one must consider certain issues that could affect manufacturability such as via and cutout size and location, and metal balance. The

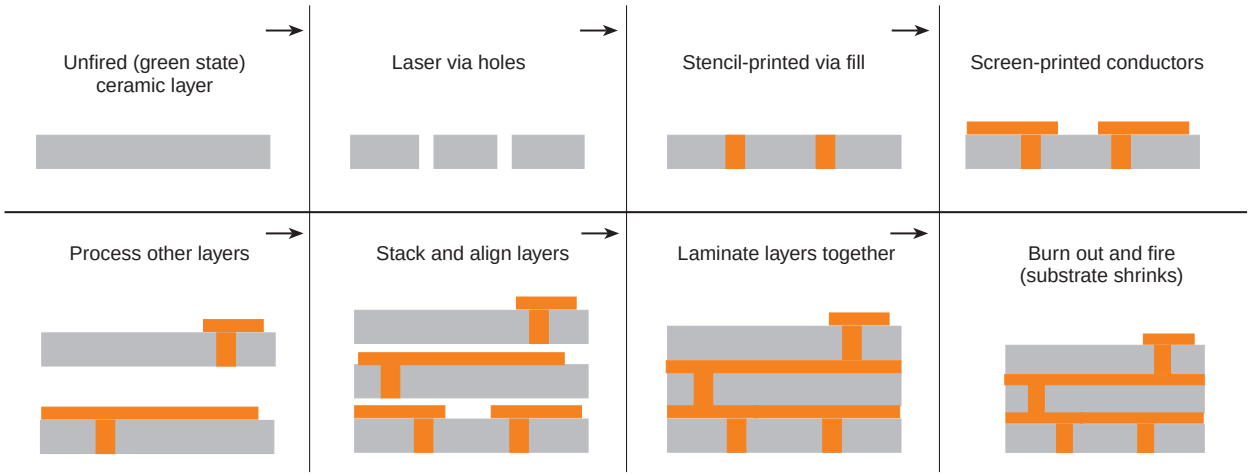


Figure 2. Schematic representation of low-temperature co-fired ceramic (LTCC) substrate fabrication sequence.

individual unfired ceramic layers are analogous to pieces of paper: they are flexible and can be cut or torn, but unlike paper, they are somewhat brittle in that they can fracture if the stresses are too great. A well-designed layout places vertically adjacent vias in a staggered pattern rather than in a straight line, and the design should avoid the formation of "ceramic islands," i.e., areas separated from the remainder of the substrate by a perforation of vias. During the processes of via filling and conductor printing, the pieces of ceramic are held in position by a vacuum that passes through a porous stone fixture to the back side of the single-layer substrate. Large-area cutouts and a large number of vias reduce the amount of surface area in contact with the vacuum fixture, making it difficult to hold the layer securely during printing. Care must be taken to limit the openings in each ceramic layer to no more than 40% of the total surface area.

The other issue, metal balance, is important for two reasons. First, the metal shrinks at a slightly different rate than the ceramic during firing; and second, the mechanical strength of the fired metal is lower than that of the fired ceramic. To ensure uniform shrinkage and mechanical integrity, the design should strive to maintain the same cross-sectional metal content across the substrate. Individual layers can be "unbalanced" as long as the sum of all the layers provides a reasonably overall even distribution of metal. Sound designs lead to robust LTCC substrates capable of yielding high-performance MCM packages, as exemplified at APL in the fabrication of a direct digital synthesizer circuit (see Fig. 19 in the article by Wagner, this issue) and a 14-GHz transmit/receive circuit (Fig. 3).

The direct digital synthesizer is a programmable RF generator, with a 600-MHz clock, that digitally synthesizes sine-wave signals in the 100- to 175-MHz range in approximately 35-Hz steps.[10] Silicon and gallium arsenide ICs that dissipate a total of over 10 W are assembled in the module. The substrate consists of 10 conductor layers constructed on 10 low-dielectric-constant (K = 4.5) ceramic layers and contains a cutout that enables the digital-to-analog converter die to be mounted directly to the package bottom for maximum heat removal.

The 14-GHz transmit/receive module contains five gallium arsenide microwave ICs fabricated by a foundry using the MESFET (metal-semiconductor field-effect transistor) process.[11] These dies (along with passive components) and thin film 50-Ω transmission lines must be packaged within a waveguide structure designed to be beyond its cutoff frequency at 14 GHz. The LTCC process, with its unique ability to include complex cavity structures having accurate dimensions, lends itself perfectly to this application. The substrate contains 23 dielectric layers, with the microwave cavity formed by the top 14 layers. The components are mounted on the cavity floor (layer 9), and all of the

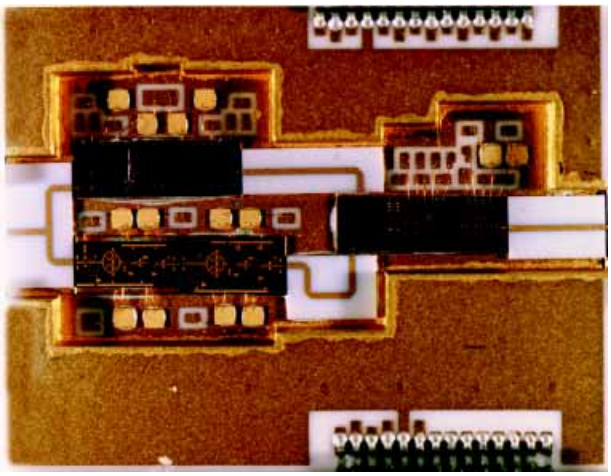


Figure 3. Transmit/receive module using LTCC MCM-C substrate technology.

layers below contain thermal vias to facilitate heat transfer from the back of the die. Signal routing occurs on all 23 layers; the package input/output is brought to the top layer. In this configuration, the transmit/receive function is achievable with only a 0.25-dB reduction in the gain of the low noise and power amplifiers.

The thick film industry's introduction of photoprintable thick film pastes promises to further reduce feature size in MCM-C substrates by eliminating screen patterning altogether. This technology has been shown to yield a process capable of producing vias, lines, and spaces down to 75 μm. In this process, the conductor and dielectric pastes are photosensitive. They are applied to the entire substrate by printing with a blank screen (a screen with all of the emulsion removed). Then, after drying the layer, it is exposed through a photomask to ultraviolet light. The unexposed regions are subsequently removed in development, leaving behind the desired circuit pattern, which is then fired using a standard thick film furnace profile. Since this system optically delineates substrate features, it has significantly greater resolution than screen printing. Additionally, blind and buried vias are easily fabricated; no critical processing is required, as is the case in MCM-L circuits. Other vendors are introducing etchable thick films that hold similar potential, especially for high-frequency circuitry.

MCM-D

The combination of superior materials and the dimensional resolving power of thin film technology enables MCM-D to dominate the MCM arena as the clear leader in packaging density and circuit speed. Feature sizes can be smaller than 10 μm, which is an order of magnitude more than possible with either MCM-L or nonphotodelineated MCM-C. The fabrication processes are similar to those used in the manufacture of ICs in that all of the features are photolithographically defined.

The classification MCM-D applies to several different dielectric/metallization technologies that share a common technological philosophy of photolithographically patterning sequential thin film layers. Spin-deposited polymers such as polyimide and benzocyclobutene are the mainstay dielectrics; chemical-vapor–deposited silicon oxides, nitrides, and oxynitrides are sometimes used as well. The conductors are usually sputter-deposited copper, aluminum, or gold.

The MCM-Ds built at APL use a single-crystal silicon wafer base with spun-on polyimide dielectrics containing buried copper conductors and gold as the top-level metallization. The first layer deposited on the silicon carrier can be either a conductor or a dielectric, depending on the circuit design.

When forming a dielectric layer, spin coating of the polyimide is done in several steps. Initially, an aminosilane solution is spun onto the surface and baked to provide a monolayer that increases the adhesion of the polyamic acid precursor. Then, to ensure a defect-free dielectric layer and to increase the degree of planarization, a second coat of the polyamic acid precursor is applied and soft-baked. The complete curing process entails further heating up to a peak temperature of 350 to 400°C, which provides enough thermal energy to crosslink the polymer and form a true polyimide.[12] The vias are formed in the polyimide by reactive-ion etching in an oxygen plasma using a photopatterned metal mask.

The next step is to remove the metal mask and lightly plasma-etch the top surface of the polyimide to increase bonding sites for the subsequent metal deposition. The metal layer is actually a tri-layer of two metals, with a thin adhesion metal underneath and on top of a thicker high-conductivity metal. After photopatterning, the metal stack is etched in various acid solutions, the photoresist is removed, and the process is repeated with the next dielectric layer. The cross-sectional drawings in Fig. 4 depict the process steps.

As with other MCM technologies, computer-aided design tools are valuable for laying out MCM-D substrates, and some processing knowledge (beyond design guidelines) can facilitate building a circuit design that enhances yield and function. The weakest link in the MCM-D substrate fabrication process is forming the dielectric. It is difficult to create large planes of defect-free polymer films, and thus a major concern when generating a substrate design is the amount of "crossover area." This area is created whenever the metal that sits on top of a given dielectric layer crosses over any metal on top of the layer immediately below.

Any open defect in the dielectric layer in the crossover area will cause a short between the two metal layers, effectively compromising the substrate. A design that minimizes the crossover area is therefore desirable to maximize yield. Most importantly, full area ground and/or power planes must be avoided, since adjacent layer ground and power planes will almost certainly assure failure. Whenever possible, distributed power and ground lines should be used, and if full planes are required, they must not be next to each other in the layer stack. Also, when routing signal traces on more than one layer, it is important to keep most of the traces within each layer running parallel to each other and to alternate the direction of adjacent signal layers so that the traces on those layers are orthogonal to each other.

These design techniques have been applied with great success to APL's MCM-D process, which has been used to fabricate a variety of circuits including an advanced communications module (see Fig. 20 in the

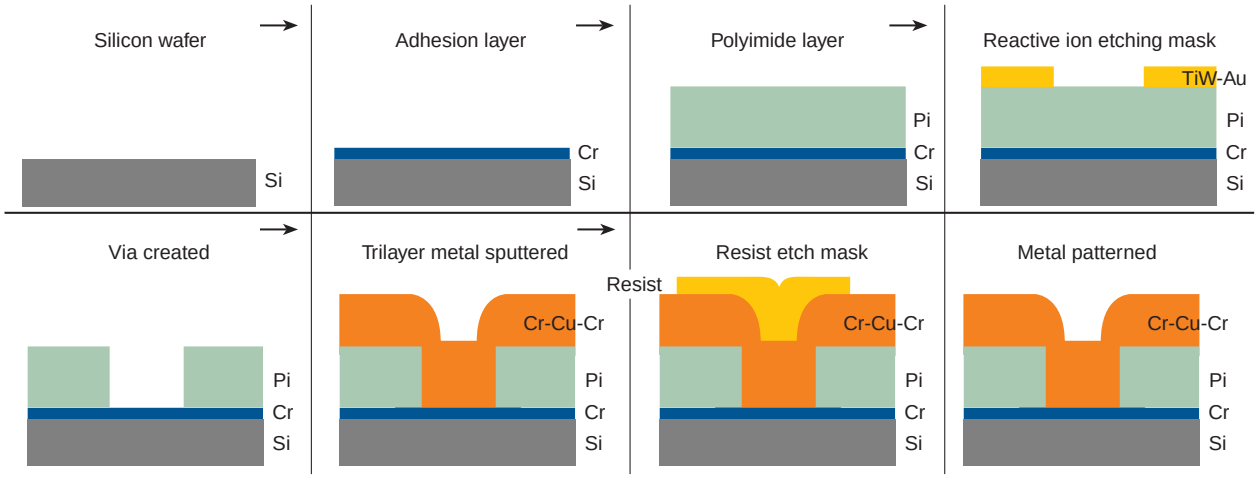


Figure 4. Schematic representation of multilayer thin film polyimide substrate fabrication sequence.

article by Wagner, this issue) and a static random-access memory (SRAM) module. The as-fabricated substrate for the SRAM module is shown prior to dicing in Fig. 5. The assembled and packaged eight-chip module with decoupling capacitors is depicted in Fig. 7 in the article by Bevan and Romenesko, this issue. The eight SRAM chips are interconnected by a seven-layer substrate into a 32K by 8-bit memory organization. Multiple SRAM modules are then integrated onto a simple PWB to form larger memory configurations. Up to 2-MB have been demonstrated to date.

Progress in MCM-D technology likely will not focus on further shrinking of feature sizes to increase packaging density, since the module surface, in some cases, may already be nearly completely covered with devices. The relatively high cost of MCM-Ds is still an important consideration. However, increasing substrate yield can reduce costs. This can be accomplished by developing more efficient processing equipment (e.g., polymer precursor dispensing systems) and by reducing the process cycle time through the use of photosensitive polymer dielectric,[11] which simplifies the process while enhancing via reliability.

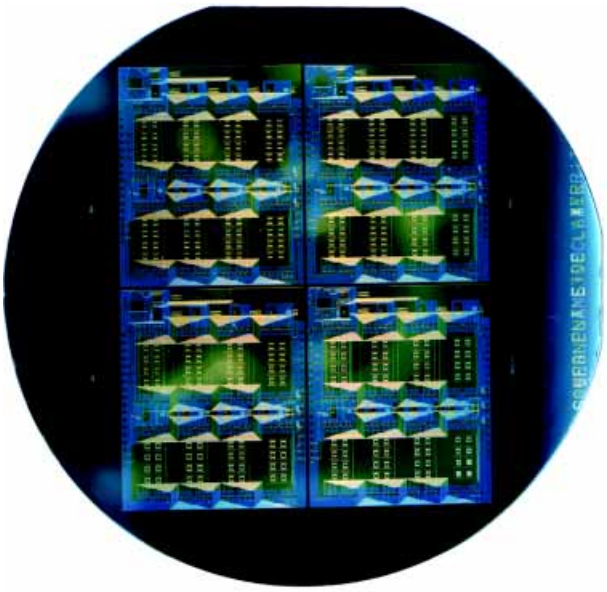


Figure 5. MCM-D substrate for the SRAM module. This silicon wafer (10-cm dia.) contains four SRAM substrate patterns.

CONCLUSION

MCMs are a mainstay of modern, high-performance packaging. Different substrate structures (MCM-Ls, -Cs, and -Ds) are required to address the diverse application areas of today's (and tomorrow's) electronic devices. APL has standard, in-place processes for all the relevant MCM substrate areas and has used these technologies to deliver high-quality, reliable products to our in-house and external customers. Higher performance needs in the future will force the reduction in line widths, layer thickness, and via size even more. New materials (e.g., diamond) and processes (e.g., laser-cut vias in PWBs) will be introduced to our substrate fabrication activities to keep pace with the changing demands of electronic technology.

REFERENCES

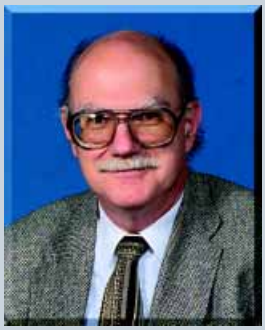
[1] Messner, G., "Price/Density Trade-offs of Multi-Chip Modules," in *Proc. 1988 Int. Microelectronics Symp.*, Seattle, WA, pp. 28–36 (1988).
[2] Charles, Jr., H. K., "Cost Versus Technology Trade-Offs for Multichip Modules," in *Proc. 1995 Int. Microelectronics Symp.*, Los Angeles, CA, pp. 553–558 (1995).
[3] Takahashi, T., Rutter, Jr., E. W., Moyer, E. S., Harris, R. F., Frye, D. C., et al., "A Photo-Definable Benzocyclobutene Resin for Thin Film Microelectronic Applications," in *Proc. Int. Microelectronics Symp.*, Yokohama, Japan, pp. 64–70 (1992).

[4] Charles, Jr., H. K., "Design Rules for Advanced Packaging," in *Proc. 1993 Int. Microelectronics Symp.*, Dallas, TX, pp. 301–306 (1993).
[5] Miller, L. F., "Controlled Collapse Reflow Chip Joining," *IBM J. Res. Dev.* 13, 239–250 (1969).
[6] Romenesko, B. M., Falk, P. R., and Hoggarth, K. G., "Microelectronic Thick Film Technology and Applications," *Johns Hopkins APL Tech. Dig.* 7(3), 284–289 (1986).
[7] Charles, Jr., H. K., "Materials/Design Considerations for MCMs," in *MCM-C/Mixed Technologies and Thick Film Sensors*, W. K. Jones, K. Kurzweil, G. Harsanyi, S. Mergui, et al. (eds.), Kluwer Academic Publishers, Dordrecht, The Netherlands, pp. 177–193 (1995).
[8] Bodendorf, O. J., Olsen, K. T., Trinko, J. F., and Winnad, J. R., "Active Silicon Chip Carrier," *IBM Tech. Disclosure Bull.* 15(2), 256 (1972).
[9] Uy, O. M., and Benson, R. C., "Package Sealing and Passivation Coatings," in *Packaging, Vol. 1, Electronic Materials Handbook*, M. L. Minges (ed.), ASM International, pp. 237–248 (1989).
[10] Lehtonen, S. J., Moore, C. R., Francomacaro, A. S., Edwards, R. L., and Clatterbaugh, G. V., "Microwave Multichip Modules," *Johns Hopkins APL Tech. Dig.* 15(1), 48–56 (1994).
[11] Francomacaro, A. S., Clatterbaugh, G. V., and Blum, N. A., "High Speed Digital Circuits on Low Stress, Thin Film, Polyimide Multichip Modules," in *Proc. 6th Int. SAMPE Electronics Conf.* pp. 358–370 (1992).
[12] Clatterbaugh, G. V., and Charles, Jr., H. K., "The Application of Photosensitive Polyimide Dielectrics in Thin Film Multilayer Hybrid Circuit Structures," in *Proc. 1988 Int. Microelectronics Symp.*, Seattle, WA, pp. 320–334 (1988).

ACKNOWLEDGMENTS: The authors gratefully acknowledge the personnel of APL's Electronic Services Group, without whose help and support the techniques and products described in this article would not be possible. A special thanks is given to S. Lynn Hoff for assistance with manuscript preparation and to Michael S. Mandella for help with the photographs.

THE AUTHORS

NORMAN A BLUM received an A.B. in 1954 from Harvard College, an M.S. in 1959, and a Ph.D. in 1964 from Brandeis University, all in the field of physics. He was a supervisor of the Resonance Physics Section at NASA's Electronics Research Center in Cambridge, MA, before joining APL in 1970 as a senior physicist in the Research Center. He was Technology Manager in the Electronic Services Group of the Technical Services Department and a member of the Principal Professional Staff before his recent retirement. Dr. Blum has an extensive background in experimental condensed matter physics, including Mössbauer and optical spectroscopies, thin films, cryophysics, photovoltaics, magnetic phenomena, laser physics, and semiconductor radiation detectors. His latest interests include the packaging of miniaturized electronics and the photolithographic patterning of complex substrate structures.



HARRY K. CHARLES, JR., received his B.S. in 1967 from Drexel University and his Ph.D. in 1972 from The Johns Hopkins University, both in electrical engineering. He joined APL in 1972 as a Postdoctoral Research Associate. He is currently Assistant Department Head for Engineering in the Technical Services Department and a member of the Principal Professional Staff. Dr. Charles has worked for 25 years in the microelectronics arena, authored over 150 articles, and is an internationally recognized specialist in electronic devices, systems, packaging, and reliability. His latest interests include multichip module design, fabrication, and testing; advanced interconnect; biomedical instrumentation; and novel sensors based on MEMS technology. He is a Fellow and former President of IMAPS (The International Microelectronics and Packaging Society), a Fellow of the IEEE, and a member of the Board of Governors of the IEEE's Components Packaging and Manufacturing Technology (CPMT) Society. His e-mail address is harry.charles@jhuapl.edu.

A. SHAUN FRANCOMACARO received a B.S. degree in microelectronic engineering from the Rochester Institute of Technology in 1988 and an M.S.E.E. degree from The Johns Hopkins University in 1992. Before joining APL in 1989, he performed research on thin film deposition and photolithography at Lockheed Electronics in New Jersey, and served as a process engineer with VLSI Technology in California. He expects to complete the requirements for an M.S. degree in technical management from JHU in 1999. Mr. Francomacaro is a senior staff engineer in the Electronic Services Group at APL, where he works on all facets of thin and thick film process development. He has worked for more than 10 years in the field of microelectronics, authored over a dozen articles, and shares several invention disclosures. His current interests include advanced multichip modules, microwave circuits, and biosensors. Mr. Francomacaro's e-mail address is shaun.francomacaro@jhuapl.edu.