Modern Electronic Packaging Technology

Matthew G. Bevan and Bruce M. Romenesko

A view of modern electronic packaging technology is presented along with its applications at APL. Although not always distinct, electronic packaging may be separated into three levels: component, board, and system. The manufacturing technologies and designs may vary at each level, but they all must provide electrical interconnection, thermal management, and mechanical and environmental protection. Each packaging level reflects a trade-off among many interrelated factors including design requirements, economics, and manufacturing infrastructure.
(Keywords: Electronic components, Electronic packaging, Packaging design, Packaging levels.)

INTRODUCTION

Electronic packaging serves a fourfold function for the electronic circuit by providing it with power and signal interconnection, a path to dissipate heat, mechanical support, and a protected environment that prevents contamination, mechanical damage, and electromagnetic interference. In some applications (e.g., biomedical), the packaging also protects the environment from contamination by the electronics.

Proper packaging design requires identification of the critical issues involved such as performance needs, the application environment, manufacturing capabilities, system heritage, testing, reliability, cost, and schedule. Electronic packaging technology uses a variety of fabrication techniques such as welding, electroplating, and injection molding to accomplish its purposes.

Published information about electronic packaging technology is in abundance today. This article will touch on the critical aspects of packaging technology and how they are applied at APL. For additional information, the reader may consult the selected bibliography at the end of this article, which lists several refereed journals, conference proceedings, and books that track progress in the packaging field.

PACKAGING DESIGN

Over time, the trade-off in requirements has divided electronic packaging into three levels (Fig. 1): device packaging, board packaging, and system packaging. Although separation into these levels is not absolute, they reflect a common method used to organize the

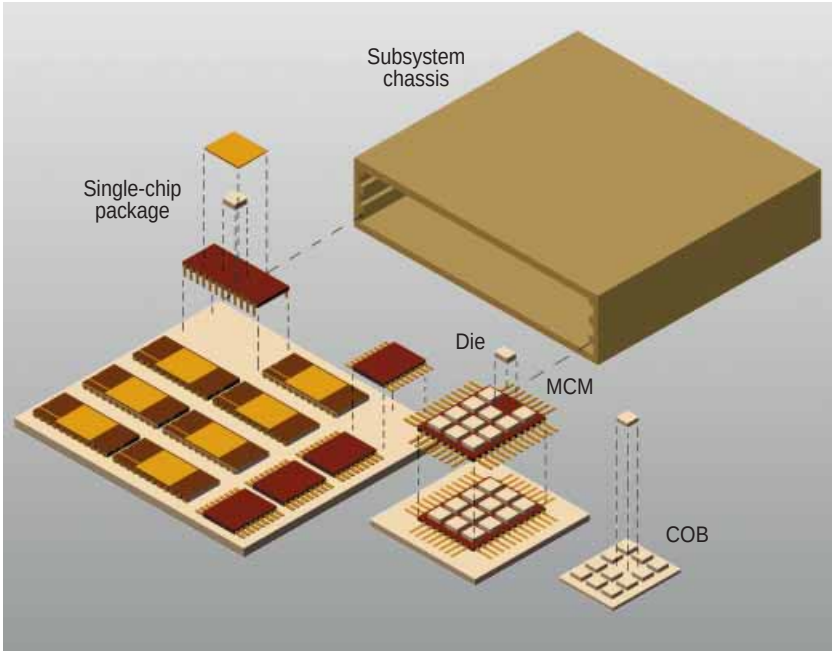

Figure 1. Three levels of packaging: the device is packaged into a component, the component is mounted on the board, and the board is installed into the subsystem chassis (MCM = multichip module, COB = chip-on-board).

electronic circuitry and categorize electronic packaging requirements. Each level of packaging provides similar functions but has a distinct purpose and design.

Device packaging protects the integrated circuit from corrosion and dissipates heat, creating a component with an electrical interface and mechanical support for installation and testing. The printed wiring board or substrate provides support and interconnection of the device packages to create electronic subfunctions suitable for higher-level testing. Box-level packaging allows for electronic interconnection between the circuit substrates, and performs housing and interfacing (such as connectors or keyboards) to the outside world. Partitioning of the electronic system is a process that breaks down the complete electronic circuit into these different levels. The breakdown considers many factors. This process requires an understanding of the circuit and its subfunctions, component and assembly availability, application requirements, as well as development and testing needs.

Meeting performance requirements is foremost in electronic packaging. Factors such as signal speed, noise sensitivity, and electromagnetic interference often dictate the approach to packaging. Signal speed may require substrates with a low dielectric constant or impedance matching. Noisy circuits and circuits that generate electromagnetic interference may hamper the proper functioning of adjacent circuits and may need to be separated from other sensitive circuits by shielding the device or filtering the power and signal lines.[1] These design considerations often dictate component placement, material choices, and space allocation.

Incorporation of off-the-shelf assemblies into the product drives many packaging decisions. Such assemblies perform crucial functions and have their own electrical and mechanical interfaces. There may be many electronic, optical, and mechanical subassemblies to be incorporated into an assembly, for example, power supplies, charge-coupled device cameras, disk drives, card guides, card cages, and connectors. For optimum performance, these subassemblies usually require exacting design considerations such as special mounting brackets and connectors, heat sinking, and environmental protection.

Although these design factors are critical in the prototype and one-of-a-kind hardware that APL designs and builds, commercial and military electronics may have additional life cycle and consumer appeal issues. Life cycle issues such as maintainability and testability must be accommodated. Ergonomics and visual appeal are high priorities in many consumer electronic products. Finally, and usually most importantly, the packaging design must fall within the cost and schedule constraints of the product.

Packaging Reliability

Reliable packaging begins in the design stage. At this point, the packaging engineer must consider the potential for thermal, mechanical, and corrosion problems and determine the best method to minimize their effects.

Heat is a by-product of the circuit's function that raises component temperature and can reduce its reliability. This temperature increase is an internally generated stress that must be accounted for in the package design. Below some threshold, elevated junction temperature has little effect on the life of a part, but above that threshold, component life shortens exponentially with increasing temperature. Thresholds range from 100 to 150°C,[2] depending on the expected product lifetime, circuit design, and materials. Hence, the package's ability to dissipate the device's heat closely correlates to its reliability. Proper thermal package design ensures that the heat dissipation path maintains the junction temperature below the threshold value. High-power devices may require special packaging design and materials to minimize the junction temperature.

Although most circuit boards have sufficient free air convection to safely dissipate heat from the device package, some do not because of high component densities or high heat generation from power transistors, or because they operate in the vacuum of space. In these situations, special features must be incorporated to increase heat removal from the component.[3] As with personal computers, fans work well in many terrestrial environments, increasing heat transfer approximately an order of magnitude over free convection.[4] In a vacuum, however, it may be necessary to improve the thermal path between the device package and substrate. This may be accomplished by filling the gaps between them with a thermally conductive material. Thermal resistance may be lowered across the substrate by bonding a metal heat spreader to it to improve heat flow to the surrounding box.

In addition to component temperature, the mechanical environment may reduce the reliability of the electronic circuit. Specifically, factors such as vibration and shock, along with temperature changes of the system, induce forces that can break components and cause fatigue failure of leads or solder joints. By modeling, the packaging engineer can identify these potential problems early in the design stage and implement design modifications to mitigate these forces.

Over the circuit's lifetime, the thermal stresses on the assembly are frequently more destructive than those created by shock and vibration. In the assembly of electronic packages and circuit substrates, a variety of materials are bonded together with adhesives or solders. Because of the dissimilar thermal expansion of these materials, temperature changes generate forces at bond interfaces. For stiff materials, these forces may be sufficiently large to cause fracture or fatigue failure. Given the prevalence of problems caused by temperature cycling in the aerospace industry, spacecraft environmental stress screening performed by APL includes both temperature cycling and thermal shock tests to screen for potential problems.

Prevention of temperature cycling damage usually requires attention to design or material selection. One common solution is to place an intermediate soft or spring-like material between the two high-modulus materials. The intermediate material absorbs the strain differences between the adjacent materials, reducing the overall stress. An example of this is the Tessera chip-scale package (CSP),[5] where silicone rubber is used between the low-expansion silicon device and the higher-expansion flex circuit. Alternative solutions include replacing high-modulus materials with low-modulus materials or improving the match in the coefficients of thermal expansion.

Temperature-induced damage may be particularly severe when using polymers near their glass transition temperature, T_g. Cooling a polymer below this level increases the elastic modulus of the polymeric material by several orders of magnitude, making the polymer much more stiff and brittle. Although going below the T_g does not damage the material, the change in modulus, coupled with its dimensional change, can cause unexpected fracture and fatigue. Concern for this failure mode has driven the APL Space Department to switch conformal coatings used on printed circuit boards from Solithane 113/300 (T_g = –10°C) to Uralane 5750 (T_g = –65°C) (G. Arakaki, personal communication, Mar 1990; also see Ref. 6).

In oceanic environments, exposure to corrosion can severely affect the performance and reliability of a circuit. Moisture, in the form of saltwater or condensing humidity, promotes corrosion of electronic circuits. Corrosion products may form between adjacent electrical conductors, creating an electrical short between them and interfering with overall circuit performance. In addition, corrosion may dissolve conductors, thereby severing the electrical path. The design engineer may incorporate design features to slow or prevent corrosion, such as conformal coating and encapsulation of the circuit boards.

System Partitioning and Modeling

After defining the top-level circuit, its environmental requirements, and its physical constraints, the system is partitioned into subsystems and components. Then, packaging engineers develop detailed designs that satisfy the requirements of the subsystems. At this point modeling is often used to predict the thermal and mechanical behavior of the system so that shortcomings in the packaging designs can be identified before fabrication begins.

Partitioning breaks down a system into logical elements, usually organized by function, testing needs, and physical size. Additional design considerations that affect partitioning may include standard circuit board sizes, thermal management, and available space. Partitioning is frequently organized by electrical function to aid in testability, such as having one circuit card dedicated to power supply or to data communications. Careful partitioning of the electronic circuit simplifies testing significantly.

In early Terrier missiles, the electronic components were hand wired, part by part, to the airframe.[7,8] As a result, the assembled missiles frequently failed acceptance tests because of a multitude of problems. The lack of functional subdivision made testing, troubleshooting, and repair difficult and time-consuming. Improved missile designs partitioned the circuits into subsystems (e.g., attitude control, telemetry, fusing), making the missile easier to assemble, test, and repair. This same functional division concept applies to the different levels of packaging.

Other issues besides testing drive the partitioning decisions. Partitioning usually accommodates the normal manufacturing sequence to minimize handling and cross-contamination. Systems may require additional volume and features to allow for repair, or they may be partitioned to minimize the amount of circuitry in an adverse environment. For example, on spacecraft, even though the sensors are exposed to the space environment, the boxes containing most of the support electronics are placed under thermal blankets to protect them from the temperature extremes and temperature cycling encountered in space.

Analytical modeling is an essential tool in the partitioning and development of reliable electronic packaging designs. Modeling offers significant cost and schedule savings for complex systems, particularly those incorporating expensive and long lead-time subassemblies. Using specialized software, electrical modeling can be performed to simulate circuit performance. The mechanical and thermal behavior of the system can be modeled using finite element methods[9] during power cycling, temperature cycling, and shock and vibration testing. By doing so, problems can be identified and fixed, with minimal impact on cost and schedule, before any hardware is fabricated.

Figure 2 shows how modeling can predict problems before assembly. Figure 2a is a schematic illustration of the full signal translator circuit board. Figures 2b and c illustrate the results of thermal and mechanical modeling. Thermal modeling predicts the temperature distribution across the board. Figure 2b shows that the ambient temperature must be kept at least 38°C below the critical junction temperature of the upconverter. The mechanical analysis in Fig. 2c shows the deflection of the assembled printed wiring board under a sinusoidal vibration. The software not

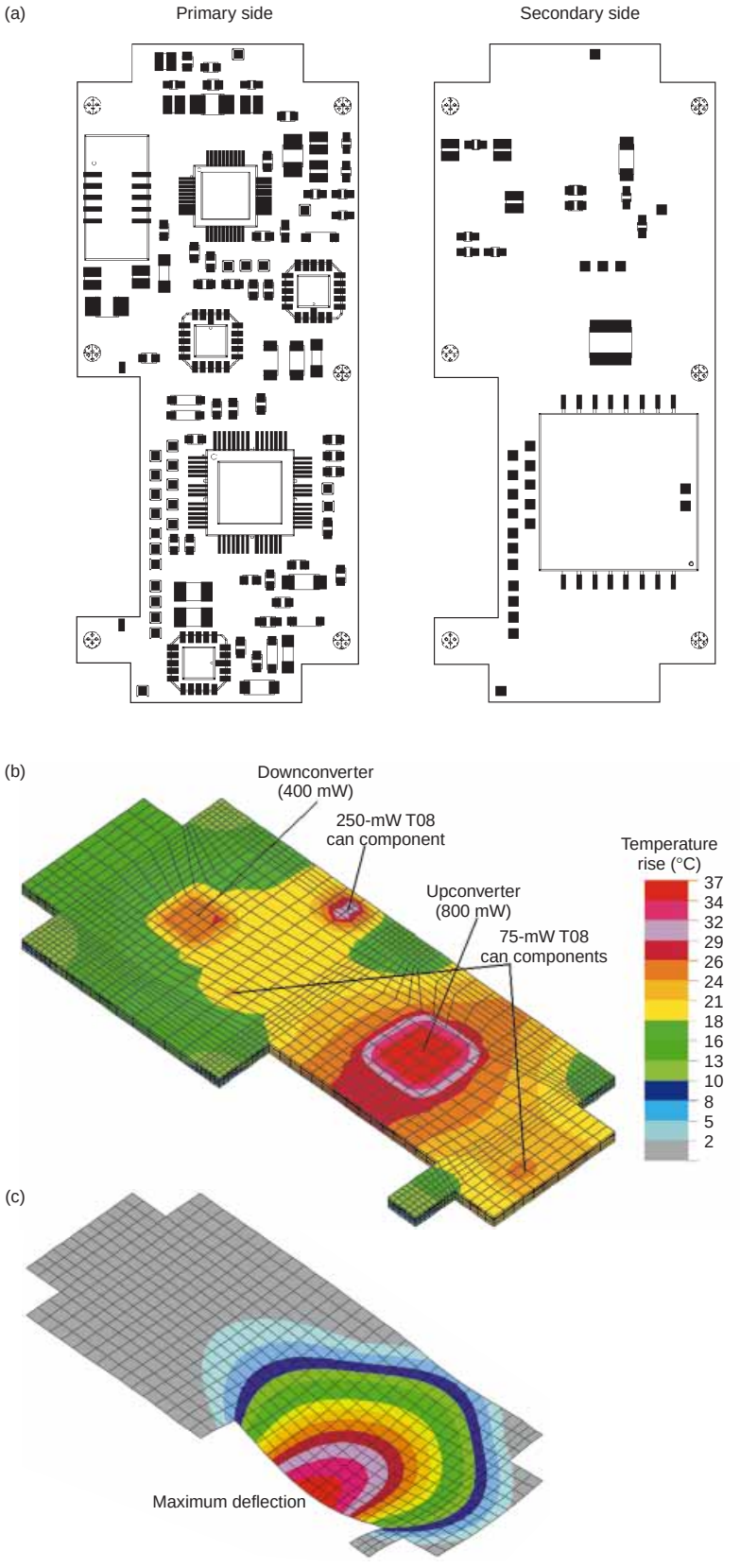

Figure 2. Modeling is used to predict problems before assembly. (a) Part locations on the front and back of a full signal translator (FST) circuit. (b) Thermal model of the FST showing predicted component and substrate temperature (and its distribution over ambient conditions). (c) Mechanical modeling showing first-mode deflection of the FST board in vibration; the mass of the upconverter causes most of the deflection.

only predicts the maximum deflection, it also predicts the distribution of the deflection across the board, accounting for variations in mass and specific locations of mounting points. By knowing the deflection locations and magnitudes at the design stage, additional stiffeners and mounting points may be incorporated in the design before the hardware is built.

Once the hardware is built, the thermal model is verified by measuring the temperature at critical locations. Since measuring deflection during vibration is somewhat difficult, strain or acceleration measurements obtained via gauges and accelerometers, respectively, may be used to validate the mechanical behavior of a model.

DEVICE PACKAGING

The first or lowest level of packaging is semiconductor device packaging. Not long ago, the selection of package styles was limited. The dual-inline package (DIP) dominated the semiconductor market and represented the majority of electronic packages sold. Today, with the drive toward miniaturization, combined with the lack of a clearly superior miniature package, many distinct package styles are available (Fig. 3), ranging from traditional DIP to chip-on-board (COB). They also range in price and area of substrate required for installation, each reflecting a different testing, assembly, and performance optimum.

The primary motives for packaging the device before assembly onto a circuit board are to allow for complete testing and to protect the device from contamination. Without packaging, testing of bare devices is expensive and difficult because of the tiny dimensions involved. When packaged, a device has far less stringent handling requirements than a bare device. Bare silicon devices must be handled cautiously in a clean-room environment. Soldering and normal handling during assembly leave contamination that often causes corrosive failure of unprotected devices. Improper handling easily damages the tiny wire interconnections on devices. For these reasons devices are usually packaged before testing and further assembly.

The design of the device packages is driven by many factors, including the number of leads and their routing on the substrate as well as the ability to dissipate the heat generated by the device. The external lead geometry must meet the customer's circuit board design constraints, assembly needs, and cost requirements. To conserve the space on a circuit board, customers frequently want the device in the smallest package possible. Smaller packages permit significant system miniaturization. Figure 4 shows how smaller packages may have the same number of leads as larger packages but cover a considerably smaller substrate area. However, miniaturization of packages frequently results in increased costs of assembly.

The redesign of the Glacier spaceborne imager built by the APL Space Department exemplifies how changing component packaging can reduce overall system size. The imager was an existing circuit design that was repackaged using several new packaging technologies (see the article by Le et al., this issue). By stacking dynamic random-access memory vertically, about a 5:1 reduction was realized in the number of packages, with a corresponding reduction in substrate area. Attaching bare, unpackaged devices directly to the substrate instead of packaged devices contributed to further miniaturization. However, these savings came at a price. Stacked memory chips are more expensive than separately packaged devices. Also, attaching unpackaged devices introduces a host of potential problems: unpackaged and incompletely tested parts create an increased amount of rework, increased rework difficulty, additional costs associated with encapsulating the device after attachment, and reliability unknowns found with any new assembly method.[10]

Device Packaging Processes

A variety of processes are used in device packaging. These processes create a package that shields the die from contamination and damage while electrically connecting it to the exterior. One of the most critical processes is the electrical interconnection of the device to the leads. This can be achieved through, for example, wire bonding, tape-automated bonding (TAB), and flip-chip soldering.[11] Historically, wire bonding has been the dominant method of interconnection. When a wire bond is made, the wire bonding machine welds one end of the wire to the device and the other end to the substrate or lead frame. Wire bonds

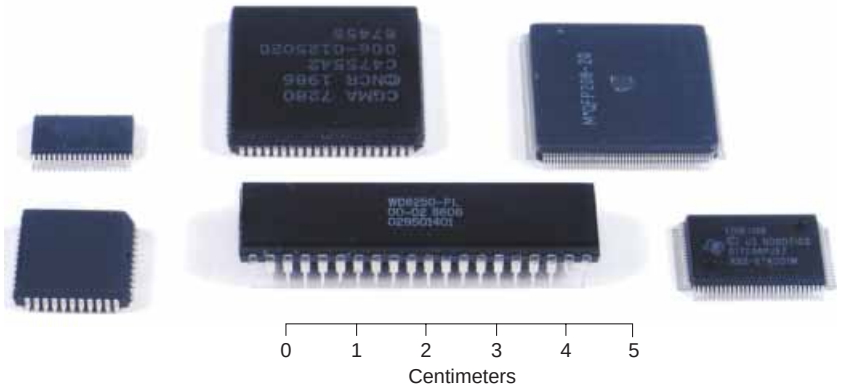

Figure 3. Some components available today are (clockwise from lower left) a 44-pin J-leaded plastic quad flatpack (PQFP), 20-pin thin small-outline package, 84-pin J-leaded PQFP, 208-pin QFP, 100-pin QFP, and 40-pin dual-inline package.

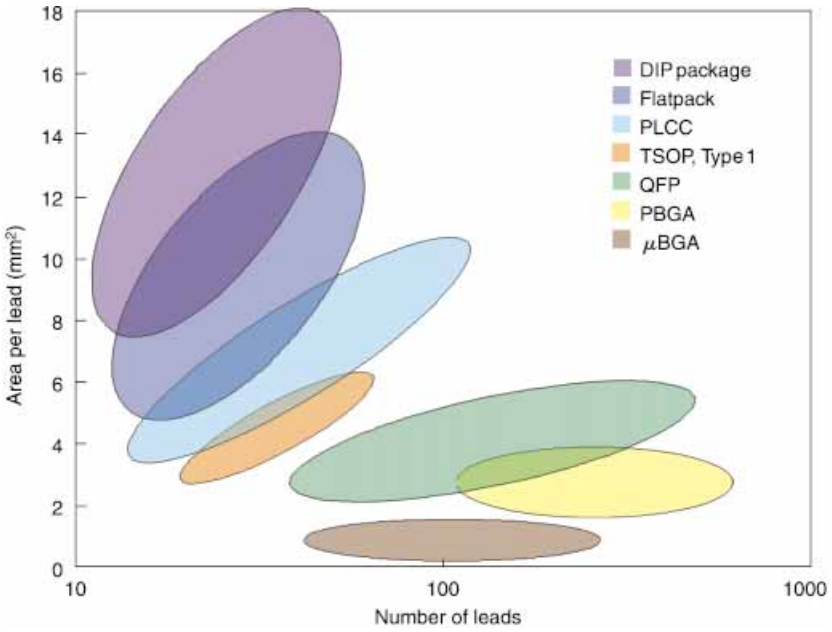

Figure 4. Plot showing the amount of substrate area required per lead and how this ratio varies with package style and total number of leads on the package. (DIP = dual-inline package, PLCC = plastic-leaded chip carrier, TSOP = thin small-outline package, QFP = quad flatpack, BGA = gall-grid array, PBGA = plastic BGA.)

are made using thin gold or aluminum-alloy wire, typically with a diameter of 25 μm (0.001 in.). Wire bonds are short, in the range of 1 to 3 mm (0.05–0.15 in.). Because they are so short and fragile, they impose additional packaging requirements. The frail wire bonds must be protected from damage and contamination, either by encasement in a rigid package or by molding in plastic.

In the 1960s, IBM developed an alternative to wire bonding, now called flip-chip technology, which uses a solder joint to form an electrical, thermal, and mechanical connection to the substrate. The flip chip process produces higher yields and more rapid throughput than wire bonding. Additionally, it requires less space on a substrate than wire bonding and permits rework. As expected, these advantages also have their cost. Flip-chip technology is more challenging to implement for much of the electronics fabrication industry. The process requires special metallization during wafer fabrication. A barrier layer and a solderable top-layer metallization must be applied over the aluminum bond pads to provide a solderable surface and prevent aluminum dissolution in the solder. The barrier layer must be compatible with a solderable top layer, protect the surface of the semiconductor device from contamination, and prevent undesirable metallurgical reactions between the solderable layer and the device metallization. Flip-chip technology also requires a nonstandard substrate and processing of the substrate to reduce the size of the pads, vias, and traces. For these reasons, the cost of a flip chip is about \$0.05 per connection versus less than \$0.001 per connection for wire bonding.[12]

The TAB method is an alternative to wire bonding and flip-chip bonding. It incorporates the bonding region with the lead frame fanout. A TAB structure typically begins as a thin laminate of copper on a polyimide film carrier. The conductors are etched out of the copper to form the electrical interconnection between the chip and the outside. The polyimide holds the copper conductors in place to facilitate rapid assembly. TAB technology uses several metallurgical coatings for conductors and bonding areas. Methods of connecting the TAB to the chip include thermocompression, thermosonic and ultrasonic bonding, and soldering. Joints may be bonded one at a time or simultaneously. The process is rapid and has found niches in certain markets. In low-volume markets (e.g., high-performance military electronics), TAB offers a highly reliable, high-performance interconnect method with a minimum of inductance and impedance. In high-volume markets, TAB offers a low-profile way to assemble circuits for applications such as digital watches and cameras.

Wire bonding, flip-chip soldering, and TAB may require additional features for mechanical and thermal interconnection. In wire bonding, the back of the device must be attached to a substrate using an adhesive, gold-silicon eutectic solder or a glass compound. The adhesive is often filled with silver or gold powder, making it electrically conductive and enhancing thermal conductivity. Because of the large surface area involved, device attachment provides a good thermal connection and high mechanical strength.

Flip-chip technology does not require additional mechanical attachment because the solder joints provide sufficient support to withstand shock and vibration forces. The flip-chip solder joints, by themselves, can dissipate considerable device heat. If further measures are needed to remove heat, two options are available. In the most demanding applications, heat may be removed from the back side of the flip chip through conduction by using a small block of water-cooled copper such as that used in the IBM thermal control module.[13] The second option is to fill the gap between the flip chip and the substrate with an encapsulant, called "underfill," to increase thermal conductivity. This underfill also provides environmental protection to the device circuitry and improves the thermal fatigue resistance of the solder joints.

Wire bonded, soldered, and TAB-mounted devices all require environmental protection from handling, contamination, and corrosion. This protection takes one of several forms. Devices may be sealed in the cavity of a ceramic or metal hermetic package whose walls are impervious to humidity and contamination, encapsulated in epoxy or silicone, or coated with inorganic materials such as silicon nitride. A common encapsulant is a filled epoxy that has been injection molded around the device and its lead frame. This material is used extensively for commercial components. As an alternative to injection-molded materials, a castable encapsulant may be applied, either as an underfill for flip-chip assembly or mounded as a "glob-top" over a wire bonded device to protect the wires.

Component Package Styles

One of the oldest and most common component packages is the DIP noted previously, which is fabricated in three basic configurations: molded plastic, ceramic, and side-brazed. The plastic injection-molded DIP dominates cost-sensitive and noncritical applications, whereas the ceramic and side-brazed packages, with their hermetic seals, are used in high-cost, high-reliability applications found in military, space, and demanding commercial electronic systems. The DIP has two rows of leads separated by 0.3, 0.4, or 0.5 in., with the individual leads spaced 0.1 in. apart. The size of the DIP is based not so much on the device size but rather on the area required by the spacing of the leads. The lead layout of the DIP consumes the greatest area per lead of any device packaging method.

The DIP package is being replaced with surface-mounted packages for a number of reasons. With devices becoming faster and more complex, the length of the component leads and substrate traces must be reduced as the number of leads is increased. The increased number of components parallels the need to reduce the overall size of the system. Surface-mounted packages satisfy these requirements in a variety of shapes and sizes (Fig. 3). These packages can be grouped into two general styles, leaded and area array. Figure 4 shows how surface-mounted packages, particularly area arrays, offer significant area savings when they replace DIPs. Area arrays are a class of packages that distribute leads on a grid pattern over the package bottom rather than only around its periphery; this method makes high lead count devices much more practical.

The area savings of surface-mounted components are often so great that substrate routing difficulties place more constraints on component density than the component size. A substrate designed to fully exploit the potential component density may have many layers and may be costly. By limiting the board thickness to four layers of metallization, the board cost can be reduced significantly with only a slight compromise of component density.

The number of leaded surface-mount package styles has proliferated without a single unifying standard. Several package design standards have been developed, each defining different package geometries and different lead layouts. Each package style has unique benefits and constraints. As the lead size becomes smaller and the number of leads increases, the difficulty of handling and installation increases. Some package styles are better suited for heat dissipation than others, a factor vital in space and temperature-critical applications.

The development of area array surface-mounted packages (Fig. 5) offers both the benefit of increased lead densities and a more forgiving manufacturing process. These packages distribute the solder joints, which number from 48 to over 1000,[14] across the bottom surface of the package instead of along the edges. This distribution allows for larger solder joints and an increased distance between them, thereby improving solder joint manufacturing yields and reliability. These solder joints provide both electrical connection and mechanical support for the component.

An early implementation of area array interconnects was the pin-grid arrays found on microprocessors in the early 1990s. Today, two leadless types of area array packages are being implemented, the ball-grid array (BGA) and the chip-scale package (CSP). The distinction between these packages is more an issue of scale than design. The BGA is larger and is built on a printed circuit board–like substrate. It has solder balls on the bottom in a grid with nominally 1- to 1.5-mm (0.04- to 0.12-in.) spacings. The CSPs are approximately 20% larger than the semiconductor devices they contain, having correspondingly smaller solder balls and grid spacings ranging from 0.5 mm (0.020 in.) to less than 0.1 mm (0.004 in.). To enhance solder joint fatigue life, the solder joints on CSPs are typically encapsulated with limited-expansion epoxy.

These package styles are so efficient in their use of substrate space that, to ease routing and reduce substrate costs, only the outer two or three rings of solder joints are often present or electrically active. Among the most significant factors that limit area array packages are their sparse commercial availability and the inability to visually examine the finished solder joints. This inability is a process quality issue that gives many companies problems. Nondestructive examination of the solder joints requires an X-ray machine capability that few electronic assembly companies possess. Transmission X-ray analysis detects many types of solder joint defects. A detailed, nondestructive analysis of solder joint shape requires X-ray laminography, but most companies are satisfied with nondestructive transmission X-ray analysis combined with sampling methods using destructive analysis techniques. With

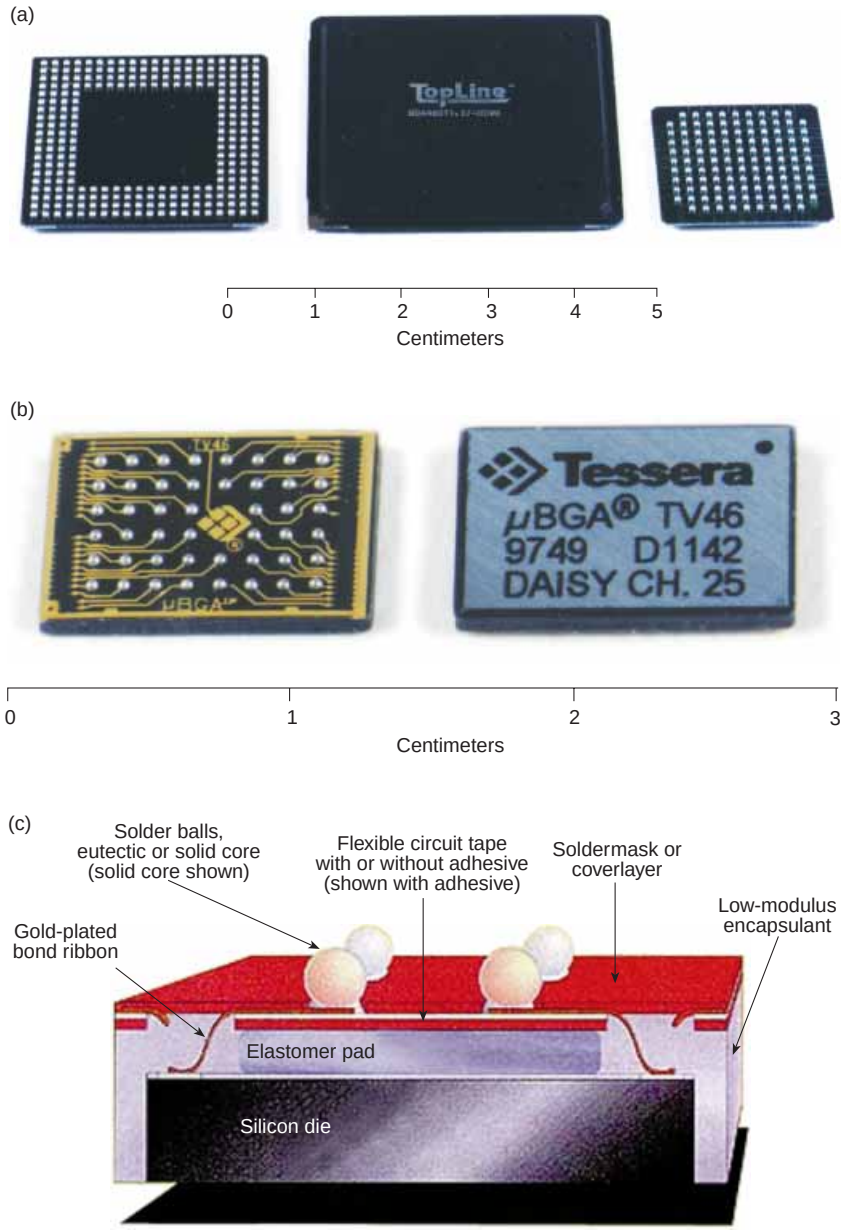

Figure 5. Several views and implementations of array packages. (a) Top and bottom views of a ball-grid array. (b) Bottom view of chip-scale packages (CSPs). (c) Cross-sectional view of a CSP. (Photograph courtesy of Tessera, Inc.)

the high yields possible with BGAs and CSPs, many companies choose to forgo the X-ray inspection of solder joints and, instead, monitor the assembly process closely.

Heat dissipation is usually not a problem for BGAs. For example, Olin has developed a high-performance 256-ball BGA (27 × 27 mm) package that, when dissipating 1 W, can be as little as 12.5°C over ambient temperatures with natural convection.[15]

The reliability of these new surface-mounted area arrays has been tested and found to be satisfactory for commercial applications; however, their history of use is short—too short to build confidence for space and military applications. Efforts are now under way to establish reliability limits for high-reliability applications.[16] Today, the use of BGA and CSP packages in these applications is limited to situations where no other traditional package can meet the requirements.

MULTICHIP MODULE PACKAGING

Sometimes it is advantageous to package several devices in one package, forming a multichip module (MCM). By combining individual devices and components into a single package, significant miniaturization is achieved over individually packaged devices mounted on a substrate. In doing so, multichip packaging muddles the distinction between device packaging and circuit boards.

The combination of Level 1 and 2 packaging into an MCM offers a significant advantage of low-volume, high-density packaging commonly found in the aerospace and military markets. In low volume, an MCM is an economical alternative to a custom-designed integrated circuit, since much of the miniaturization is achieved without the high initial cost of integrated circuit design. Many highly integrated devices began as an MCM before subsequent production volume justified a commitment to redesign as a single silicon circuit. The disadvantages to MCM technology over individually packaged devices are significantly higher costs of the assembly and decreased yield caused by using incompletely tested silicon die. Verification of device performance without packaging (i.e., the "known-good-die" problem) has received considerable attention in the electronics industry, but little progress has been made in the ability to do so. The critical issues are cost and system yield, for without the high probability of a working device, assembly yields are low (Fig. 6), and the test and rework costs increase exponentially.

Multichip packaging substrates range widely in cost and interconnect density. Those MCMs with printed circuit board substrates have the lowest cost and lowest interconnect density; those with single-crystal silicon substrates have the highest cost and highest interconnect density. Alumina and other

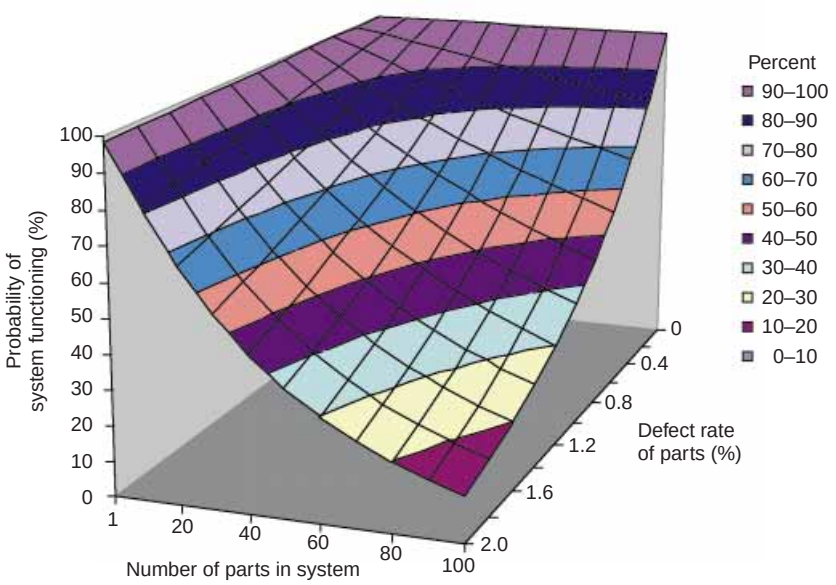

Figure 6. Plot of system yields (probability of functioning) with the reliability of the component and the number of parts in the system.

ceramic substrate technologies represent cost/density/performance trade-offs between these two extremes.

Traditionally, suppliers of MCMs for military and aerospace applications place them in hermetic packages constructed of ceramic, glass, and metal. Hermetic packages provide a barrier to moisture and relatively constant mechanical and electrical properties over a wide temperature range. A less expensive alternative is encapsulation of MCM circuits in an epoxy or silicone polymer. These encapsulants slow moisture ingress and mitigate corrosion, meeting the reliability requirements of many applications. Although their protection is not as assured, encapsulation is sufficient for many environments.

Multichip packaging has a long history of use at APL in satellites and special-purpose circuits (Fig. 7).[17] The Laboratory has fabricated MCMs on several types of substrates including silicon wafer, low-temperature co-fired ceramic, and thick film ceramic. These MCMs are typically mounted in hermetic packages that are sealed by soldering or welding. (See the article by Blum et al., this issue, for further details on MCM development at APL.)

THE CIRCUIT SUBSTRATE

The purpose of the circuit substrate is to provide a mounting surface and electrical interconnection for the components. For most electronics, the circuit substrate turns off-the-shelf components into a custom, application-specific circuit. Considerations in the choice of a substrate and its design include such assembly processes and performance issues as signal delay and capacitance. The circuit substrate should allow for testing and repair before integration into the next level.

In designing a circuit substrate, the shock and vibration environment of the application must be accommodated. Because components are small, damage from shock and vibration forces usually is not an issue in device packaging. With larger substrates like circuit boards, however, both mass and moment increase, thereby increasing the potential for damage. As noted earlier, typical methods to reduce shock and vibration damage include the addition of stiffeners and extra mounting points. Reducing the distance between mounting points mitigates the deflection from the shock and vibration and changes the fundamental resonant frequency. Adding stiffeners to the substrate may also reduce the deflection and stresses on the components.

Conformal coatings are applied to assembled circuit substrates for many purposes. If the circuit substrate is exposed to moisture and ionic contamination, it may require conformal coating to insulate the surface. Some circuits on the Tomahawk cruise missile are immersed in fuel, requiring conformal coatings that not only protect the circuit from corrosion but are also stable in fuel. The Space Department uses conformal coatings not so much to prevent corrosion but to dampen shock and vibration as well as to prevent stray metal contamination from shorting the circuit. Conformal coatings may have one of several polymer chemistries.[11] Polyurethane, silicone, and Parylene conformal coatings are commonly applied to circuit boards assembled at APL.

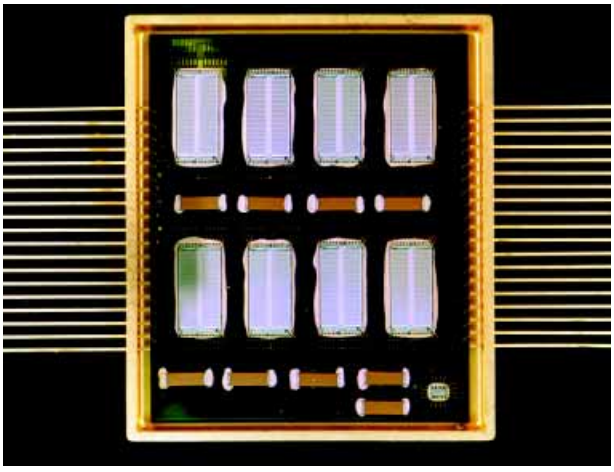

Figure 7. An APL-designed and -fabricated static random-access memory module using MCM technology. Module area is 3.5 × 4.1 cm.

A printed circuit board is normally fabricated as an epoxy or polyimide fiberglass composite structure. It contains layers of copper traces on the surface and within the structure that are connected by metallized vias. Components are soldered to the surface and in through-holes. The materials and processes used at APL to fabricate substrates were developed to maximize electrical performance within cost and durability constraints. For example, the coefficients of in-plane thermal expansion of the composite and the copper traces are similar, minimizing substrate warpage during soldering and temperature cycling.

Most vias extend through the entire thickness of the board, connecting any of the inner layers of the board to the surface. This configuration limits the routing of traces to the space between the vias. Blind and buried vias (i.e., vias that do not extend through the board) avoid this constraint but significantly increase the price of the board. A blind via extends from the surface of the substrate to a dead end at an inner layer; a buried via begins and ends on inner layers of the substrate. These special types of vias ease routing by limiting via length, allowing a trace to be routed above or below the area that would otherwise be occupied by the via. Although boards with these special types of vias are costly, they may still be more economical than the use of silicon or ceramic alternatives.

Several variations to the traditional board offer alternative packaging options. New advances in ceramic substrates and boards allow passive resistors and capacitors to be buried in the substrate, which frees up additional space on the surface of the substrate. However, these built-in components do not have the range of values, tolerances, or performance available from discrete components.

For high-frequency circuits that are particularly sensitive to capacitive coupling, the circuit substrate must often be constructed with a special, uniform dielectric material such as Duroid. The Duroid dielectric is a mixture of alumina powder and polytetrafluoroethylene that has a controlled, dielectric constant which varies little across the substrate. The copper traces on these boards are laid out using special rules to optimize circuit performance and minimize reflections. These rules include careful grounding, rounding the corners of traces, and choosing trace layouts with matched impedance to tune the circuit.

Circuit substrate technology has moved from the traditional flat, rigid boards to flexible substrates and rigid-flex boards, a hybrid of the rigid and flexible technologies. Flexible substrates are made from sheets of polyimide (e.g., Kapton), laminated with copper foil to form traces. These may have several layers like rigid substrates. Flexible substrates permit rolling and folding to fit the space available, which has many advantages in the packaging of electronics in constrained areas or in areas with odd shapes. It also permits the circuit to be assembled and tested flat, then folded into the available space. Many consumer electronic products such as cameras and watches contain such flexible substrates.

Rigid-flex boards combine the advantages of both flexible and rigid substrates. Such composite structures use flexible segments to connect rigid portions of the circuit board (Fig. 8). One common application of rigid-flex boards is for motherboards. Before rigid-flex technology, the motherboard was connected to the external connectors using up to hundreds of discrete wires. This manual wiring process was time-consuming and error prone. By substituting a segment of flex substrate for the discrete wires, the wiring process is reduced to soldering the connector pins onto a board, thereby eliminating problematic hand wiring.

CHASSIS-LEVEL PACKAGING

Chassis-level packaging connects the circuit boards and mounts them into a chassis, forming a system or subsystem. For many systems (e.g., personal computers), this is the level of packaging seen by the user. In satellites, this chassis-level package is connected to a structural frame and electrically connected to other chassis having different functions. The design phase of chassis packaging has similar mechanical, thermal, and materials considerations found in device and circuit board packaging. For APL's typical spacecraft and for most avionics applications, card guides hold the circuit boards by their sides in an aluminum housing, with a motherboard connecting the different boards (Fig. 9). This layout usually reflects the system partitioning to facilitate testing. Card guides ease insertion and removal of circuit boards while increasing heat dissipation. To facilitate electrical testing, extender cards can be used with this layout to probe individual boards while operating the entire box.

Traditionally, systems engineering allots each subsystem or major function its own chassis. Each chassis would be connected to the system through a power line and data bus and contain its own power supply and data transfer functions. To conserve space, reduce costs, and improve reliability, many newer systems are being packaged into a common chassis. These common chassis contain circuit boards for several electronic functions, located in one housing, on a common motherboard. By combining many cards and functions into one housing, redundant power supplies, data transfer circuits, and harnesses are eliminated. This increases packaging density and potentially improves system reliability. Although this packaging concept has advantages, it complicates testing, heat removal, and system integration. Because of electromagnetic interference, it

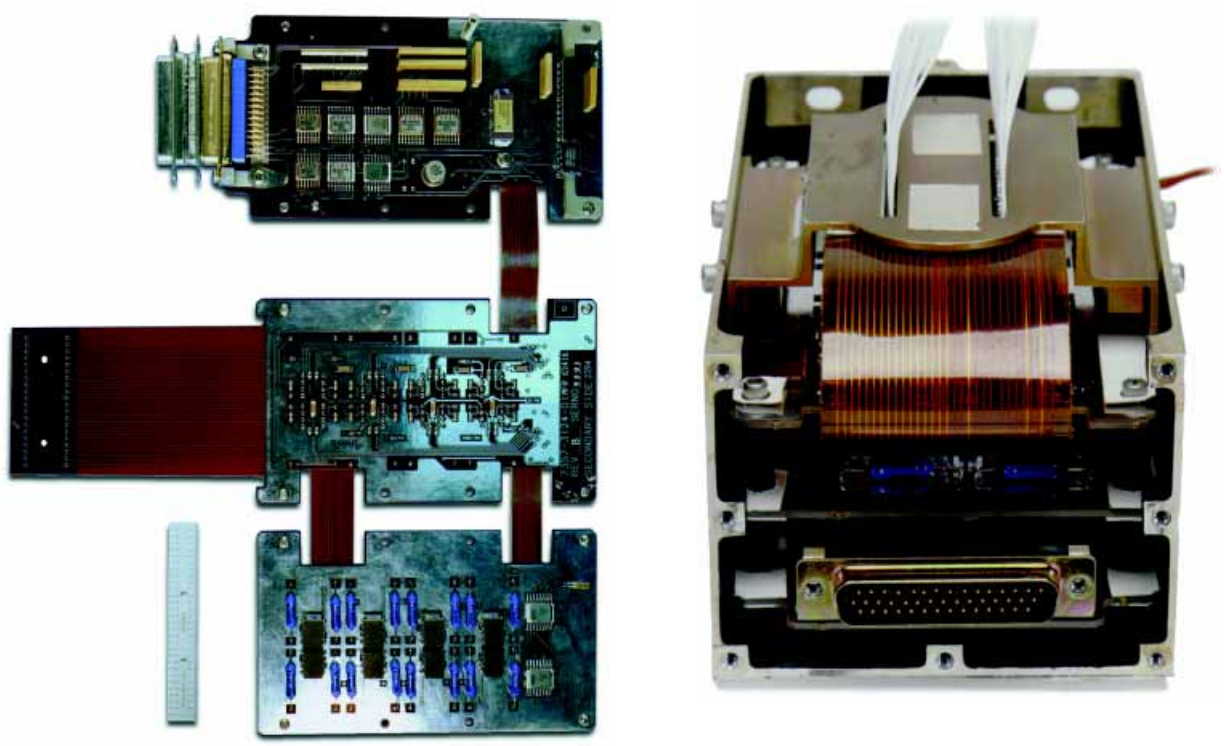

Figure 8. Four boards and their interconnections are combined into one rigid-flex assembly. The overall assembly size is 13.3 × 8.3 × 6.5 cm.

may not meet the special requirements of radio-frequency and microwave circuits.

A new development in card cages is the substitution of graphite-epoxy composite materials for aluminum.[18] With graphite-epoxy's high modulus-to-density ratio and high thermal conductivity, this substitution can reduce the overall weight of card cages. However, it also requires careful layout and analysis to achieve weight savings while meeting thermal dissipation requirements.[19] In choosing a composite card cage, the additional cost of design, analysis, and fabrication must be balanced with the potential weight savings and improvement in thermal performance.

CONCLUSION

Electronic packaging technology applies a diverse range of engineering practices to the packaging of electronic circuits. After the requirements, constraints, and environment of the electronic circuit are considered, the system is partitioned into component, substrate, and box levels, each one bringing unique but similar electrical, mechanical, and thermal concerns. Analytical modeling may be performed for each level of packaging to simulate the electrical, mechanical, and thermal behavior of the system to identify and correct problems in the design stage. To simplify testing, each level of packaging typically isolates a function of the electronic circuit. Although these levels may not always be distinct, they form the building blocks of the total circuit. As circuits become more complex and miniaturized, electronic packaging needs become more

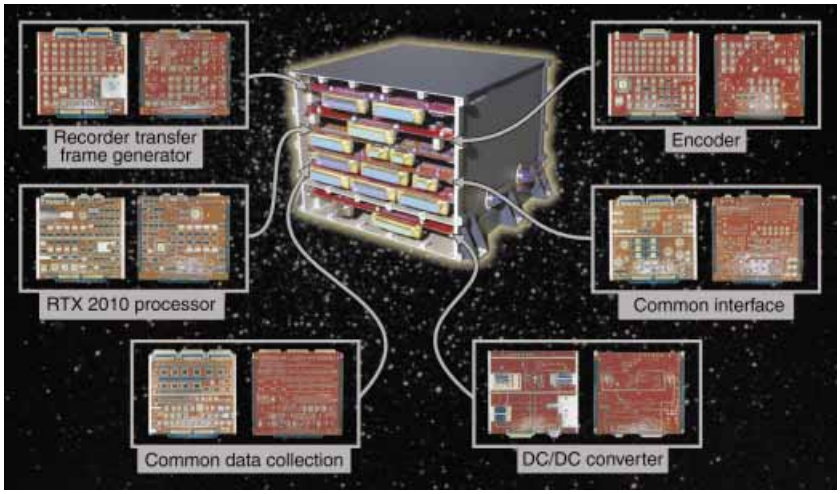

Figure 9. Exploded view of a box and circuit cards used in the Near Earth Asteroid Rendezvous command/telemetry processor (24.4 × 23.9 × 17.2 cm, 10.9 lb).

challenging, and careful electronic packaging becomes more crucial to mission success.

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THE AUTHORS

MATTHEW G. BEVAN holds a B.S. in metallurgy and materials science from Carnegie-Mellon University and an M.S. and Ph.D. in materials science and engineering from the University of Maryland, College Park. He joined APL in 1991. Dr. Bevan has worked in the Technical Services Department in both the Electronics and Mechanical Fabrication Groups, focusing on many areas of electronic packaging, from semiconductor to subsystem packaging. He has authored numerous publications in the field of electronic packaging and reliability. His e-mail address is matthew.bevan@jhuapl.edu.

BRUCE M. ROMENESKO is a Principal Staff physicist in APL's Materials Laboratory. He holds a B.S. in mathematics and physics from the University of Wisconsin and a Ph.D. in experimental solid-state physics from the University of Maryland. Dr. Romenesko is responsible for the packaging and failure analysis of high-reliability electronics, including hybrid microcircuits, solder/surface-mounted devices, and board-level assemblies. He has also been active in experimentation in microwave hybrid circuit reliability, radiation testing of electronics used in spacecraft programs, and ball-grid array packaging technologies. Dr. Romenesko has published over 40 papers in his field. He is currently a member of the IEEE and IMAPS, and serves as chair of IMAPS's Interconnections Subcommittee. His e-mail address is bruce.romenesko@jhuapl.edu.