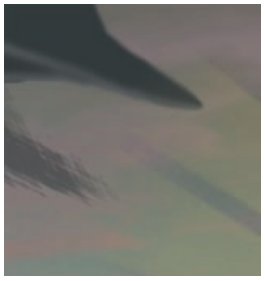

Coherent Data Collectors: A Hardware Perspective

Russell Rzemien

For more than 15 years, the Applied Physics Laboratory has been designing and operating coherent radar data-collection instrumentation. In this article, the engineering challenges and design approaches used to meet analysis requirements are described, examples of collectors are provided, and the nature of future development efforts is outlined.
(Keywords: Coherent signal processing, Radar analysis, Radar instrumentation, Radar systems, Test and evaluation.)

INTRODUCTION

Radar[1–3] is an acronym derived from the words *ra*dio *d*etection *a*nd *r*anging. The term reveals much about the operation and use of early radars. Those first devices used radio waves to detect the presence of objects and to measure the ranges of those objects. Modern radars frequently provide additional information, such as angular position and inbound velocity of an approaching target. However, the primary function of radar is target detection; all else follows from this. The detection problem remains a challenge, particularly with the development of stealth design techniques that significantly reduce the strength of the target's echo. Today's Fleet radars must detect those echoes even when they are buried in a background of "clutter" caused by reflections from objects in the environment such as the sea, rainstorms, or land masses.

Surveillance radars use either coherent or noncoherent techniques (and occasionally both) when detecting targets. Noncoherent processing uses the amplitude or strength of the echo to locate the target. Because clutter returns may be orders of magnitude greater in amplitude than those from approaching aircraft or missiles, processors that only use amplitude information may fail to detect these targets in such environments.

Far better performance is achieved by coherent radars, i.e., radars that use the phase or frequency information of the return echoes and not just the amplitude of the return signal. An echo's phase (or frequency) remains constant for stationary objects like clutter, whereas the phase varies for moving objects. It is this changing phase, along with the amplitude of the echo, that the signal processors in coherent radars use to discriminate targets from background clutter. In modern radars, the phase and amplitude information is frequently available as two digitized data streams called the I (in-phase) and Q (quadrature-phase) channels. Phase is calculated as arctan(I/Q) and amplitude as $\sqrt{I^2 + Q^2}$.

An effective coherent radar must generate a signal stable in both amplitude and phase. Instabilities in the transmitted pulse or spurious signals present in the receiver will affect detection sensitivity by, for example, raising the noise floor or detection threshold in the processor, thereby masking weak target returns. In some

cases, the processor may generate false detections (false alarms). Coherent data, collected and analyzed, provide a way to measure system stability, a means to determine target visibility in the presence of strong clutter, and a database to use for checking the accuracy of environment and target models used by the radar system designers.

Instrumenting a radar to collect coherent data can be complex. Unlike radar video, which is relatively easy to obtain and record, coherent data frequently require special interface circuitry both in the radar and in the collector. (*IEEE Standard Radar Definitions* defines radar video as the signal that remains after envelope or phase detection, which in early radar was the displayed signal. One can think of this as a process that removes the phase or frequency information, leaving only the amplitude or "strength" of the echo.) Data rates are usually several times greater, in some cases more than an order of magnitude greater, than video rates. Additional waveform and radar status data, such as transmitter frequency, pulse code, and pulse repetition interval, need to be recorded as well. Developing a device to perform this task and to meet program analysis and evaluation requirements is a significant technical challenge. The following sections describe approaches that have been successful in the past.

ESTABLISHING COLLECTOR REQUIREMENTS

Before design can begin, it is important that the system requirements be stated clearly. Is the collector needed to evaluate target detectability, or is there an interest in studying aspects of the radar environment, or both? Are specific performance parameters to be measured, such as how small a target, relative to the clutter, can be detected? This parameter is frequently called the subclutter target visibility. Are the data needed to determine how pulse compression affects target visibility in clutter? (Pulse compression is a technique whereby a long-duration radar pulse can be processed to provide a high-range resolution view of either a target or the environment. The compression technique usually leaves some residual "noise," referred to as range sidelobes, around echoes, and this residue may be greater than the echo of a small target of interest.) Answers to these questions will determine how much, how fast, and what type of data should be collected.

Another requirement might be to gather sufficient data for playback in studies of system performance on a global level (e.g., effectiveness of different processing schemes used in automatic track-while-scan processors). This requirement makes it necessary to collect all or most of the data at a continuous rate for tens of minutes. If, on the other hand, interest is limited to search radar performance against a particular target, data collection can be restricted to a particular region, or sector, of the surveillance volume. Use of this procedure significantly reduces the average data rate that needs to be stored by the collector.

Characteristics of the radar to be instrumented greatly affect collector system requirements. For mono-pulse track radars, the number of channels can be 3 or more times that required in a search radar because monopulse radars use several beams, transmitted or received simultaneously, to precisely locate the position of a target. To evaluate radar performance, several parallel data channels containing the results of this multibeam (but single pulse) interrogation must be collected. Thus, track radars are more difficult to instrument than search radars because the burst or instantaneous data rates are greater. Fortunately, for pulse radars, only a fraction of these data need be collected. Typically, a range gate, equivalent to a window in time, is established about the position of the target, and data need be collected only within this gate. The reduction of the average data rate is equivalent to that achieved by angle sectoring of the search radar's surveillance volume.

Environmental studies for search radars require global collection capability. The strength of a radar signal echo from clutter will fluctuate over time, and echo returns from different directions and at different ranges will also vary greatly. Statistical measures of the clutter, such as the mean echo strength and the standard deviation of the echoes' returns, are used to help characterize the clutter environment. A small sample of data, e.g., from one or two pulses, over a limited range will not be sufficient to determine these statistics, nor is it possible to process such data and accurately determine the false alarm rate that would result from operation in this environment. It is also difficult to determine where best to position the collection "slice" or to convince oneself that the slice of data collected is truly representative of the environment (Fig. 1).

More fundamentally, even if analysis could obtain the correct parameters to specify, for example, the probability distribution describing the clutter's normalized cross section, such a representation is somewhat misleading. The radar processor will not see the long-term average clutter but must deal with the spatially clumpy nature of the clutter. This is particularly true for land clutter, where shadowing effects cause echoes to be zero for extended ranges followed by areas of large clutter returns. Sea clutter tends to drop off in amplitude, more or less smoothly, with range from the radar. Figure 2 shows these characteristics, though the range scale does not allow one to appreciate the relatively smooth fall off of sea clutter.

The collector designers must take all of these considerations into account. The data rates from the radar largely determine the speed of the input circuitry. The average data rate and length of data collection events,

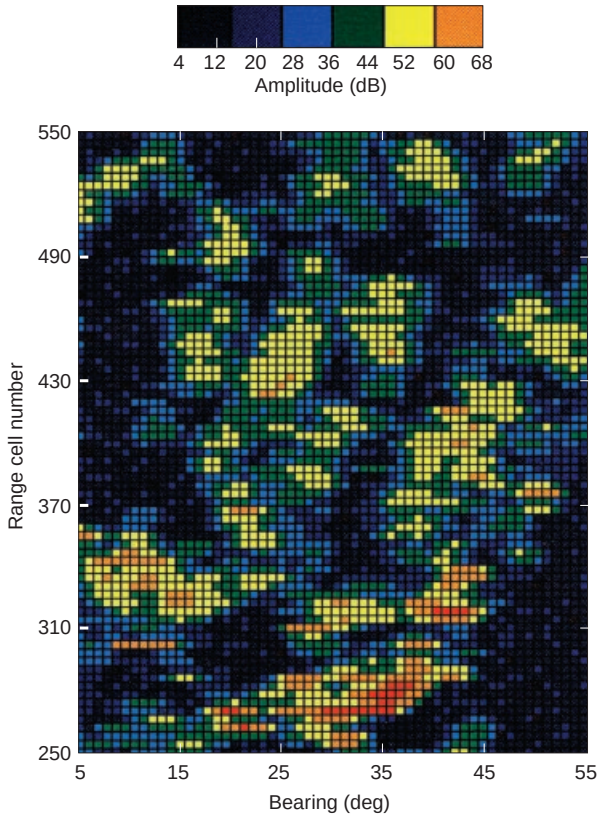

Figure 1. Land clutter data from a surveillance radar. Each column represents echoes from a single pulse. The nonhomogeneous nature of the clutter is apparent.

as established by program requirements and what is technically and financially feasible, determine the minimum acceptable speed and capacity of the output storage devices. The number and types of data sources and the formatting requirements, along with the foregoing considerations, determine the overall architecture of the device.

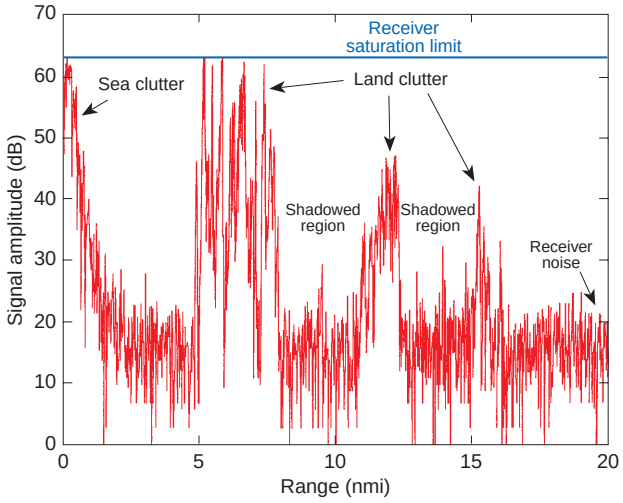

Figure 2. Echoes from a single pulse showing in-close sea clutter and land clutter with shadowing. nmi = nautical miles.

EFFECT OF THE RADAR ON DESIGN

The rate at which the collector receives data is determined primarily by the radar set's analog-to-digital (A/D) converters. Conversion rates for these devices are chosen to ensure capture of the return echo, regardless of the time at which it is received. Therefore, at a minimum, samples must be taken with spacing equal to the transmitted pulse width. (Radar front-end processing typically stretches the received pulse so that the processed echo will not "hide" between samples.) Some loss in signal amplitude results from this minimum sampling, but the loss is normally not enough to justify oversampling. (Oversampling occurs when the time between A/D conversions is less than the time duration of the transmitted pulse.)

The conversion rate multiplied by the number of bits per converter determines the data rate from each channel. The number of bits chosen for use in the radar depends on many factors, such as system dynamic range requirements, subclutter visibility, and type of signal processing performed in the radar. Cost is an important factor, since an A/D converter, which contains more bits, is more expensive. In addition, the added bits must be maintained and processed, which increases the cost of the processor.

Other radar parameters, such as transmitter frequency, pulse code, antenna pointing information, and track gate location, add to the total data rate. These additional data will significantly affect the collector design but usually not the data rate throughput, since most of this information comes relatively infrequently compared with the I/Q data. The radar system data do affect analysis and can be used in the collector for data gating decisions, particularly the antenna azimuth and elevation (if relevant) pointing information.

It can be difficult to physically extract these data. Most modern radars do not provide external ports into the electronics at the level needed to support coherent data collection requirements, largely because of the added cost. During early development work, many of these data points are accessible as test ports in some form or another, but once the system is moved to production, these test ports are removed. In other cases, the data are simply not available in a convenient form for data extraction. In an age of high-performance digital signal processing chips and very-large-scale integration, many processes can be performed on a single circuit card, with intermediate results never appearing external to the processing devices.

Given that the data are available, routing those data to the external instrumentation is the next consideration. Instrumentation interfaces that degrade system performance significantly reduce the number of collection opportunities. This is especially true if data collection is desired in locations where ships must be at maximum readiness state, where it is essential that the

instrumentation have minimal or no system impact. Thus, the data extraction process should not affect system performance. Sometimes this requirement is not necessary, particularly if the collection or test requirements dictate modifications to the radar set. Such a test might involve modifications to the radar waveform to determine the effect on performance. The radar set, itself, might not be able to process the new waveform, but the data can still be gathered and later analyzed by processor simulations.

Normally, the interface must provide buffering of output signals and minimal loading of signal lines. The buffering reduces the likelihood of inducing noise or signal spikes into the processor via the cables between the radar and the collector. Minimal loading averts timing problems and maintains noise margin. If special interface circuitry must be added, for example, to provide drivers for signals, care must be taken to make sure that the new circuitry and any added wiring do not create noise or timing problems. Finally, for analog signals, care must be taken to extract those signals without corrupting coherency or inducing noise.

The complexity of the collector and its interface also affect total design cost and parts procurement dollars. As in most programs, trade-offs between cost and capability have to be made. The final system design will reflect these considerations. Time constraints may affect design by forcing engineers to produce a simpler, less capable system.

COLLECTOR ARCHITECTURE

Data collectors differ in terms of capability, as do the radar systems that they are to instrument. The basic functions of these devices are similar. Figure 3 is a block diagram of a generic coherent data collector (CDC). It shows the major functional components and the overall architecture of such devices. There is an interface to the radar consisting of circuitry in the radar and in the collector processor. The processor provides internal test circuitry, data control and formatting, high-speed buffer memory, a system controller, input and output to peripherals, and operator controls and monitoring functions. Implementation considerations for each of these are described next.

Interfacing to the radar set may require long cables running to the processor, particularly when the radar equipment and collector are not located in the same compartment. The driver electronics for the signals, typically located in the radar or an auxiliary electronics box near the radar, provide both the power (current drive) and the noise immunity needed to ensure signal integrity. Differential drivers are used. These drivers send a signal as a pair of complementary signals, i.e., each is an inverted version of the other. Differential receivers in the collector will "decode" these pairs, accepting for any particular pair only signals that are simultaneously present as inverted versions. The pairs are sent via twisted pairs of wire. Noise coupling onto these data lines normally results in voltages of similar level and the same polarity on both wires of the pair. This "common mode" noise is rejected at the receivers, thereby providing noise immunity even for long cables, where coupling between signal lines can be a severe problem.

Internal test circuitry is provided to allow the electronics to be debugged during initial system development and to have built-in test capability once the unit is fielded. This circuitry simulates as closely as possible the timing and nature of data expected from the radar. The collector will have been thoroughly checked out by means of this circuitry before integration with the radar set is attempted. This procedure leaves only subtle timing differences for which one must account. For systems with short development times, this circuitry is invaluable, particularly if the schedule allows only a brief integration period for the collector and radar set.

Once the data have entered the collector, they must be formatted to provide both efficient packing of data and proper labeling of the data for use in analysis. The number of bits of I/Q data seldom add up to 32. However, internal bus circuitry and memory cards used in these systems prefer a 32-bit bus or data stream. The formatting circuitry adjusts the incoming data to fit this bus, thereby eliminating excessive overhead. For example, a radar system may have 12 bits of I and 12 bits of Q data. The hardware is less complex if one packs these data as a single 24-bit word, leaving the remaining 8 bits unused. Unfortunately, this 25% overhead effectively decreases useful throughput by the same percentage. Most systems cannot afford this waste, both in terms of speed and total storage capacity.

Other data received from the radar, such as the frequency of the transmitted pulse and pulse code, are packed as needed into header words or trailer words that

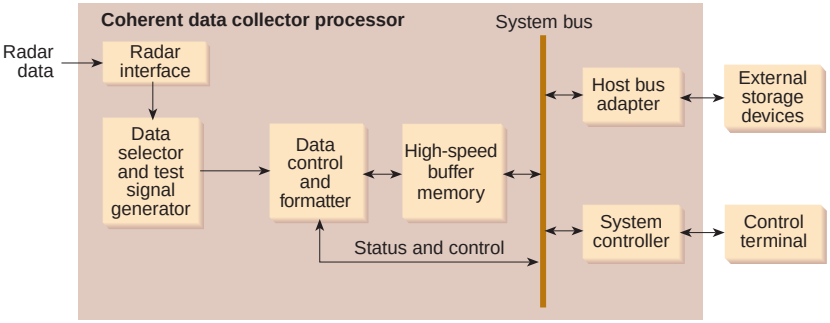

Figure 3. Block diagram of a generic coherent data collector. The radar data are usually buffered digital data.

bracket blocks of I/Q data. Just as formatting words into 32 bits is most efficient, so too is blocking data into groups of words that are large binary multiples, such as 4,192 or 16,384 words. These blocks of data are labeled with header and trailer words, which together with the data words add up to appropriate binary multiples. The overhead incurred by creating these words is typically less than a fraction of a percent. They are invaluable during system development and essential during data analysis.

The formatted data are bussed to high-speed memory circuit cards for temporary storage. These buffer boards are typically dual-ported, commercially available cards. Dual-ported means that data can be read into the card on one port while other data are being read out of the other port. The output of the buffer boards typically is read on the system bus at appropriate times determined by the system controller board. The buffer boards used in modern collectors can hold tens or hundreds of megabytes of data, allowing whole scans of radar data to be stored on one or two of these boards. This storage allows the data to be sectored under software control, as opposed to hardware gating. Earlier collectors created gates in range and bearing by comparing the current azimuth angle of the radar with switch settings for start and stop collection angles as set by the collector operator. Hardware gating is effective but somewhat cumbersome and does not allow automatic sector steering such as is possible via software control. The use of commercially available memory cards allows the flexibility of controlling data over commercial busses with open standards that are well understood and well supported by a variety of products and vendors.

Regardless of the buffering technique, collected data must be read into permanent storage of some type. Two configurations are typically used. The most desirable sends the data directly to magnetic tape. This method provides permanent storage with essentially unlimited capacity, since the amount of data stored on tape allows for long periods of continuous collection, and the time to remove and insert a new tape is small enough that it does not affect the overall quality of the collected data. (If even small gaps are unacceptable, a ping-pong mechanism is established that allows on-the-fly switching of the data stream to a second tape-drive unit. The tape in the first unit is then replaced, and the unit is made ready for collection while the second unit is recording). Unfortunately, affordable tape-drive units provide, at best, a storage rate of only a few megabytes per second. This capability is impressive when one considers that state-of-the-art tape-drive units available only 15 years ago had a storage rate of only approximately 150 KB/s, and 20 years ago, the storage rate of most tape-drive units was only 15 KB/s.

Requirements for some collectors significantly exceed tape-drive capability. During the early 1990s, the storage rate of affordable tape drives was 0.5 MB/s. In most cases, this was insufficient. For example, the throughput requirement for the AN/SPS-48E CDC is approximately 4 MB/s. (The AN/SPS-48E radar set is a long-range air surveillance radar found on many classes of ships, including aircraft carriers and Spruance-class destroyers.) To meet these requirements, a parallel disk array (PDA) was used for temporary storage (Fig. 4). The PDA uses several hard disk drives, each

Figure 4. Parallel disk array, keyboard, and monitor screen housed in shock-mounted enclosures. This configuration was originally designed for use aboard a target ship, where sonic booms and generally rough operating conditions make it necessary to protect the hard disk drives from excessive shock. This system can store up to 2.6 GB of data at up to 8 MB/s. It has been used with the Phalanx coherent data collector (CDC), the AN/SPS-48E CDC, and the AN/SPS-48E auxiliary detection processor.

with a storage rate of approximately 2 MB/s, to achieve the desired performance. Because of the parallelism, total storage capacity increases as well as speed. The capacity is limited, making it necessary to download the data to magnetic tape at some point. In most cases, this is not a severe limitation. The devices listed in Table 1 show the transition from tape-only to PDA systems. This mix will probably continue into the future as requirements become more demanding and both tape drives and PDAs become more capable.

The interface to the PDA is usually based on a proprietary bus structure developed by the manufacturer. Fortunately, most manufacturers provide host bus adapters, which allow data to be sent to the PDAs by way of the system bus. PDAs used in these devices have these adapters, which plug into the VERSAbus Eurocard (VME) bus standard. This bus was chosen for the collectors since it is well supported in the industry, very flexible, and well understood by engineers at APL. As will be mentioned later, future systems may migrate to other bus standards.

The system controller serves several functions. It is the primary interface of the operator to the collector. It allows the operator to perform self-tests, establish collection sectors, start and stop collections, and test collected data. The extent of these capabilities depends on the system. Typically, self-tests are limited to selection of fixed test patterns for input data at the front end of the processor and subsequent collection and data verification. Because the test data occur at the expected radar data rates, this test is very powerful in both system development and later checks. Testing of collected radar data is limited to checks of data header and trailer information and verification of pulse repetition intervals. More extensive data checks are performed off-line using data reduction equipment that accompanies the collector. The system controller also provides status and error information, allowing the operator to detect problems early.

Finally, although this article is about collectors, this capability is sometimes integrated into radar processors. The collection capability can stand alone in the processor, simply providing a data extraction capability, or it can operate in parallel with the processor. In some cases, the extraction capability can be used in a playback mode, allowing data to be read from storage back into the processor in real time. (Real time refers, in this case, to the ability of the storage system to input data to the processor at the same rate as data coming from the radar.) This capability is very valuable, since it allows systems to be retested under essentially identical conditions. This alternative is far less expensive than land-based or at-sea testing.

EXAMPLES OF PREVIOUS DESIGNS

APL has been building and operating coherent data collectors for over 15 years. Table 1 lists radar systems that have been instrumented and their input and output data rates. In the review of these devices that follows, areas are highlighted in which technological advancements have resulted in improved collector capability.

The first coherent collector was built for the AN/SPS-40, a long-range surveillance radar, to support development of simulators for training radar operators. The collected coherent data were used instead of simulated data. This database provided trainees with a realistic picture of the environment and allowed them to test the effectiveness of the available radar processes. The collector was unique for its time because it generated I/Q data with a single analog-to-digital converter. Digital coherent data were obtained by double sampling the intermediate frequency (IF) line in the

Table 1. Radar systems for which APL has built coherent data collectors, and their capabilities.

Radar system	Date	Burst (MB/s)	Sustained (MB/s)	Storage medium
AN/SPS-40	1981	1.3	0.015	9-track tape
Mark 92 CORT	1983	80	0.145	9-track tape
Phalanx Block 0/1	1984	15	1.1	Hard disk/9-track tape
AN/SPS-48E	1989	6	0.1	9-track tape
TAS Mark 23	1991	1	0.2	8-mm tape cartridge
AN/SPS-48E DMTI	1991	8	8	PDA/8-mm tape cartridge
AN/SPS048E APD	1991	8	8	PDA/8-mm tape cartridge
Tartar Mark 74	1993	10	8	PDA/8-mm tape cartridge
Phalanx baseline 2	1993	15	8	PDA/8-mm tape cartridge
Mark 92 MRP	1994	10	10	PDA/8-mm tape cartridge
Mark 92 MOD 6	1994	80	12	PDA/8-mm tape cartridge

Note: The burst column refers to the data rate as seen directly from the radar into the processor. The sustained rate refers to the amount of data that must be continuously stored and is the fraction of the data that remains after range and/or bearing sectoring. The storage medium refers to both the temporary storage to hard disks or arrays and the permanent storage to magnetic tape. CORT = coherent receiver and transmitter; TAS = target acquisition system; DMTI = digital moving target indicator; APD = asynchronous pulse detector; MRP = Mark 92 radar processor; MOD = modification; PDA = parallel disk array.

receiver at a rate such that consecutive samples were shifted in time by 90 electrical degrees.[4] Much of the remaining circuitry was based on designs used in digital noncoherent collectors. Throughput was limited to a maximum rate of 15 KB/s. In 1981, this was a respectable data carry-away rate for a moderately priced tape-drive unit. The radar input data rate was 2 orders of magnitude greater, making it necessary to limit collection to very small sectors. In terms of characterizing the environment, this device was barely adequate.

The Mark 92 coherent receiver/transmitter and the Phalanx close-in weapon system Block 1 development programs sponsored development of a new generation of coherent collectors.[5,6] (The Mark 92 fire control system radars provide surveillance and tracking capabilities primarily for Oliver Hazard Perry class frigates. Phalanx radars provide short-range detection and tracking capabilities in support of gunfire engagements against attacking targets. Phalanx is found on most classes of Navy ships.) These devices made use of several new technologies to meet requirements. Streaming tape drives, which achieved high speed by writing continuously to tape, had become affordable and offered a 10-fold increase in sustained storage rate. Note that the 80-MB/s burst rate for Mark 92 refers to the track radar. The search radar input rate is 30 MB/s. This Mark 92 CDC used both range and azimuth sectoring to reduce the sustained data throughput.

Although the data throughput was sufficient for Mark 92 requirements, Phalanx required almost another order of magnitude increase in throughput primarily because the pulse repetition interval for Phalanx is much smaller than that for Mark 92 (Fig. 5). (Range sectoring, a technique that limits data collection to only those ranges selected by the operator, is undesirable for short pulse repetition intervals since the waveform is highly range ambiguous and gaps in the recorded range lead to unacceptably large gaps in the data record.) APL developed a simple two-disk array, a forerunner of the more complex parallel disk arrays used today. This collector distributed the data to obtain approximately twice the sustained storage rate as a single disk. This is a nontrivial task requiring, among other things, a means of synchronizing data rate to disk spinning rate so that head seek time does not excessively degrade throughput.

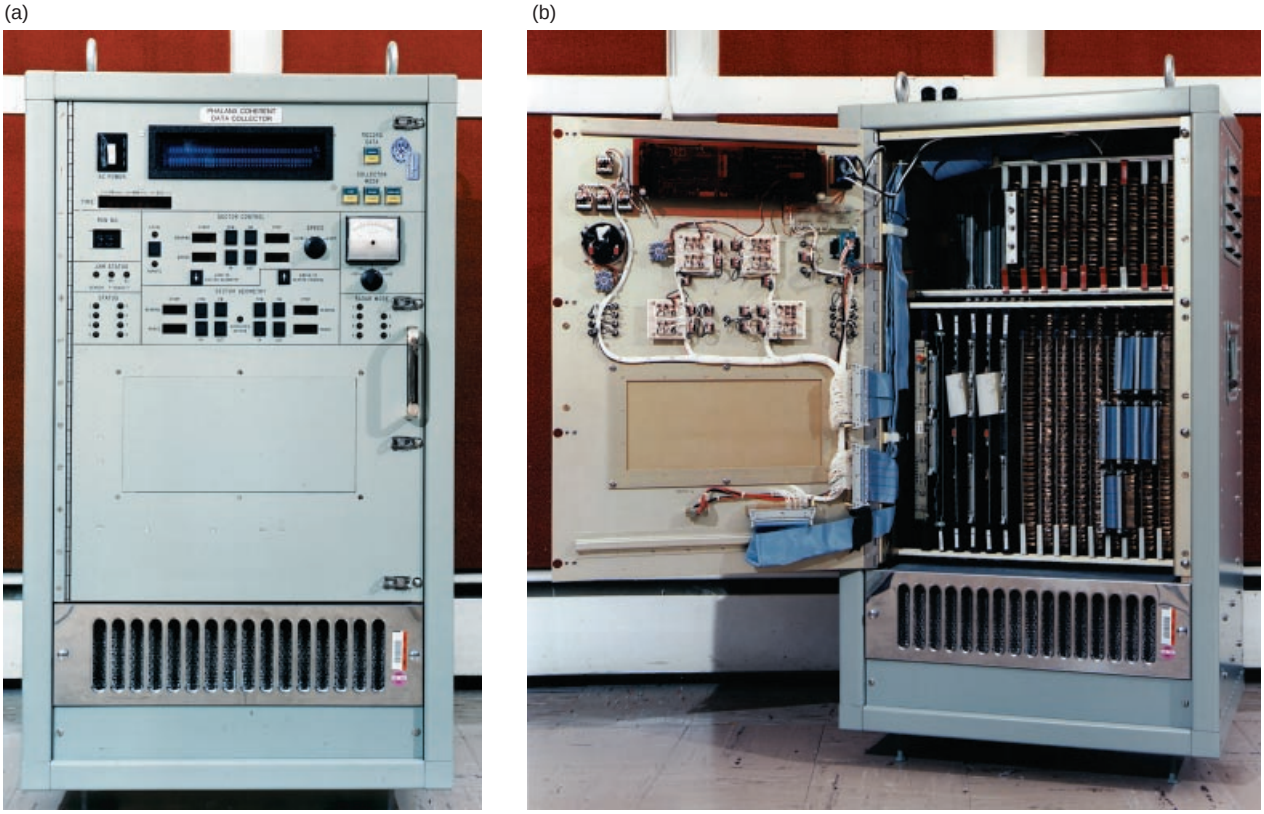

Figure 5. Phalanx coherent data collector (CDC) processor. (a) Exterior view. Note the push buttons centered on the front panel. These, and the corresponding displays, allowed the operator to select and direct the data-collection sector. (b) Interior view. The panel door wiring is mostly to support the collect sector setup and control. This circuitry became unnecessary on later CDCs when data sectoring came under software control. The card cage has an upper rack for custom wire-wrap boards. The lower rack is in the old VERSAbus standard. Approximately two-thirds of these cards are custom-designed wire-wrap cards.

Both collectors used a new system bus architecture called VERSAbus. (A system bus is a means of moving processing and control information between components of a system.) VERSAbus was the forerunner of the highly successful VMEbus. (VERSA was coined by Motorola for their proprietary bus architecture; VMEbus stands for VERSAmodule Eurocard bus). An industry-standardized bus structure was essential for providing a cost-effective system with the necessary throughput. Although system controller circuitry and host bus adapters were available in this form factor, both the Mark 92 and Phalanx collectors relied heavily on custom-design interface, control, and buffering circuitry. At the time, the VERSAbus market was new and not yet well supported by commercial vendors. Collection sectors were set by the operator using front panel switches. The terminal was used primarily to monitor system status, run a limited number of self-tests, and display small amounts of collected data on the screen to provide some capability for verifying the integrity of the collected data.

In the late 1980s and early 1990s, the successful use of these collectors in support of their respective radar development efforts led other programs to seek similar capabilities. In two cases, the AN/SPS-48E digital moving-target-indicator mode field change and the target acquisition system Mark 23 radar, it was not necessary to build separate collectors. Interface circuitry was designed that translated data from the radar set into a format compatible with the Mark 92 CDC. The remaining processor electronics met the narrowly defined goals of these programs, which consisted primarily of environmental clutter studies.

The next generation of coherent data collectors was developed using VMEbus. Radar programs using these devices were AN/SPS-48E, Tartar Mark 74 modification (MOD) 15, Phalanx, and Mark 92. VMEbus is the industry's best-supported open-standard bus architecture. Its use made it relatively easy to incorporate commercial boards that provided functions such as dual-port high-speed buffer memory capability, sophisticated system controller capability with built-in driver electronics for both the control terminal and the tape-drive units, and host bus adapter boards for interface to commercial parallel disk arrays. This last capability, from a hardware perspective, provides a near-turnkey system for data storage. Some device driver software needs to be written, but this task is relatively simple in contrast to the earlier work with the first Phalanx PDA. Perhaps the best feature of these new systems is the ability to perform better internal testing, data verification, system monitoring, and system control. A good example of the last is the ability to collect data periodically, shifting the collect sector in a predetermined manner. This capability allows automatic, unattended sampling of the environment over long periods of time.

The Tartar Mark 74 MOD 15 radar set CDC[7] made maximum use of this new architecture. It has interfaces to *three* sets of I/Q digital data channels as well as two naval tactical data system instrumentation ports. To support this capability, three banks of high-speed buffer memory cards were included. The system controller kept track of data from the five sources, writing it to the hard disk as needed. The device is unique in that it was the first such device built by APL at the request of an outside laboratory (the Naval Surface Warfare Center, Dahlgren, Virginia) for its use. After successful system integration aboard USS *California*, APL turned the device over to the sponsoring organization.

The AN/SPS-48E auxiliary detection processor was the first device of its kind to combine coherent data collection with both a coherent signal processor and coherent data real-time playback. The input data were time multiplexed to both the PDA host bus adapter and the signal processing electronics, all located in the same enclosure. For real-time playback, data were read from the disk and routed through the signal processor. This ability provided a means for checking the performance of processor software using realistic data at real-time speeds.

A similar concept was used in a processor developed by APL as an upgrade for the Mark 92 MOD 2 search radar. In this case, the data rates were too fast to allow time multiplexing of data on the system bus to support simultaneous collection and processing. A parallel bus architecture was developed that simultaneously routed data to a processor card cage and a data-extraction card cage. A card cage holds the circuit cards used in a system. The card cage was bridged using custom circuit boards and circuitry designed, fabricated, and tested at APL. In real-time playback, the data were routed from the data-extraction card cage to the signal-processing card cage via the custom boards. The playback capability was invaluable, particularly during early development of the tracker software, when data collected at sea on low-cross-section, low-flying targets were available for system debugging.

Most recently, new collectors have been produced for both the Mark 92 MOD 6 radars and the Phalanx Baseline 2 search radar. These radars use faster parallel disk arrays and more sophisticated system controller software to provide larger collect sector size, longer collect times, and greater system control. Phalanx required no significant changes in the collector architecture; however, the Mark 92 collector required internal bus restructuring. The input data rate for the search radar is approximately 30 MB/s. This rate is somewhat faster than the realistic input data rate to the dual-port memory boards used for the high-speed buffers. This situation was handled by development of separate parallel input ports to distribute the input data simultaneously between two banks of memory cards. The banks resided on the same system

bus, allowing the system controller to extract the desired data once they were loaded onto the cards. This enhanced capability proved its worth in testing aboard ships deployed in the Arabian Sea, where radar environmental studies require larger sectors.

FUTURE DESIGNS

In most cases, if one were to attempt to design a collector that can store all input data for an indefinite period of time, one would find that either the needed technology does not exist or it is too expensive. These are the main reasons why sectoring and temporary storage to PDAs are used in the collectors described. Fortunately, such solutions are adequate for most programs. For the Aegis SPY-1 radar, the situation is different. The data storage requirements, even in a minimal system, are daunting. To begin with, the total input data rate for all channels approaches 1000 MB/s. This severely stresses the input capabilities of electronics, unless one chooses to use massive parallelism to distribute the load. The task of sectoring the data, either before storage in the high-speed buffers or via selective data reads under system controller coordination, is substantial. Sectoring the input data can result in sustained throughput data rates on the order of 50–100 MB/s. Parallel disk arrays are available that support such rates, and host bus adapters can be found that will interface to them. However, the sustained throughput rates of the VMEbus will not. The task at this point is finding an architecture that will successfully move the data from the processor to the PDA.

There is a need for improved throughput in many systems, not just the data collectors. Technology continues to evolve in the key areas of parallel disk arrays, tape-drive units, and, particularly, high-speed data links. Several high-speed data busses have been introduced in the last few years that will eventually break the data-flow bottleneck on the VMEbus. Currently, the specified maximum data transfer rate on VME is 40 MB/s. This is an idealization, depending on instantaneous responses from the boards transferring the data. In reality, achievable rates rarely exceed 20 MB/s, with 16 MB/s being typical. The new VME64 standard (American National Standards Institute/VMEbus Industrial Trade Association 1-1994) provides significant improvements. First, the standard doubles the available data bus width, making realistic transfer rates of 40 MB/s achievable. Second, the new standard will eventually add several extensions that will formalize secondary high-speed data busses like QuickRing, RACEway, and SKYchannel. Third, the standard defines new input/output connectors that can be used for auxiliary high-speed busses between cards. These connectors will allow users to transfer data in parallel with other bus transactions and at much faster rates.

Table 2 shows the speeds for several of these data busses. Given the number and rapid development of these technologies, such a table can only be representative of what is available today in the marketplace. I have included the most popular of the available busses. The values represent specified maximum rates. The achievable rates can be 10–50% less, depending on implementation. In general, busses used for data transfer will be somewhat more efficient than those used for bus control because of overhead associated with the latter. For example, the version of small computer systems interface (SCSI, pronounced "scuzzy") frequently referred to as "fast SCSI" (theoretical throughput of 20 MB/s; actual throughput closer to 17 MB/s) must send control commands and set up transfers over the same signal lines used for the data transfers. (SCSI is a popular interface standard used to connect various types of peripherals to computers.) This situation forces a periodic interruption of the data stream, which results in the loss. Despite these caveats, these busses will play important roles in future designs. They will be used for the high-speed data transfers, possibly between several card cages, while overall data control is maintained within the familiar VMEbus architecture.

Parallel disk arrays are now available with storage capacities of hundreds of gigabytes and speeds in excess of 100 MB/s. These devices provide the performance; however, both the size and cost make them unattractive for most programs. This situation is improving rapidly as disk drives become smaller, denser (i.e., able to store more data on smaller physical disks), and less expensive. The commercial markets, such as on-demand video, network servers, and medical imagers, are driving manufacturers by their requirements of fast random access to a particular set of data residing on a mass storage device. Storage devices such as hard disks and compact disks are most suitable for providing this capability. The moderately priced magnetic tape drive units are slower and, consequently, will continue to serve as the download medium for the PDAs used in the more demanding applications.

Future collectors and processors must deal with the issue of how best to access the I/Q data from systems with multiple coherent data channels. Examples of such systems include monopulse tracking radars (i.e., a radar that uses a single pulse to obtain angular position information on a target by simultaneous comparison of two or more antenna beams), radars using coherent channels for both sidelobe blanking and electronic countermeasures detection, and radar systems with multiple antennas and parallel processing channels. The number of wires needed to output all the data can be prohibitive. Testing situations, especially aboard ships, limit the amount of such wiring that is acceptable to the ship and practical in terms of manpower and risk to the operational integrity of the radar system.

Table 2. The more common commercially available busses for system control and high-speed data transfer.

Bus	Mode	Speed (MB/s)	Medium	Distance	Comments
VMEbus	Parallel	40	Dedicated backplane	21-slot/19-in. rack	Open-standard, general-purpose bus.
VSB	Parallel	40	Backplane overlay	Up to 6 VME slots	Open-standard, general-purpose bus.
VME64	Parallel	80	Dedicated backplane	21-slot/19-in. rack	Open-standard, general-purpose bus.
SKYChannel	Parallel	320	Backplane overlay	8 slots plus 2 extender ports	Open-standard, general-purpose bus.
RACEway	Parallel	160	Active backplane	Extendable	Open-standard, general-purpose bus.
HIPPI	Parallel	100/200	Copper/optical	25 m/2 km	Interface standard for peripherals, processors, and supercomputers.
Futurebus+	Parallel	100–3200	Dedicated backplane	14-slot/19-in. rack	Open-standard, general-purpose bus. Note: Upper-end data rates are theoretical, based on 10-ns transfer rate and 320-bit data words.
SCSI	Parallel	1.5–40	Copper cable	3 m	Peripheral interface. There are several versions, such as SCSI I, SCSI II, and Ultra SCSI.
SSA	Serial	40	Copper/optical	20 m/680 m	Open-standard, control/data bus.
Fibre channel	Serial	16.6/133	Copper/optical	30 m/10 km	Interconnection standard for peripherals, mass storage systems, mainframes, workstations, and other high-speed devices.
Firewire	Serial	50	Copper cable	4.5 m	Open-standard, control/data bus.
FDDI	Serial	12.5	Copper/optical	100 m/2 km	Primarily used for local area networks.
ATM	Serial	19–78	User-chosen	>300 m	Data transmission technology, primarily for wide area networks.
Ethernet	Serial	1.25/12.5	Copper/optical	100 m/4 km	Networking system with many variations, such as 10base-2, 10base-5, 10base-T, and the 100base-x series. There is also a slower version at 1 Mb/s, but that is not considered here.

Note: Because new busses are being added all the time, this or any other table cannot be all inclusive. The busses listed are the better known ones. ATM = asynchronous transfer mode; FDDI = fiber distributed data interface; HIPPI = high performance parallel interface; SCSI = small computer system interface.

An analog approach, whereby the received echo and a phase reference signal are sent to an external analog-to-digital converter, will greatly reduce the interface wiring to the radar. This approach can be successful and was used for the first Phalanx CDC. However, care must be taken to ensure the spectral purity of the signals. Also, the full dynamic range of the system must be maintained. Unfortunately, such an approach does not indicate how well the radar, itself, actually performs these same functions. Such concerns are important for characterizing the environment, and they become critical when one is trying to assess radar performance. For example, problems associated with the analog-to-digital converters, such as induced noise spurs that corrupt the received signal, missing codes that corrupt the integrity of the digitized output, and output signal biases, might affect system performance and remain undetected when an analog interface is used.

In the end, the most desired approach would be built-in card slots that provide access to the appropriate data. The instrumentation installation team would bring along the required interface cards, which would

consist of digital buffering circuitry and high-speed parallel-to-serial converters driving fiber-optic cable to the CDC processor. The radar would have built into it card slots that make the required digital data available. Some radar manufacturers already do this because these test points are of value to them during their initial development efforts. Future development efforts should encourage this approach.

CONCLUSIONS

APL has been instrumenting coherent radars successfully for over 15 years. Innovative designs taking advantage of state-of-the-art technologies have resulted in the development of these high-performance devices. They provide the system designer and analyst with a unique, and much-needed, radar view of the environment. As APL moves into the 21st century, this type of instrumentation will continue to be needed for the development and evaluation of modern radar systems.

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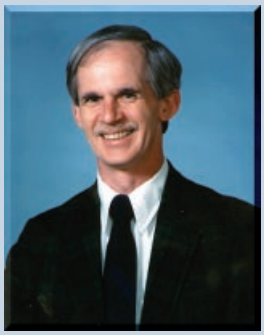

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