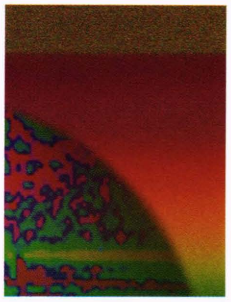

A Compact Polarization Imager

Karl E. Thompson, David M. Rust, and Hua Chen

A new type of image detector has been designed to analyze the polarization of light simultaneously at all picture elements (pixels) in a scene. The Integrated Dual Imaging Detector (IDID) consists of a polarizing beamsplitter bonded to a custom-designed charge-coupled device with signal-analysis circuitry, all integrated on a silicon chip. The IDID should simplify the design and operation of imaging polarimeters and spectroscopic imagers used, for example, in atmospheric and solar research. Other applications include environmental monitoring and robot vision. Innovations in the IDID include two interleaved 512×1024 pixel imaging arrays (one for each polarization plane), large dynamic range (well depth of 10^6 electrons per pixel), simultaneous readout and display of both images at 10^6 pixels per second, and on-chip analog signal processing to produce polarization maps in real time. When used with a lithium niobate Fabry–Perot etalon or other color filter that can encode spectral information as polarization, the IDID can reveal tiny differences between simultaneous images at two wavelengths.

INTRODUCTION

Many natural processes polarize light. Examples are everywhere: light emitted from stars, light passing through clouds or through lenses such as the cornea, and light reflected by metals and glass. Analysis of the polarization allows us to measure magnetic fields (on stars), diagnose disease (in eyes), and detect corrosion (in metals).

Polarized light has been studied at least since early in the Nineteenth Century, when W. Nicol described a crystal prism that can be used to detect linearly polarized light. A Nicol prism can show that the reflection off water is polarized (Fig. 1). One need only look through the prism and rotate it to see that light reflected from water varies in brightness with the orientation of the crystal. A complete specification of the polarization state is useful because it provides a more general description of light than does intensity alone. To describe the water's polarization scientifically, you must measure the light passed by the prism at a number of different angles. You can use a sheet polarizer, a modern invention, but both the prism and the sheet method pose a measurement problem that is very difficult to overcome. In the time between measurements, the water's brightness will certainly change, even if only

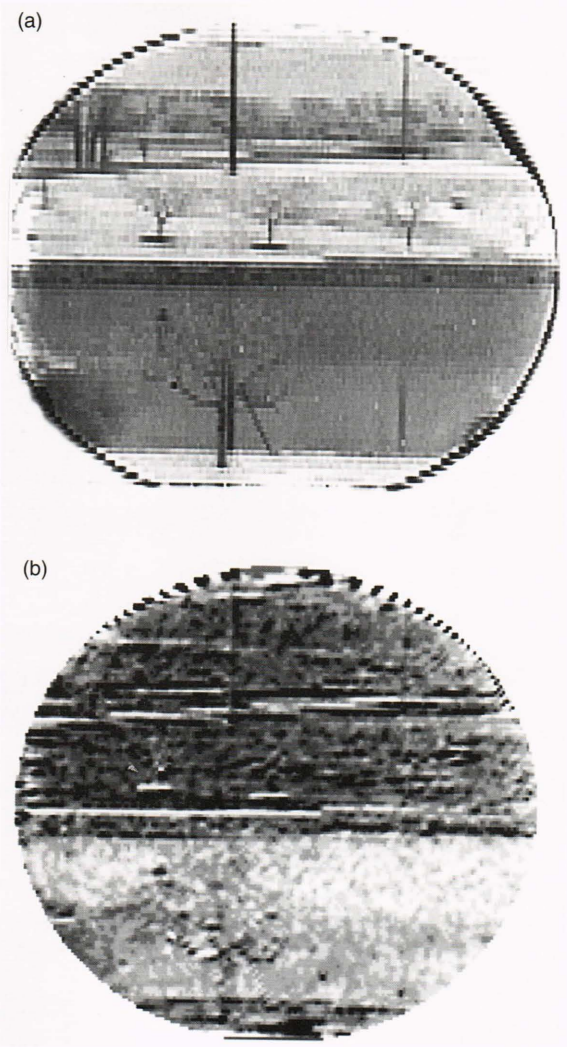

Figure 1. Polarization of light detected by the IDID. (a) View of the duck pond from APL's Kossiakoff Center looking out onto Johns Hopkins Road. (b) Polarization of the light in the scene in (a). Only the reflection of the sky in the water is strongly polarized (white).

slightly. It is difficult and sometimes impossible, then, to disentangle temporal brightness variations from the transmission variations associated with rotating the polarization analyzer. Also, motion of any optical element may change the transmitted intensity simply because of dust on the surface or nonuniformity of the materials. In general, the precision with which polarization can be determined is limited by instrument motion or flexure or by subject motion or distortion by atmospheric turbulence.

To fully characterize the polarization of light, at least five measurements must be made and their differences studied.[1] Even at TV rates (30 images/s), small scene changes between successive frames can seriously degrade some measurements. For real-time polarization imaging, an added problem is the high cost and complexity of data-processing equipment that can keep up with a stream of video images. Sequential measurements are satisfactory in many situations, especially in the laboratory where illumination can be controlled precisely and measurements can be repeated many times to remove random errors. In many applications, however, for example, in robot vision and astronomy, the atmosphere or the view angle changes rapidly. In this article, we describe a polarization sensor that can provide a precise, real-time, quantitative measurement of the polarization at all points in a scene by obtaining strictly simultaneous and cospatial images in two senses of polarization. We have built and tested a prototype of the Integrated Dual Imaging Detector (IDID), and we will describe the early results of our tests and our plans for an IDID that will offer significant advantages over this prototype.

The IDID was developed with support from the NASA Innovative Research Program. The design objectives were to make a compact, robust polarization imager that requires only scant power and computing resources and that will stay calibrated even when subjected to the severe vibration of a space launch, for example. Since the devices it replaces are heavier and include moving parts, it is one answer to the call for small sensors that can be carried aboard smaller and cheaper spacecraft. There are other answers, for example, arrangements with beam-splitting prisms and multiple detectors, but we believe that the IDID offers an outstandingly robust approach and that it can be applied to solve a wider range of measurement problems than other polarization imaging schemes.

OPTICAL DESIGN

The fundamental products of the IDID, besides two polarized images, A and B (which could, for example, correspond to a scene as recorded with sheet polarizers passing light in the vertical and horizontal polarizations, respectively), are difference images, $A - B$, conventional intensity images, $A + B$, and intensity-corrected polarization images, $(A - B)/(A + B)$. Images A and B are formed as shown in Fig. 2. The camera housing and image-forming lens are not different from those in other electronic cameras, of which there are many on the market. In the IDID, however, the light-sensing charged-coupled device (CCD) is bonded to a thin birefringent ("bends light two ways") wafer.

Calcite is the best known birefringent material, and Nicol used it in his original prism. The outstanding property of calcite crystals is that the angle through which they deflect light depends on the direction of the light beam and its plane of polarization relative to the crystal axes. In the IDID, the crystal axes are oriented to aim light that is linearly polarized parallel to the rows of pixels directly downward. This is called the ordinary beam. Light polarized perpendicular to the pixel rows

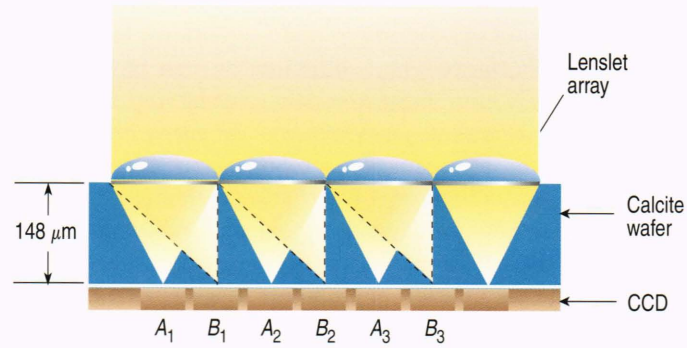

Figure 2. Optics of the IDID. An array of lenslets is cemented to a calcite wafer and aligned with the picture elements (pixels) of the CCD. Ordinary rays focus on the *A* array and extraordinary rays (dashed lines) focus on the *B* array of light-sensing elements.

is bent toward the adjacent row of pixels, as shown by the dashed lines in Fig. 2. This is called the extraordinary beam. If the thickness of the crystal is chosen just right, the deflected beam falls exactly on the next row of pixels. The bending angle β is given by the formula

$$\tan\beta = \frac{(n_o^2 - n_e^2)\tan\chi}{(n_o^2 - n_e^2)\tan^2\chi}, \qquad (1)$$

where χ is the angle that the crystal's optic axis makes with the plane normal to the wafer face, and n_o and n_e are the indices of refraction (bending) for the ordinary and extraordinary beams, respectively. To obtain the highest separation of the two beams with the thinnest possible wafer, angle χ should be 45°. Then, the angle β between the beams in calcite is 6.15°. Table 1 gives $\tan\beta$ and the indices of refraction for red light (near 610 nm) in calcite, lithium niobate, and rutile.

According to Table 1, light of the two orthogonal senses of linear polarization will fall on alternating rows of pixels, as shown in Fig. 2, when the thickness of the calcite wafer is 9.27 times the spacing between the rows. Since the pixel spacing for typical CCDs is about 16 μm, the thickness of a wafer of either calcite or rutile is only 148 μm, i.e., the beams follow different paths through only a microscopic part of the distance from the light source to the actual light sensors. In contrast, the distance to the camera lens is about 35 mm. This vital point is illustrated in Fig. 2, which shows that light of both polarizations follows only one trajectory except for the last 148 μm. Thus, alternate pixel rows see exactly the same scene through the same optics. Misalignments and other distortions will be introduced during assembly, but once the wafer is cemented to the sensor and it is calibrated in polarized light, it should be a reliable polarization imager forevermore.

Table 1. Properties of common birefringent crystals.

Material	n_o	n_e	$\tan\beta$
Calcite ($CaCO_3$)	1.654	1.485	1/9.27
Lithium niobate ($LiNbO_3$)	2.297	2.208	1/25.38
Rutile (TiO_2)	2.627	2.919	1/9.32

Note: n_o and n_e are the indices of refraction for ordinary and extraordinary beams, respectively, and β is the bending angle.

Linearly polarized light falling on the wafer divides into two beams according to the following formulas:

$$I_o = I_i \cos^2\phi \qquad (2)$$

$$I_e = I_i \sin^2\phi, \qquad (3)$$

where I_i is the intensity of the incident beam, I_o is the intensity of the beam that follows the ordinary rules of refraction, I_e is the intensity of the extraordinarily refracted beam, and ϕ is the angle that the plane of polarization makes with the plane containing the optic axis. Ignoring calibration factors for now, we see that the difference of Eqs. 2 and 3 is

$$I_o - I_e = I_i(\cos^2\phi - \sin^2\phi) = I_i \cos 2\phi. \qquad (4)$$

Dividing by the sum of Eqs. 2 and 3, we get

$$(I_o - I_e)/(I_o + I_e) \equiv (A - B)/(A + B) = \cos 2\phi. \qquad (5)$$

At each *A*,*B* pixel pair, we retrieve the stokes *Q* parameter, which is $\cos 2\phi$ for linearly polarized light.

The array of cylindrical lenses shown in Fig. 2 is aligned with the rows of pixels to focus the light on the most sensitive part of each pixel and to prevent spillover of light from adjacent pixels. The pitch of the lenslet array is exactly half that of the pixel array so that the ordinary and extraordinary rays illuminate only the *A* pixels and *B* pixels, respectively. Use of the lenslets with a calcite or rutile wafer means that there will be little spillover from the target pixels even for an *f*/2 beam. Thus, the IDID can be used in very fast cameras when a lenslet array is incorporated. A simpler scheme, with opaque strips replacing the lenslets, was used in

the prototype. It requires the *f*-number of the beam to be at least *f*/12.

Assembly of an IDID requires alignment of the cylindrical lenses with the pixels to within ≈1 μm. However, as described later, the needed precision can be achieved by using the detector, itself, to monitor the alignment.

DETECTOR DESIGN

The IDID detector is a custom-designed CCD integrated with on-chip analog circuitry that directly outputs images of scene intensity and polarization. A floor plan of IDID's detector and electronics is illustrated in Fig. 3. It consists of the detector array, a detector array termination band, a pair of high-speed serial registers, four distributed clock-driving networks, and four analog signal-processing elements. Two of the networks drive the parallel array and two drive the high-speed serial CCD. The performance objectives of the device are listed in Table 2.

CCD Fabrication

The CCD should be capable of high frame rates while maintaining high signal-to-noise ratios in the images. We plan to accomplish this by a mixture of process and architectural enhancements of standard fabrication techniques.

CCDs are fabricated by only a few vendors worldwide. It is a complex, multistep process that involves deposition of silicon and metal features down to about 1 μm in size. Fabrication of our CCD will start with a 0.01–0.02 ohm·cm *P*-type bulk silicon substrate that has a thin 15–40 ohm·cm 15-μm epitaxial layer deposited on the front surface. A deep phosphorus implant is made to define *N*-well regions where *P*-channel type metal-oxide semiconductor (PMOS) devices, which will perform the analog arithmetic, will be constructed. A standard local oxidation of silicon process defines the active areas of the device. A threshold-adjusting boron implant then sets both the *N*-type metal-oxide semiconductor (NMOS) and PMOS thresholds at 1 V. A shallow arsenic implant (buried-channel implant) is performed next to define the buried channel of the CCD. An oxide/nitride gate dielectric (300 Å/300 Å) is deposited for both the CCD and CMOS gates. The first layer of polysilicon ("poly one") is deposited, patterned, etched, and oxidized to form the barrier phases. An additional shallow arsenic implant (storage implant) is made in the regions where the first polysilicon layer has been removed to establish a fixed potential (3 V) difference between poly one and poly two CCD gates. Two more layers of polysilicon are then deposited, patterned, etched, and oxidized to form the storage phases in a two-phase or uniphase clocking method. Arsenic and boron are implanted in the silicon to define the source and drain regions for the NMOS and PMOS devices, respectively. An intermediate oxide layer is then deposited and reflowed to make the surface planar. Contact holes are etched, and a first layer of aluminum ("metal one") is deposited to form the interconnections between the various structures, followed by another oxide layer. Additional holes are etched, and the second layer of aluminum is deposited to complete the interconnections. Finally, a protective overcoat glass is deposited, and holes are etched to conductive pads to provide external access to the circuitry. This fabrication sequence closely resembles the Orbit Semiconductor Corporation's standard 2-μm double poly–double metal, *N*-well bipolar complementary MOS (BiCMOS) CCD fabrication sequence, but there are several enhancements. The enhancements are as follows:

- Addition of a third polysilicon level
- Addition of a permanent nitride cap over all gate oxide regions
- Reduction of the interpoly oxide
- Increased conductor current densities
- Buried-channel dopant changed from phosphorus to arsenic
- Modification of the buried-channel implant from a single implant to a triple implant sequence with the addition of buried-channel storage and buried-channel step implants
- Addition of a lightly doped drain (LDD)

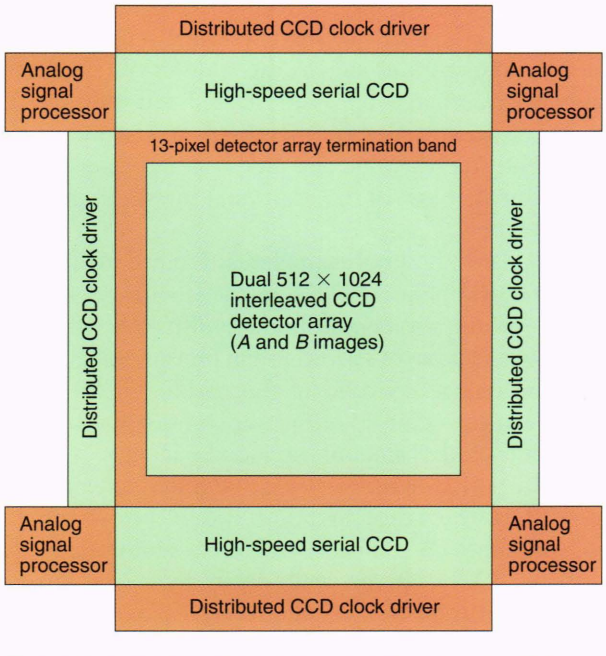

Figure 3. Floor plan of the Integrated Dual Imaging Detector (IDID).

Table 2. Electronic design objectives of the IDID.

Input:	5 V CMOS compatible
Output:	10 MHz, 50 Ω compatible ±3 V analog. Configuration should consist of four output ports, each port capable of performing the following arithmetic operations: A, B, $A + B$, $A - B$, $(A - B)/(A + B)$.
Rates:	20-MHz high-speed serial CCD register 2-MHz parallel-to-serial transfer 10-MHz analog signal processing 20-kHz parallel CCD imaging array 15 frames/s in single port mode
Imager:	$2 \times 512 \times 1024$ interleaved CCD array 1×10^6 electron storage capacity per pixel ≥70% light-collecting efficiency Front illumination Low dark current (room temperature) 10-V uniphase CCD
Serial CCD:	1.2×10^6 electron storage capacity per pixel Better than 99.9999 charge transfer efficiency 10-V uniphase CCD
Power:	10–12 W for the analog signal processing (3 W per processing unit) 4 W for CCD and associated clock drivers (1-ns clock edge rates)
Area:	≤1.25 in.^{2}

Note: CMOS = complementary metal-oxide semiconductor.

Tables 3–6 summarize the principal structural and device specifications resulting from the process enhancements.

The gate dielectric for both CCD and transistor polysilicon gates consists of an oxide/nitride dual dielectric. The thickness of the dielectric combination for poly one gates is 300 Å/400 Å, which represents the actual thickness grown or deposited. During the patterning of poly one and poly two, the thickness of the top dielectric, silicon nitride, is reduced because of the low selectivity in the etching process between polysilicon and silicon nitride. During each of the polysilicon etching steps, approximately 50 Å of silicon nitride is lost in those regions. This loss implies that the dielectric thickness under poly two will be 300 Å/350 Å and the thickness under poly three will be 300 Å/300 Å. Table 3 summarizes the poly gate specifications.

The buried-channel CCD is developed by a combination of three implants instead of a single implant. The three implants are the buried-channel implant, which is placed under all CCD poly gates; the storage implant, which is placed under poly two and poly three CCD gates; and the step implant, which cuts the poly two and poly three CCD gates as illustrated at the bottom of Fig. 4. The storage implant is used to create a fixed potential difference between poly one, poly two, and poly three CCD gates. This fixed potential defines the charge well depth (2.0 ± 0.5 V). The step implant is used to increase the high-speed charge-transfer efficiency by providing an additional field-induced drift for the electrons under poly two and poly three. The shape of the step implant also aids in the transfer of charge because of the charge crowding, called self-induced drift, that occurs at the thinner implant region. In addition, the step implant also helps to increase the charge density because of the additional threshold shift of approximately 1 V.

The standard phosphorus implants that are used to form the buried channel will be replaced with arsenic implants. Arsenic was chosen because of its low diffusion constant, a factor of 10 lower than phosphorus, and because the charge centroid of the mobile charge is localized near the centroid of the implant distribution, independent of the amount of mobile charge. The depth of the buried channel, storage, and step implants should fall in the range of 500 ± 100 Å below the $Si–SiO_2$ interface. We expect to obtain a uniform and controllable CCD charge well depth by using the buried-channel implant to define the poly one CCD gate threshold and a combination of the buried-channel, storage, and step implants to define the poly two and poly three CCD gate threshold forms. This

Table 3. Thickness of the dielectric layers.

CCD channel	Minimum (Å)	Typical (Å)	Maximum (Å)
Poly one gate[a]	275/375	300/400	325/425
Poly two gate[a]	275/325	300/350	325/375
Poly three gate[a]	275/275	300/300	325/325
Interpoly	2,000	2,200	2,400
Field oxide (all poly to substrate)	5,500	6,000	6,500
Metal one to all poly	8,000	8,500	9,000
Metal one to substrate	13,500	14,500	15,500
Metal one to metal two	7,500	8,000	8,500

[a]Poly gate is a dual dielectric of oxide and nitride (oxide thickness/nitride thickness).

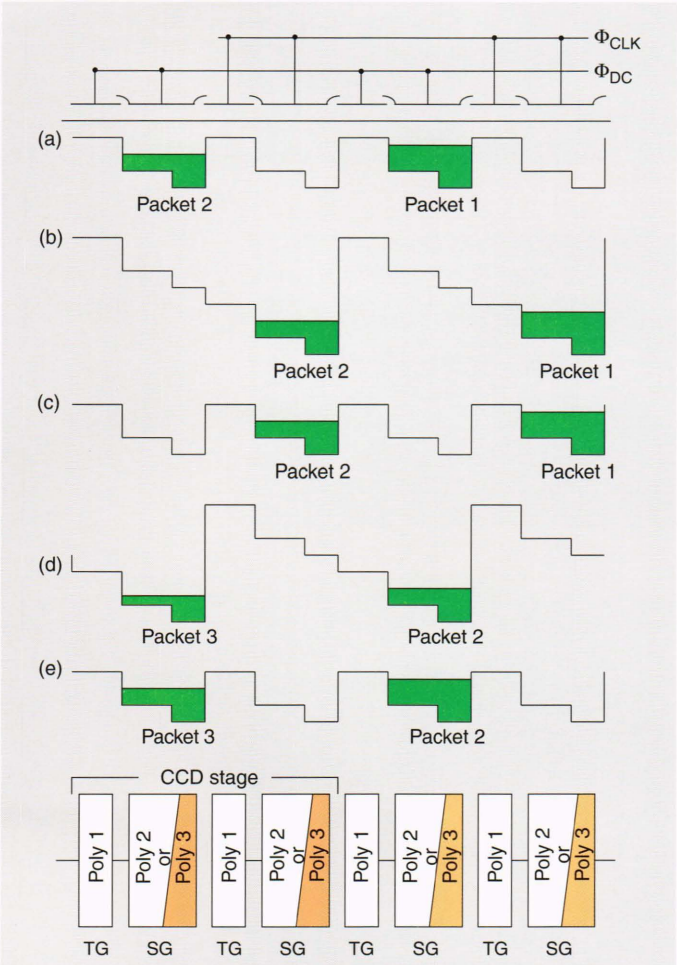

Figure 4. The uniphase CCD topology and two stages of operation. The top part of the figure shows a cross-sectional view of the charge-transfer circuitry. The middle of the figure (a–e) illustrates charge transfer using potential well diagrams. The bottom part is a view of the physical structures (TG, transfer gate; SG, storage gate); the shaded regions of the poly two/poly three gates show the location of the step implant.

approach is required to achieve the desired 20-MHz readout rate. The characteristics of the buried-channel CCD are given in Table 4.

The dielectric thickness between all polysilicon layers was chosen to minimize the poly–poly overlap capacitance, and the thickness of the metal conductor was increased to support higher current densities. This combination of enhancements will enable the CCD clock driver to drive the CCD more efficiently at high clock rates and also improve reliability and yield. A summary of the interpoly dielectric specifications is given in Table 4. The conductor specifications are given in Table 5.

The LDD processing feature has been added to allow the implementation of high-voltage analog and digital CMOS circuitry. This feature is important because it facilitates the integration of the high-speed clocking and analog signal processing with the CCD function. The LDD increases the effective resistance to drain of the NMOS devices and, thus, should prevent avalanche breakdown. In addition, the gate lengths of both the NMOS and PMOS devices are increased to improve the punch-through potential. This potential is defined as the drain-source differential voltage required to cause uncontrollable current flow between the drain and source. Table 6 contains the device characteristics for both *N*- and *P*-channel high-voltage poly transistors.

Function of the Uniphase Buried-Channel CCD Architecture

We chose a uniphase buried-channel CCD architecture because of its ability to operate at extremely high clock rates (50–100 MHz for a 10-μm storage gate length) while maintaining reasonable charge transfer efficiency (CTE) of 99.99%.[2] As a result of the reduc-

tion in the self-induced field, CTE tends to degrade in low-light operation, when the charge packets are small. The addition of the step implant across the storage gate, shown in Fig. 4, will increase the low-light CTE by confining the charge packets to a smaller portion of the storage gate nearer the edge closest to the transfer direction.

Each pixel where photoelectrons are collected is actually composed of four gates: two poly one gates, known as transfer gates (TGs), and two poly two or poly three gates, known as storage gates (SGs). The uniphase CCD architecture has adjacent poly one/poly two (poly three) gates connected together through one of the common busses Φ_{DC} or Φ_{CLK}. As indicated by their names, Φ_{DC} is typically attached to a DC potential and Φ_{CLK} is typically attached to a clock driver. Because of the two controls required for the uniphase CCD architecture, it is often referred to as a two-phase architecture. With the uniphase CCD architecture, pixel element isolation is achieved naturally under all biasing conditions as long as the channel remains depleted.

Operation of a uniphase two-stage CCD is illustrated in Fig. 4. The potential well diagram of Fig. 4a has $\Phi_{CLK} = \Phi_{DC}$, with two charge packets located under the Φ_{DC} SGs. Figure 4b has $\Phi_{CLK} > \Phi_{DC}$, and the potential well under the Φ_{CLK} transfer/storage gate (TG/SG) pairs is lowered. This allows the charge under the Φ_{DC} SGs to move into the well under the Φ_{CLK} SGs. In Fig. 4c, $\Phi_{CLK} = \Phi_{DC}$, and the charge packets have moved 1/2 stage to the right. Figure 4d has $\Phi_{CLK} < \Phi_{DC}$, and the

Table 4. CCD channel voltages.

CCD channel	Minimum (V)	Typical (V)	Maximum (V)
Poly one CCD gates	3.0	3.5	4.0
Poly two CCD gates[a]	5.5	6.5	7.5

[a]A second implant, the storage implant, is done under all poly two CCD gates to establish a charge well capacity of 2.5–3.5 V.

Table 5. Conductor thicknesses.

Conductor	Minimum (Å)	Typical (Å)	Maximum (Å)	Density (mA/μm)
Poly one	3,700	4,000	4,300	—
Poly two	3,700	4,000	4,300	—
Metal one	7,500	8,000	8,500	0.50–0.75
Metal two	10,500	11,500	12,500	0.75–1.00

Note: Dashes denote data are not available.

Table 6. Characteristics of high-voltage *N*- and *P*-channel devices.

Transistor	Minimum	Typical	Maximum
N-Channel transistor			
Threshold (V)	1.0	0.75	0.5
Kappa = $\mu C_{ox}/2$ ($\mu A/V^2$)[a]	8.9	9.6	10.5
Punch-through (V)†	15.0	17.5	20.0
Delta length (μm)	−0.75	−0.50	−0.25
P-Channel transistor			
Threshold (V)	−1.0	−0.75	−0.5
Kappa = $\mu C_{ox}/2$ ($\mu A/V^2$)[a]	8.9	9.6	10.5
Punch-through (V)[b]	−20.0	−17.5	−15.0
Delta length (μm)	−0.75	−0.50	−0.25

[a]Kappa is determined with drain-to-source voltage = 0.1 V and gate-to-source voltage = 2 V or 3 V.
[b]Punch-through is determined for a 3-μm gate length device.

potential under the Φ_{CLK} TG/SG pairs is raised. This allows the charge under the Φ_{CLK} SGs to move into the potential well under the Φ_{DC} SGs. Returning to $\Phi_{CLK} = \Phi_{DC}$, as in Fig. 4e, completes the movement of each charge packet by one stage to the right.

When the sensor is exposed to light, Φ_{CLK} electrodes are biased to a potential that is lower than that of the Φ_{DC} electrodes but that maintains the channel region in depletion so that charge collection may occur. This increases the photosensitive area along the direction of the CCD channel to 100% and uses the channel under the Φ_{DC} SG electrodes as the collection centers. The modified uniphase CCD potential profile is illustrated by the potential well diagrams at the top of Fig. 5.

Photons that strike the imager in or about the CCD channel region are converted into electron-hole pairs. The electrons located within the domain of a given pixel are collected and stored under that pixel's Φ_{DC} SG electrodes. Electrons located under the Φ_{CLK} TG electrodes have a high probability of being collected by one of two pixels.

As the electrons accumulate in the channel under the Φ_{DC} SG electrodes, the potential well begins to fill. When the height of the accumulated electrons reaches the barrier height set by the Φ_{DC} TG electrodes, the pixel charge well is full and any excess charge is shared with neighboring pixels after the integration process. This is an undesirable effect that would have been eliminated by the inclusion of an antiblooming structure. Since such a structure has not been included, antiblooming can be controlled only by controlling the photon flux allowed to strike the photosensitive areas.

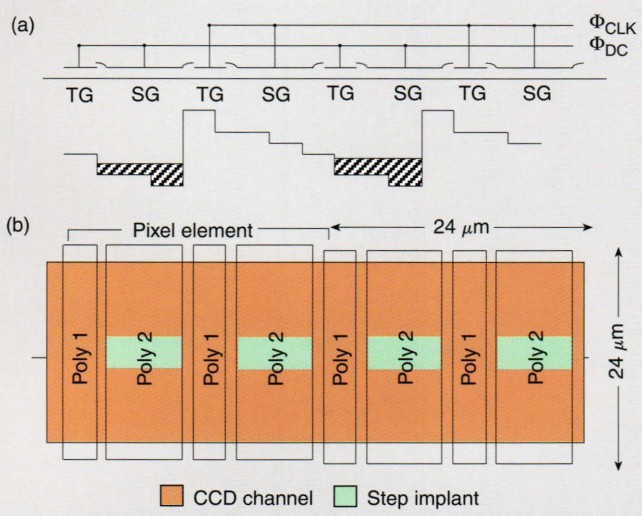

Figure 5. Two stages of the modified uniphase buried-channel CCD architecture and associated potential well diagrams for the pixel element. (a) The upper potential well diagram illustrates a horizontal cross-sectional view (TG, transfer gate; SG, storage gate). (b) The lower potential well diagram illustrates a vertical cross-sectional view through the antiblooming drain.

Device Characteristics

Photosensitive Area

The design of the pixel element optimizes the photosensitive area by allowing both Φ_{DC} and Φ_{CLK} to be biased so that the entire CCD channel region is depleted. This enables the entire CCD channel to participate in the photon conversion process. The exclusion of an antiblooming structure allows the width of the CCD channel to be 21 μm of the 24-μm pitch, which leads to an area efficiency of 87.5%. The penalty for devoting such a large percentage of the pixel to photon conversion is the inability to control blooming from one pixel to another automatically. Further improvement in the processing to include a vertical antiblooming structure (Fig. 5) will circumvent this problem while not affecting the percentage of the pixel that is photosensitive.

Quantum Efficiency

The process on which this device is based has not yet been run; therefore, quantum efficiency data are not available. The quantum efficiency may be approximated by use of the following process and operational parameters:

- The IDID is a front-side illuminated imager.
- The approximate thickness of all polysilicon layers is 3000 Å.
- The approximate thickness of the boron phosphate silica glass protective oxide is 8000 Å.
- The starting epitaxial thickness is 15 μm.
- The epitaxial resistivity is 15–40 Ω·cm.

The characteristic peak quantum efficiency for devices of this type is 20–30% over a spectral range of 500–900 nm.

Charge Capacity

The fabrication process has been optimized to achieve the highest possible charge capacity while maintaining buried-channel operation. The combination of the shallow arsenic buried-channel implants (500–1000 Å) and the thin oxide/nitride dual dielectric will produce a channel charge capacity density of approximately 3375 electrons $V^{-1}\cdot\mu m^{-2}$ for poly two storage gates and 3500 electrons $V^{-1}\cdot\mu m^{-2}$ for poly three storage gates. The difference between the charge capacities is a result of the silicon nitride reduction caused by the etching of poly one and poly two.

To maximize the charge capacity, we will use poly three storage gates in the implementation of the photosensitive pixels. If we assume that the step implant is 4 μm wide and has a 0.5-V potential, the storage implant has a 2-V potential, and the storage gate area

is 7.5 × 21 μm, the full-well charge capacity of the pixel element is 1.155 × 10^6 electrons.

Dark Current

The intrinsic dark current performance of this device at room temperature should be 1–5 nA/cm^2, which corresponds to 36,000–18,0000 electrons per pixel per second. This implies that 6.5–32 s will be required for the dark current to completely fill an empty well. Alternatively, it means that in 1/30th s, the dark current will be roughly equal to the shot noise for wells nearly filled to saturation.

The addition of the integrated clock driver and analog signal-processing circuits will increase the dark current. Depending upon the objective, the device may have to be cooled in order to achieve adequate dark current performance. The exact temperature required to meet the device performance specifications will depend on the power dissipation.

Charge Transfer Efficiency

The CTE of buried-channel CCD devices with this pixel element pitch have been reported at 99.999.[1,2] Inclusion of the step implant to aid in the low-signal self-induced transfer should improve the transfer efficiency.

Noise

The minimum charge capacity noise performance is set by the goal of being able to image a 10-lux (4 × 10^4 photons $s^{-1} \cdot \mu m^{-2}$) signal over a 200-μs integration time. If we assume that the CCD channel dimensions of a pixel element are 21 × 24 μm, the total number of photons that may strike the CCD is approximately 2900 photons. The number of photons that reach the CCD channel, as determined by the quantum efficiency, is approximately 725 photons. This establishes the minimum charge capacity upper noise limit.

Several sources of noise must be considered. These are transfer noise, photon noise, dark current, amplifier noise, and bulk trapping noise. The estimated values of the various noise sources are listed in Table 7, which assumes a maximum of 2130 transfers, 2 transfers per pixel or horizontal element, and 525 pixel and 540 horizontal elements in the transfer path. Results are also shown for electron densities of 1.155 × 10^6 and 725 electrons, which correspond to the full-well and

Table 7. Noise sources under various conditions.

Noise source	Variable	Value (no. of electrons)	Condition
Transfer	N_T(rms)	318	Full well and CTE of 99.999%
		4	Minimum and CTE of 99.999%
Photon	N_P(rms)	1074	Full well
		27	Minimum
Dark current	N_D(rms)	55	20-MHz clock, 200-μs integration time, 5 × 10^{-17} A/μm^2, 32,000 charge packets
Bulk	N_B(rms)	3	Bulk trap density of 2 × 10^{-6} (Ref. 6), 300 K
Amplifier	N_A(rms)	8	Full bandwidth input referred noise 60 μV, sensitivity of 1 μV/electron
Total	N_T(rms)	1122	For full well, including photon noise
		323	For full well, excluding photon noise
		62	For minimum capacity, including photon noise
		56	For minimum capacity, excluding photon noise

Note: rms = root mean square; CTE = charge transfer efficiency.

minimum charge capacities, respectively. Listed at the bottom of Table 7 is the total noise under several conditions. For full-well charge capacity, the total noise is dominated by photon noise, N_T (rms) = 1122 electrons. If photon noise is ignored, the dominant noise source is transfer noise, N_T (rms) = 323 electrons. For minimum charge capacity, the noise is dominated by both photon and dark current noise, N_T (rms) = 62 electrons. If photon noise is ignored, the total noise is N_T (rms) = 56 electrons.

Dynamic Range

The dynamic range is defined as the signal-to-noise ratio. The signal is defined as the full-well charge capacity, and the noise is defined by the total full-well rms noise. Ignoring photon noise, the dynamic range is 71 dB.

Resolution and Contrast

Spatial resolution of an image sensor is defined as the sensor's ability to discriminate between closely spaced points in the image. The target resolution for this system is 25 cycles/mm with 20% contrast. If the minimum observable picture feature is 4 times the pixel element spacing (24 μm) and the only noise source is photon noise, the low-light (10 lux with an average quantum efficiency of 25%, ideal optical elements) resolution of this device is approximately 26.85 cycles/mm at 20% contrast. If we include additional noise sources, the device resolution is degraded to 16.21 cycles/mm, which is dominated by dark current. This dependence on the dark current may be reduced if the device is cooled. Complete elimination of dark current would yield a resolution of 24.43 cycles/mm for low light levels. In most applications, solar research, for example, the light levels will be far higher than 10 lux and the detector will easily achieve the targeted resolution.

High-Speed Serial CCD

Like the detector array, the high-speed serial CCD is a modular design. The module width is constrained to the same width as the detector array module. Figure 6 illustrates the basic components of a single high-speed serial CCD module. The module contains an array of horizontal charge transfer elements, denoted as "Serial CCD," a pair of floating gate outputs, and a parallel-to-serial interface.

Horizontal Elements

These elements are used to transfer the image from the detector array to one of the two image de-interleaving circuits. Like the pixel element, the design of the horizontal element is based on the uniphase buried-channel CCD architecture, which optimizes the CTE and speed while limiting artifacts caused by signal charge interaction with surface trapping mechanisms. Optically, the horizontal elements will have an opaque covering to eliminate the photosensitive response. The CCD architecture of the horizontal element, along with its corresponding parallel-to-serial transfer interface, is illustrated in Fig. 7.

The location of the gates is critical to the operation of the element during the parallel-to-serial charge transfer. Both the Φ_{DC} and Φ_{CLK} TGs are located along the horizontal CCD channel, with the Φ_{DC} SG centered about the parallel channel. During the parallel-to-serial transfer, the charge is restricted to the channel region under the Φ_{DC} SG by biasing Φ_{CLK} off with respect to Φ_{DC} ($\Phi_{DC} > \Phi_{CLK}$), as illustrated by the potential well diagram in Fig. 7.

During horizontal charge transfer, the serial-to-parallel transfer gate, Φ_{PS}, is biased off with respect to Φ_{DC} ($\Phi_{DC} > \Phi_{PS}$). The horizontal charge transfer is similar to that described in the section on uniphase buried-channel CCD operation.

The dimensions of the horizontal element were chosen to make the length of the horizontal element

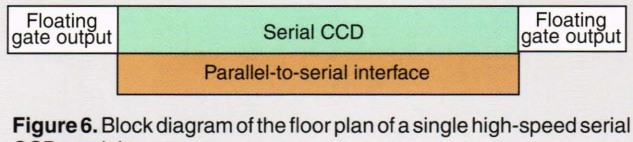

Figure 6. Block diagram of the floor plan of a single high-speed serial CCD module.

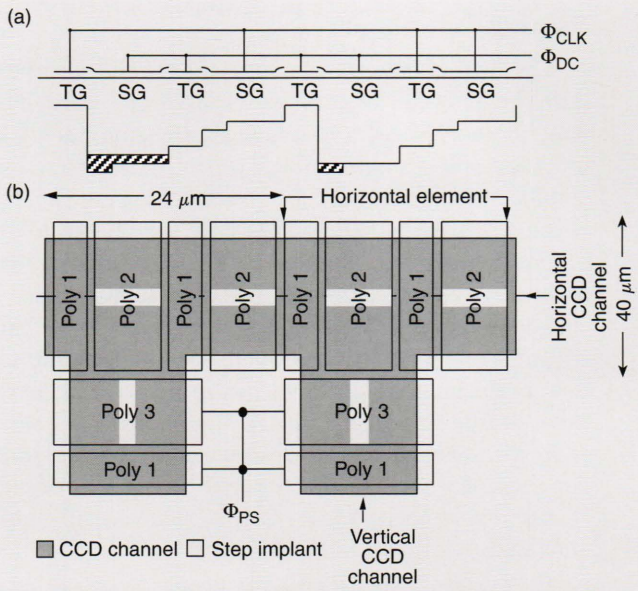

Figure 7. Two stages of the uniphase buried-channel CCD architecture (b) and associated potential well diagram for the horizontal element (a) (TG, transfer gate; SG, storage gate). The potential well diagram illustrates the channel potential during parallel-to-serial charge transfer, $\Phi_{DC} > \Phi_{CLK}$. Also included in the architecture is the parallel-to-serial transfer gate Φ_{PS}.

equal to the width of the pixel element, since each row of pixel elements must mate to a single horizontal element, thus establishing the width of 24 μm. In addition, the width of the horizontal element was chosen so that the highest possible CTE is maintained during high-speed clocking of the serial CCD. This usually dictates that the charge capacity of the horizontal element should exceed that of the pixel element by 50–75%, corresponding to a horizontal width ranging from 30 to 45 μm. As indicated by Fig. 7, 40 μm has been selected.

Charge Capacity

As mentioned, poly three was used for implementation of the pixel element storage gate, which leaves poly two for implementation of the storage gates of the horizontal elements. Also mentioned was the storage capacity of 3375 electrons $V^{-1} \cdot \mu m^{-2}$ for poly two storage gates. If we assume that the step implant is 4 μm wide and has a 0.5-V potential, the storage implant has a 2-V potential, and the storage gate area is 7.5×40 μm, the full-well charge capacity of the pixel element is 2.0×10^6 electrons.

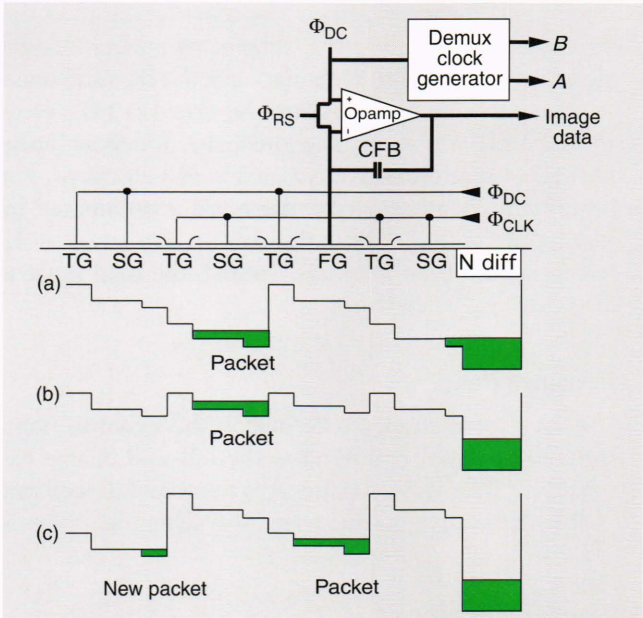

Figure 8. Illustration of the floating gate output architecture along with potential well diagrams (a–c) showing the channel potential during the various phases of the charge-to-voltage conversion (TG, transfer gate; SG, storage gate; CFB, feedback capacitor).

Dark Current

The intrinsic dark current performance of this device should range from 1 to 5 nA/cm^2, which corresponds to 68,600–342,900 electrons per pixel per second. This implies that 3.4–16.8 s will be required for the dark current to completely fill an empty well.

Floating Gate Output

The final charge transfer element of the high-speed serial CCD is the floating gate output structure. This structure consists of a uniphase buried-channel CCD, precision operational amplifier (opamp), capacitor, and demux clock generator, as illustrated in Fig. 8. The uniphase CCD is used to transport the charge to the output floating gate, denoted as (FG). Operation of the floating gate is described in the next subsection.

The demux clock generator is responsible for generating strobe pulses that activate the input sample and hold in the analog signal-processing element. On every other pulse of the Φ_{CLK}, the *A* output strobe is pulsed to store the image data in the *A* input sample and hold. For those Φ_{CLK} where the *A* output is not strobed, the *B* output is strobed, storing data in the *B* input sample and hold.

Charge-to-Voltage Conversion

Charge-to-voltage conversion is implemented by means of a pinned floating gate. The conversion is accomplished by connecting the negative terminal of an opamp to the floating gate, the positive terminal to Φ_{DC}, and a reset transistor or switch across the inputs and adding a negative feedback capacitor (CFB). When $\Phi_{CLK} > \Phi_{DC}$, the reset transistor is on, biasing the floating gate to the potential Φ_{DC}. The channel potential and charge packet location are illustrated by the potential well diagram of Fig. 8a.

As the potential on Φ_{CLK} is reduced so that $\Phi_{CLK} = \Phi_{DC}$, the reset transistor is turned off, disconnecting the floating gate and the negative terminal of the opamp from Φ_{DC}. This results in a slight change in the channel potential from its reset level, as illustrated by the potential well diagram of Fig. 8b.

As the potential on Φ_{CLK} is reduced even more so that $\Phi_{CLK} < \Phi_{DC}$, the charge packet is injected into the channel region under the floating gate. This injection of charge attempts to reduce the voltage on the negative terminal of the opamp, causing the output of the opamp to increase. The increase in the opamp output is proportional to the ratio of the sum of the floating gate and opamp input capacitances, and the feedback capacitor CFB. The net result of the circuit is to fix the channel potential so that each electron in the packet is measured across the same net capacitance (i.e., a linear charge-to-voltage conversion). The potential well diagram in Fig. 8c illustrates the channel potentials during charge conversion.

There are three drawbacks to this method of charge-to-voltage conversion: (1) higher power as a result of the offset voltage of the opamp, (2) higher fixed offset as a result of the offset voltage of the opamp, and (3)

possibly higher noise. The voltage offset may be reduced significantly by using a dual opamp topology in which one opamp provides the offset correction term for the other. This method will be effective as long as the input devices of both opamps are close. The specifications for such an opamp architecture are described later.

The sensitivity of the conversion process is programmable by adjusting the feedback capacitor CFB. A maximum sensitivity of 3–4 μV/electron is possible. Further increases in the sensitivity would result in the introduction of nonlinearities because of the limited input range of the opamp.

Precision Opamp

The precision opamp is an offset canceling design that uses two high-gain opamps, one to provide gain and the other to provide offset correction. The basic opamp is a modified cascade design, which was used in the IDID project. The device specifications for the IDID precision opamp are listed in Table 8.

Analog Signal-Processing Element

The output of the floating gate amplifier is coupled into the analog signal-processing element, which generates a 50-Ω compatible analog data stream. A functional block diagram of the analog signal-processing element is shown in Fig. 9.

Each analog processing element is made up of two 50-Ω drivers for generating the analog data stream, an analog multiplexer, analog sample and holds, unity gain buffers, and five arithmetic operators. The arithmetic operations available are A, B, $A + B$, $A - B$, and $(A - B)/(A + B)$. Operations A and B are implemented in the charge domain, whereas the other operations are implemented in the voltage domain. Both the A and B operators are available simultaneously from either of a pair of sample-and-hold devices that buffer the floating gate output. Similarly, the $A + B$ and $A - B$ operators are available simultaneously from a pair of sample-and-hold devices that buffer two precision opamps configured to implement addition and subtraction. The $(A - B)/(A + B)$ operator is available from a sample-and-hold device that buffers a precision opamp with an analog multiplier in its feedback loop. The analog multiplexer is used to select one of five set outputs: A, B, $A + B$, $A - B$, and $(A - B)/(A + B)$.

Sample and Hold

An internal sample-and-hold circuit is used to extend the sampling period to the period of the high-speed serial CCD clock Φ_{CLK}. This circuit is based on an edge-triggered double sampling design.

Low-Impedance Output Driver

The low-impedance output driver was designed to provide reasonable drive at high frequencies into either a resistive or capacitive load. This device is designed to drive either a 500-Ω load or a 5-pF capacitance in excess of 50 MHz with a ±2 V output swing. The

Table 8. Performance specifications for IDID precision opamps.

Supply voltages	5 V, analog ground
	0 V, negative supply
	10 V, positive supply
	−5 V, substrate supply
Power	140 mW
Output load	4 pF
Output swing	±4 V about analog ground
Common mode input range	±4 V
Open loop gain	>75 dB
Offset voltage	≤1 mV
Slew rate	400 V/μs
Settling time	≤45 ns for 12 bits (relative to final output)
Unity gain bandwidth	≥45 MHz
Noise	≤60 μV (integrated noise over unity gain bandwidth)
Phase margin	45–60
Temperature	0–70°C
Technology	Orbit Semiconductor 2-μm *N*-well CCD BiCMOS

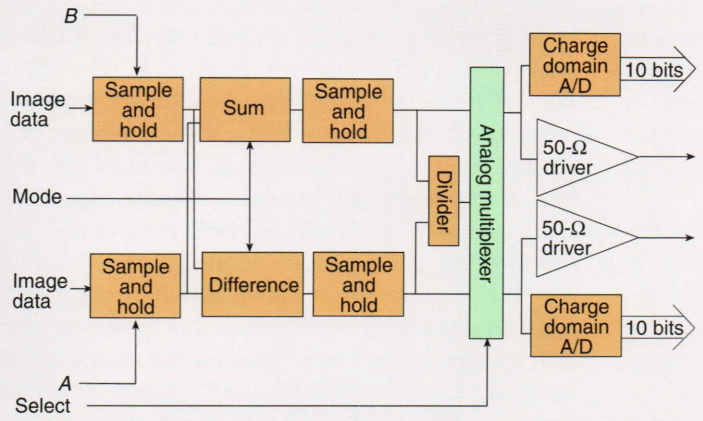

Figure 9. Functional block diagram of the analog signal-processing element.

performance specifications of the 50-Ω driver are given in Table 9.

CCD Clock Driver

The CCD clock driver is used to provide a standard user interface to clock the CCD. A block diagram of the clock driver is given in Fig. 10. It consists of two basic elements, a variable voltage translator and a cascadable CCD clock driver. The variable voltage logic translator is used to convert from CMOS input clock voltage levels to CCD clock voltage levels. The cascadable CCD clock drivers are used to provide power to drive the CCD load capacitance. The output CCD clock voltage is varied by adjusting the power supply voltages. The performance specifications of the cascadable CCD clock driver and the variable voltage logic translator are listed in Tables 10 and 11, respectively.

Distributed CCD Clock Driver and Serial Register

The architecture of the distributed CCD clock drivers that will be used to drive the detector array is the same as that for the CCD clock driver described in the previous section. A serial register and associated clock circuitry reads out the entire *A* and *B* image array in 27.2 ms. The vertical clock signals shift full rows of the stored charges into the serial shift register at 25.6 μs per row, and horizontal clock signals shift these charges to the output port at 50 ns per pixel pair. Each consists of an *A* and a *B* pixel, and the output port presents both pixels simultaneously. The clock drivers are on the chip.

On-Chip Analog Arithmetic

The block diagram in Fig. 7 shows how the *A*- and *B*-pixel charges pass through analog circuitry that computes $A - B$, $A + B$, and $(A - B)/(A + B)$ on a pixel-by-pixel basis. This gives the user immediate access to the arithmetic results, each at 10 million pixels/s. Traditional analog techniques are used to form the

Table 9. Performance specifications for IDID 50-Ω drivers.

Supply voltages	5 V, analog ground
	0 V, negative supply
	10 V, positive supply
	−5 V, substrate supply
Standby power	450 mW
Output load	50 Ω
Output swing	±3 V about analog ground
Common mode input range	±3 V
Open loop gain	>75 dB
Offset voltage	≤1 mV
Slew rate	2 V/ns
Settling time	≤45 ns for 12 bits (relative to final output)
Gain bandwidth product	≥100 MHz
Noise	≤60 μV (integrated noise over unity gain bandwidth)
Phase margin	45–60
Temperature	0–70°C
Technology	Orbit Semiconductor 2-μm *N*-well CCD BiCMOS

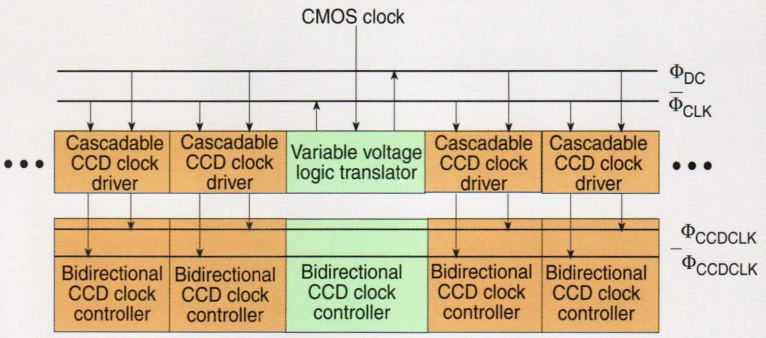

Figure 10. Functional block diagram of the CCD clock driver.

quotient, whereas the sum and difference signals are processed in the charge domain. The charge domain technique yields a data precision of 2 parts in 10^5 or better as a result of the following features:

1. The CCD is of the buried-channel type, which is characterized by ultra-low trapping densities and a transfer noise of ~10 electrons rms when cooled to −50°C or below.[3,4]
2. A thinned epitaxial substrate is used. It yields superior dark current performance (10 pA/cm^2) when the chip is cooled to −40°C or below. The transfer efficiency should be high (0.999995).[4]
3. The arithmetic and analog-to-digital architectures are ultra-small CCD structures that minimize the number of transfers.

Two digital and two 50-Ω analog output channels are available per port. The analog-to-digital conversion is based on a compact, high-speed (20 megapixels/s) pipelined charge-domain circuit with 10-bit accuracy. An analog multiplexer drives the individual output circuits with the respective results from the signal-processing functions. There are four sets of output ports to avoid crippling the device in case of a failure in an output port.

The choice of whether to use the analog or digital output channels in a particular application will depend on the desired precision. For many measurements, 10-bit precision will be adequate and the digitized signals can be used directly. Quantum efficiency differences between adjacent A and B pixels may actually limit the precision to ≈1% in such cases. For higher precision applications, the $A - B$, $A + B$, and $(A - B)/(A + B)$ analog signals can be digitized externally at 12- to 16-bit resolution and the results corrected for quantum efficiency variations by reference to a look-up table. This "gain table" can be obtained anytime by illuminating the IDID with spatially uniform unpolarized light. We expect that the gain corrections will be quite stable since the polarimetric precision will depend (aside from photon statistical noise) only on the ratios g_A/g_B of the gains of the pixel pairs. Since the light reaching each pixel in an A,B pair will follow one optical path before entering the IDID, the usual sources that make gain tables unstable (e.g., flexure in the apparatus, dust particles) will affect the signal levels in A and B in the same proportion, and they will cancel out of the ratios.

ASSEMBLY AND TESTS OF THE IDID PROTOTYPE

Detailed design of the IDID began in 1992 and is nearly complete. We await an opportunity to fabricate a batch of IDID chips. So far, we have tested a small experimental CCD chip to test a range of process parameters and charge collection cell designs. We have also tested shift-register, analog arithmetic, and analog-to-digital conversion circuitry. We fabricated a number of rutile wafers with chromium masks, and we bonded

Table 10. Performance specifications of the cascadable CCD clock driver.

Supply voltages	0 V, negative supply
	5–12 V, positive supply
	−5 V, substrate supply
Power	350 mW at 100 MHz
Output load	40 pF
Output swing	5–12 V
Temperature	−50–125°C
Technology	Orbit Semiconductor 2-μm N-well CCD BiCMOS

Table 11. Performance specifications of the variable voltage logic translator.

Input	CMOS
Supply voltages	0 V, negative supply
	5–12 V, positive supply
	−5 V, substrate supply
Power	400 mW at 100 MHz
Output load	40 pF
Output swing	5–12 V
Temperature	−50–125°C
Technology	Orbit Semiconductor 2-μm *N*-well CCD BiCMOS

one to a commercial CCD to produce a functional prototype.

Assembly

The IDID prototype chip consists of a rutile wafer (TiO_2) that is 150 mm thick and 2.6 mm in diameter bonded to the face of a small, conventional CCD. It is controlled by an IBM 386 personal computer with a plug-in board provided by the Electrim Corporation. It achieves a frame rate of 10 Hz when exposure time is 100 ms. The pitch of the pixels is 16 μm. Instead of an array of cylindrical lenslets as planned for the standard IDID, illustrated in Fig. 2, we used a Ronchi ruling cemented to the face of the wafer. The ruling provides an inexpensive way to mask light from the *B* pixels so that the illumination from the extraordinary beams will not be mixed with illumination from the ordinary beams. There is a loss in light of a factor of 2, but otherwise the arrangement allows us to test the optical principles and to develop assembly techniques. Figure 11 shows a view of the Ronchi ruling through the wafer. The photomicrograph was taken in polarized light. It reveals a 5% overlap between the two images of the transparent parts of the ruling. This overlap can be eliminated in later assemblies, and it can be calibrated out in the prototype.

Alignment of the ruling and the pixel rows to within about 1 μm presented a challenging task. We have a precision motion platform whose rotation is controllable to 0.1°. This is adequate, but the translational motion control has an accuracy of only 100 μm in two axes. To overcome the seemingly unbridgeable gap between the needed positioning precision and the available capability, we used the IDID, itself, to monitor the alignment of the ruling. First, we mounted an unpolarized point-like light source 2 m above the assembly area. We removed the lens from the camera, which allowed an effectively collimated light beam to strike the CCD so that the opaque rulings cast linear shadows on the pixel rows. Rotational misalignment produced a strong moiré pattern in the image, which was displayed in real time. We operated the CCD in a dark room (except for the point of light). Alignment was basically by the trial-and-error method. Experience showed that about 100 trials is sufficient to achieve satisfactory alignment.

During alignment, the wafer was floating on the 196 × 165 pixel array of the CCD in a thin layer of optical cement, which solidifies on exposure to ultraviolet light. After many trials, the virtual disappearance of the moiré pattern signaled near-perfect alignment. The assembly was made permanent by exposing it to ultraviolet light.

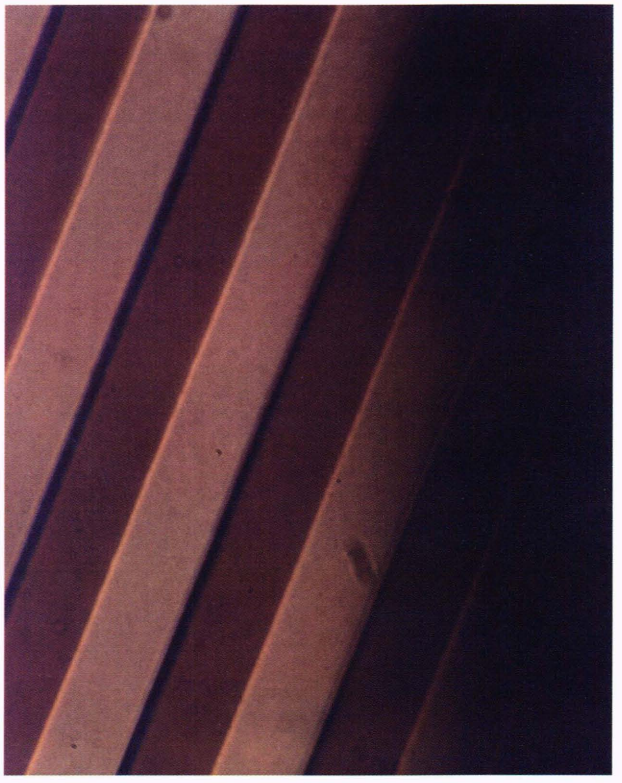

Figure 11. View of the Ronchi ruling through the wafer.

Calibration

We calibrated the IDID with light linearly polarized by a sheet polarizer placed in front of the camera. A white, flat cardboard panel was uniformly illuminated with white light. A series of identical exposures was obtained for use in constructing a map of the relative pixel gains. Raw 8-bit image data were transferred from the personal computer to a mainframe computer and processed with the Interactive Data Language. A map of the relative pixel sensitivities ("gain map") shows little pixel-to-pixel variation for the central 128 × 100 pixels of the image array. The gain map was obtained by averaging 16 frames of the uniform scene without the polarizer. At room temperature, the dark current typically averages 25 counts out of a total of 255. This is much worse than projected for the final IDID.

To calibrate the response to polarized light, we rotated the polarizer in 10° steps and recorded the intensity variation on each pixel. We corrected for dark current and computed the polarization images $(A - B)/(A + B)$, which represent images of the Stokes parameter Q. For linearly polarized light, a perfect instrument would give $Q = \cos 2\phi$, as shown in Eq. 5.

Figure 12 shows the experimental data and their cosine envelope. The average Q values of the central 128 × 100 pixels reproduce the equation except for a magnitude reduction of a factor of 2. We think this loss of efficiency is a result of the relatively large f-number ($f/8$) used, which possibly leads to some beam spilling onto the wrong pixels. As for the 4° phase shift in ϕ, it simply reveals the unleveled camera relative to the true horizontal orientation. The curve shown in Fig. 12 can be used to find the true Stokes Q parameter in applications.

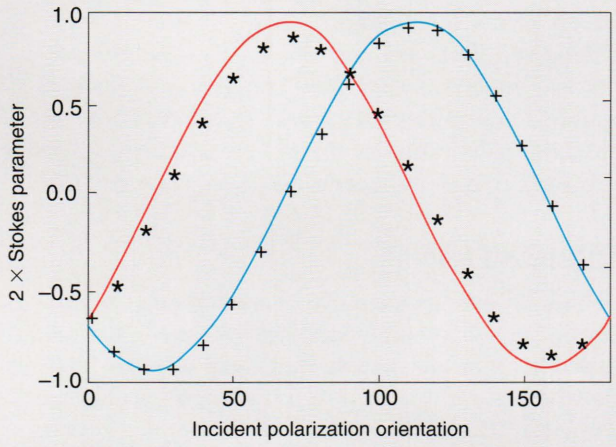

Figure 12. Comparison of the experimental data and theoretical response curves for the Stokes parameters Q and U plotted against the orientation of incident polarized light for two settings of the liquid crystal retarder, $\delta = 0$ (+) and $\delta = 180$ (∗). The actual signals have been multiplied by 2 to account for inefficiencies in the IDID prototype.

Generally speaking, Q represents the degree of linear polarization in the horizontal direction (for $Q = 1$) in contrast with the vertical direction (for $Q = -1$). Other Q values represent polarization states in between. There are possible ambiguities without additional measurements. For example, $Q = 0$ can be interpreted as linearly polarized light in the orientations of ±45°, or unpolarized light, or circularly polarized light. Nevertheless, Q provides enough information for many applications.

The IDID can rapidly record all four Stokes parameters when a liquid crystal retarder is mounted in front of the camera lens and its operation synchronized with the camera's frame-grabbing rate. Three exposures are sufficient to fully determine all the Stokes parameters. They correspond to three phase retardances ($\delta = 0, 90°$, and 180°) for light passing through the liquid crystal. Four images corresponding to the four Stokes parameters (I, Q, U, and V) can be produced from such measurements for any given scene. The Stokes parameters correspond to intensity (I), linear polarization along horizontal and vertical axes (Q), linear polarization along axes at ±45° to the horizontal (U), and circular polarization (V). Here we just present the preliminary calibration curves for Stokes Q and U with the liquid crystal retarder set to 0° and 180°, respectively (Fig. 12).

In the experimental setup, the fast axis and the slow axis of the liquid crystal retarder were aligned along the x axis and the y axis, respectively. The pixel rows in the IDID chip make a 22.5° angle to the x axis, so the A and B pixels receive the rays as shown in Fig. 2. For the polarized incident light to the IDID, the electric vector is given by

$$\mathbf{E} = a\cos\omega t \cdot \mathbf{i} + b\cos(\omega t + \delta)\cdot \mathbf{j}, \tag{6}$$

where a and b are the projections on the axes. According to Malus' law, the intensity received by an analyzer whose axes are at an arbitrary angle from the x axis is

$$I(\theta) = \frac{1}{4}(a^2 + b^2) + \frac{1}{4}(a^2 - b^2)\cos 2\theta + \frac{1}{2}ab\cos\delta\sin 2\theta. \tag{7}$$

Substituting $\theta_A = 22.5°$ and $\theta_B = 90° + 22.5°$ into θ for the corresponding A and B components, we obtain

$$A = \frac{1}{4}(a^2 + b^2) + \frac{1}{\sqrt{2}}\left[\frac{1}{4}(a^2 - b^2) + \frac{1}{2}ab\cos\delta\right], \tag{8}$$

$$B = \frac{1}{4}(a^2 + b^2) - \frac{1}{\sqrt{2}}\left[\frac{1}{4}(a^2 - b^2) + \frac{1}{2}ab\cos\delta\right]. \quad (9)$$

In the tests, the linear polarizer was rotated from the y axis to produce the magnitudes

$$a = -I_i \sin\phi, \quad (10)$$

$$b = -I_i \cos\phi. \quad (11)$$

The phase δ was set by applying the appropriate voltage to the liquid crystal retarder. If we insert a, b, and δ into Eqs. 10 and 11, we have

$$\frac{A - B}{A + B} = (-)\frac{1}{\sqrt{2}}[\cos 2\phi + \cos\delta \sin 2\phi], \quad (12)$$

which is the Stokes parameter Q in the present frame of the IDID when $\delta = 0°$, and U when $\delta = 180°$.

A liquid crystal retarder from Meadowlark Optics was used in our experiment. Curves of Q and U (without the gain map correction) were obtained for retardances $\delta = 0°$ and 180°. They are shown in Fig. 12, with the theoretical curves as their corresponding envelopes. The IDID reproduces Eq. 12 correctly but, again, there is a reduction in the amplitude of the signal. We attribute this to small misalignments in the present device. Their effect can be removed in calibration.

FIELD EXPERIMENT

A software package called POLCAM is being developed at APL for automated polarization image acquisition and processing as well as real-time display and visualization (i.e., mapping polarization parameters into colors.) The unique capabilities of the IDID have been demonstrated in a number of field experiments.

Figure 13 shows the raw image and several processed images of an automobile under a cloudy summer sky. The circular wafer creates the polarization-sensitive area. The Ronchi ruling is clearly seen outside this area, as are some drops of excess optical cement. Notice that the ordinary-ray image and extraordinary-ray image are similar, but the difference (polarization) image allows one to see the polarization easily. The glass polarizes light much more strongly than do the painted metal parts.

Light reflected from the front window of the car is dominated by the horizontally polarized component. Light reflected from the side window mainly consists of the vertically polarized component, whereas the surrounding scene is mostly unpolarized. These observations actually confirm a simple physical analysis, as follows. For specular reflection, unpolarized (as assumed for a cloudy sky, or light coming directly from the vicinity of the Sun) incident light of intensity I_s is attenuated according to the Fresnel reflection coefficients $F_{\|}$ and $F_{\perp}$ for its parallel and perpendicular components, respectively, with respect to the specular plane consisting of the surface normal and viewing direction. For the front window of the car, the specular plane lies along the vertical direction. Combining the diffuse intensity I_d, which is known to be isotropic for not too large a viewing angle, we have[5]

$$A = \frac{F_{\perp}}{F_{\perp} + F_{\|}} I_s + \frac{1}{2} I_d, \quad (13)$$

$$B = \frac{F_{\|}}{F_{\perp} + F_{\|}} I_s + \frac{1}{2} I_d. \quad (14)$$

For a glass surface, $F_{\perp}/F_{\|} \approx 7$ for a specular angle $\psi \approx 45°$, as in our case. By assuming $I_d \approx I_i$ (appropriate for an extended light source), we obtain

$$Q = \frac{F_{\perp} - F_{\|}}{F_{\perp} + F_{\|}} \cdot \frac{I_s}{I_s + I_d} \approx \frac{3}{8}. \quad (15)$$

This is very close to what we observed after taking the calibration curve into account.

For the automobile's side window, the specular plane lies in the horizontal direction and the roles of $F_{\perp}$ and $F_{\|}$ just exchange. This directly leads to $Q \approx 3/8$, also close to what we observed.

Using the IDID we have obtained many other polarization images of electronic components (for fault detection) and of natural scenes. They reveal, for example, the polarization of the sky on a sunny day and the polarization of light reflected from water surfaces.

APPLICATIONS

The IDID has a wide range of applications. In computer vision, it can immensely simplify some important visual tasks that are more complicated or even infeasible when one is confined to using intensity information. Material classification is one example. Experiments on circuit board inspection show that it is easy to discriminate between metal and dielectrics according to their conductivities. In robot vision, polarization information aids in identifying three-dimensional objects. For example, under most lighting conditions, the front and side of a dielectric object will have opposite

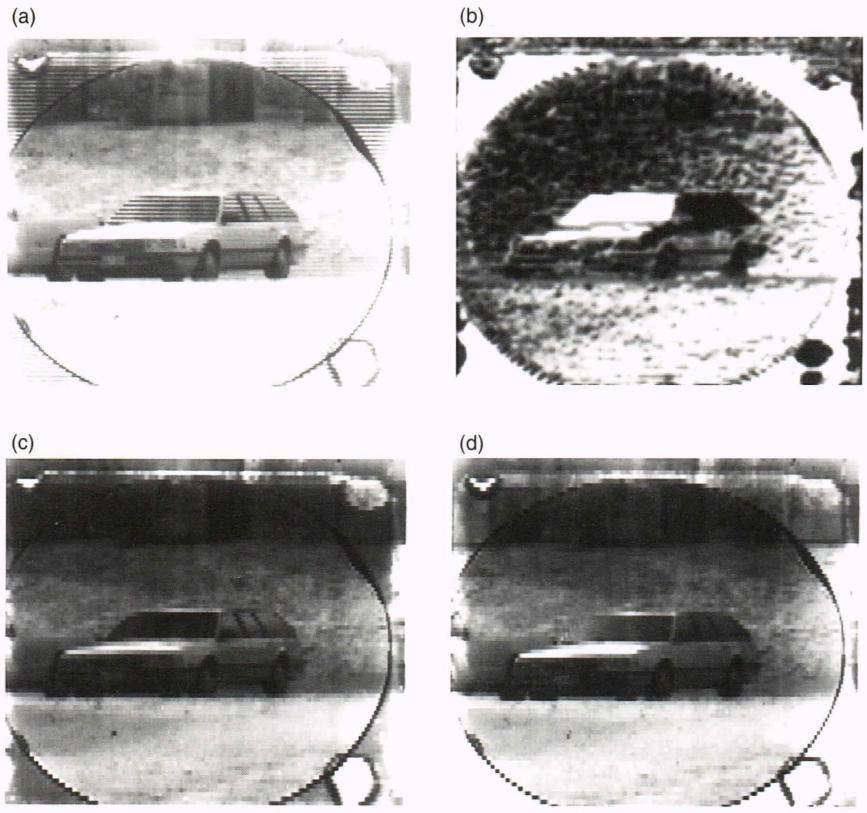

Figure 13. Images obtained with the IDID prototype. (a) Original image showing the circular wafer, blobs of glue, and the Ronchi ruling. (b) Polarization image showing horizontally polarized light (white) from the automobile front windshield and vertically polarized light (black) from the side windows. (c) Ordinary-ray image. (d) Extraordinary-ray image.

polarization. In environmental sensing, the IDID can detect variations of phenological characteristics of crop canopies, such as corn flowering and water stress, from polarization measurement of reflected light.

In the course of our work, we realized that other image qualities, such as spectral content and focus, could be measured with high speed and precision if they could be encoded as polarization. For spectral studies, the IDID can be used behind a birefringent Fabry–Perot etalon or other filters (e.g., dichroics, Lyot-type filters) that encode spectral information in orthogonal states of polarization.[6] One method of encoding with a birefringent etalon is described by Bonnaccini and Smartt[6] and by Rust.[7] They show that an etalon made of lithium niobate, which is an electro-optic birefringent crystal, has two series of passbands distributed across a broad spectral region. The light passed by one set of bands is polarized orthogonally to light passed by the other, and wavelengths passed by one set of bands can be changed by application of voltage to the crystal. A lithium niobate etalon and the IDID can scan the spectrum with one passband and hold the other fixed to provide a reference image for precision photometry of molecular and atomic lines.

When an auxiliary filter is used to encode wavelengths as polarization, $A - B$ would represent a point in the spectrum corrected for background. In another application, the quotient $(A - B)/(A + B)$ would represent the Doppler velocity of the solar gases when images A and B come from the two wings of an atomic line.

Earth Science

NASA's Earth Observing System is an important component of the U.S. research thrust to learn more about our environment. The Earth Observing System and other Earth-observing missions will need to map atomic and molecular emissions with unprecedented spectral and spatial resolution. To understand the chemistry and transport of molecular species in the middle atmosphere, the concentrations of O_3, N_2O, CH_4, $CFCl_3$, CF_2Cl_2, HCl, HNO_3, H_2O_2, HNO_4, $ClONO_2$, etc., should be mapped with 10% accuracy, at least. It will require precision spectroscopic imaging, and we plan to test the IDID in this area.

Other uses for the IDID are emerging in studies of the energetics of the upper mesosphere and lower thermosphere, where thermodynamic equilibrium cannot be assumed to control the emission rates. Emission line profiles for OH, NO, and CO_2 need to be studied with high time and spatial resolution to determine the composition and temperature structure of the region. Narrow-band images will help to measure the spatial variation of the outgoing energy.

Although remote sensing of surface features relies most heavily on morphology and color, there is growing interest in polarimetric measurements. For example, Masuda and Takashima[8] describe how the thermodynamic phase of water droplets and ice crystals in cirrus clouds might be determined from photopolarimetry. Rondeaux and Herman[9] show that polarimetric imagery provides a potentially rich source of data on flowering and water stress in corn and soybean crop canopies.

Solar Research

We plan to use the IDID to attack some particular problems encountered in solar research. As discussed by

Kunches et al.,[10] manned exploration of space beyond Earth's magnetosphere will require substantial improvements in the reliability of solar activity forecasts. Without good forecasts, the freedom of astronauts to explore the Moon and to carry out extravehicular activities will be limited because of the threat of lethal or disabling protons from flares. Because all solar activity, including the eruptive flares and mass ejections that disturb the geomagnetic field, arise from the action of solar magnetic fields, we are interested in making as precise measurements of those fields as possible. Maps of solar surface magnetic fields can be constructed from measurements of the polarization in sunlight, in spectral lines sensitive to the Zeeman effect.[11]

CONCLUSION

The IDID is a versatile polarization imager whose principal advantage is that it records two planes of polarization in a scene simultaneously and through virtually the same optical paths. Thus, it is especially useful in rapidly changing environments. It is also rugged and compact, so it joins other new sensors that are being developed to make observations from space less expensive. The underlying electronic design advances associated with this device may have wide applicability. Successful incorporation of signal-processing electronics in the sensor chips may show the way to reduce the amount of digital signal-processing hardware now required for many imaging applications. Precision relative spectrophotometry and polarimetry should be able to emerge from the benign environment of specialized laboratories and observatories for easier application to monitoring our environment.

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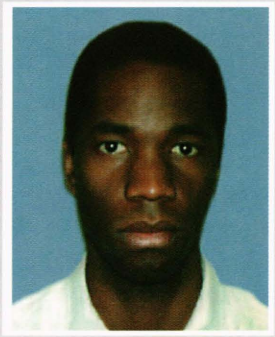

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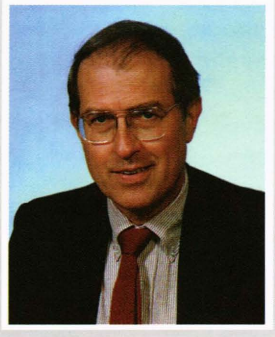

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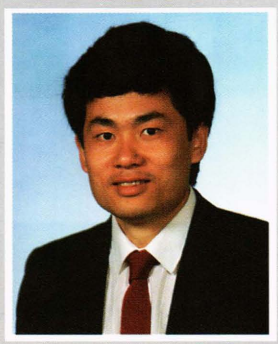

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