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RELIABILITY OF GALLIUM ARSENIDE DEVICES

Reliability qualification tests for space applications were carried out on several types of gallium arsenide transistors and process control monitors. A variability in the maturity and quality of the GaAs devices was determined. Failure analyses indicated that both subsurface defects and arsenic on device surfaces can lead to long-term burnout.

INTRODUCTION

The use of gallium arsenide (GaAs) transistors and integrated circuits for space and military applications has greatly expanded over the past few years. The main reasons for the exploitation of this compound semiconductor are that GaAs devices can operate at higher frequencies and have greater radiation hardness than their silicon counterparts. At this time, however, silicon technology still has a considerable lead in the area of reliability. The basis for the silicon's superior reliability is inherent and lies in the nature of its oxide, which can be grown under controlled conditions and has better protective properties. Unfortunately, the oxide of GaAs does not exhibit these qualities.

The purpose of our reliability studies of commercially available GaAs signal transistors is to assess independently their state of maturity for use in spaceborne radio frequency (RF) systems such as X-band transmitters and S-band beacon receivers. Specifically, in this article we report our evaluations of high-electron-mobility transistors (HEMT'S), signal metal-semiconductor field-effect transistors (MESFET'S), power MESFET's, and a digital process control monitoring device.

To assist the reader in understanding GaAs technology, we will first briefly describe the basic field-effect transistors (FET's) and then outline a few of their failure mechanisms. We will then discuss the results of the reliability testing and failure analysis. The article concludes with a summary of our findings.

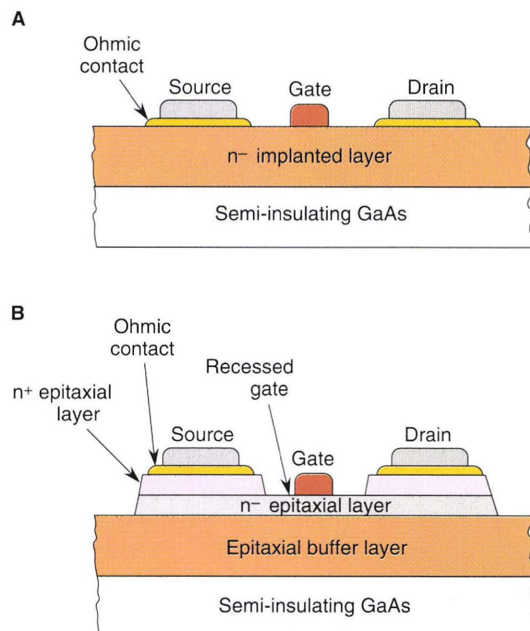


Figure 1. Cross-sectional views showing the evolution of GaAs metal-semiconductor field-effect transistor (MESFET) technology. **A.** The traditional MESFET is a planar, direct ion-implanted GaAs device. **B.** The newly developed MESFET has n^+ and n^- epitaxial layers and a recessed gate structure using a self-aligned process.

MESFET STRUCTURE

The traditional MESFET is a planar, direct ion-implanted GaAs device (Fig. 1A). A newly developed MESFET has n^+ and n^- epitaxial layers and a recessed gate structure using a self-aligned process (Fig. 1B). The new MESFET contains a buffer layer between a thin active n^- epitaxial layer and a semi-insulating GaAs substrate. The thickness of the n^- epitaxial layer is one thousand to a few thousand angstroms, and it has a carrier concentration of about 2×10^{17} cm^{-3}. The thickness of the highly resistive buffer layer is 3 to 5 μm, and it has a carrier concentration of less than 1×10^{14} cm^{-3}. The buffer layer confines carriers to the active region and thereby acts as a buffer between the semi-insulating GaAs substrate and the active layer. A recessed gate structure, which results from localized n^+ epitaxial contact layers for both drain and source pads, reduces the source resistance and improves noise figures. The heavily doped n^+ epitaxial layers enhance current transport through the metal-semiconductor interface by reducing the drain-to-source resistance. The most popular ohmic contact to GaAs is Au-GeNi. A Au-Ge mixture is evaporated from a eutectic film (88% Au, 12% Ge by weight), and a Ni layer is subsequently deposited to improve the melting of the eutectic film and increase the solubility of GaAs, thereby maintaining a smooth morphology. The gate length is less than 1 μm for higher gain, lower noise figure, and better frequency response. Most manufactur-

ers of MESFET's use the self-aligned gate process to control source-to-gate and drain-to-gate spacing. Aluminum is the most common gate metal; to achieve higher power handling, however, refractory metals such as Ti-Pt are being used as additives to Al. The gate metal should have characteristics such as high conductivity, good adhesion, and poor interdiffusion properties with GaAs up to 400°C.

The MESFET is the most common GaAs transistor technology because of its simple planar structure, ease of manufacturing, and high yield. Most GaAs foundries use MESFET structures for either digital or analog applications.

The failure modes observed to date for GaAs transistors have predominantly been wearout mechanisms caused by metal–GaAs interdiffusion.[1] Dielectric failures have not been observed frequently, and failure of the substrate material is not prominent because of the semi-insulating properties of GaAs. In GaAs MESFET's with Au or Al metallization, the major modes of failure caused by metal–GaAs interdiffusion are (1) ohmic contact degradation caused by interdiffusion to the source or drain of FET structures; (2) Schottky gate degradation caused by interdiffusion to the channel of FET structures;[2,3] and (3) electromigration, usually with Al metallization, on surfaces.

A combination of the first two failure modes has been shown to be responsible for gate-to-drain and gate-to-source shorts in GaAs power MESFET's.[4] Schottky gate degradation is sometimes observed as channel compensation or the "sinking gate" phenomenon[5] by combining electrical measurements with failure analysis.

In addition to the three failure modes just mentioned, two kinds of catastrophic failure[6,7] can occur with power MESFET's: (1) instantaneous burnout, which involves the thermal runaway of the buffer or substrate, and (2) long-term burnout, in which Ga is oxidized and As is reduced, eventually leading to the conduction of large currents and melting of the device.

HEMT STRUCTURE

A cross section of a typical HEMT grown by molecular beam epitaxy is shown in Figure 2. The top layer of 200 Å of highly doped 2×10^{19} cm^{-3} p$^+$-GaAs is confined to the gate region and serves to raise the surface potential of the gate to allow for higher doping levels in the lower n$^-$ layers. This increased surface potential can increase the aspect ratio of the device to avoid short-channel effects.[8] The n-GaAs contact layer allows for a low-resistance ohmic contact to the Ni–Au–Ge source and drain metallizations and prevents the AlGaAs layers from oxidizing. The n-GaAs contact layer, n-$Al_xGa_{1-x}As$ graded layer, and n-$Al_{0.3}Ga_{0.7}As$ constant-composition layer are all doped to 2×10^{18} cm^{-3} and have a combined total thickness of 400 Å. The 50-Å undoped $Al_{0.3}Ga_{0.7}As$ spacer layers separate the ionized donor atoms in the constant composition layer from the two-dimensional electron gas confined at the conduction band discontinuity at the spacer layer/undoped GaAs interface. The two-dimensional electron gas has an electron mobility of 6000 cm^2/(V·s) at room temperature; this is the quasi-ballistic transport "highway" that is unique to HEMT's. The undoped GaAs buffer layer also acts as a barrier to the diffusion of impurities and defects from the semi-insulating GaAs substrate during the molecular beam epitaxy growth and confines carriers to the channel region. Other features of conventional HEMT's include a closely spaced structure between the source and the gate to reduce the resistance of the two-dimensional electron gas layer, reduced gate-fringing capacitance, and a spatial parasitic resistance.[9] The p$^+$-GaAs layer was absent in devices from other manufacturers, and the gate consisted of a conventional Schottky diode.

When heterojunction structures such as HEMT's are evaluated, one must add the following to the previously mentioned MESFET failure modes: interdiffusion between semiconductor layers, which can destroy the stability of the desired heterostructure. As discussed earlier, the causes of the reliability problems are the lack of a stable oxide structure for compound semiconductors such as GaAs and the presence of possibly unstable heterojunctions in GaAs semiconductor structures. (For a more detailed list of failure mechanisms of these compound semiconductors, see Table 1.)

DEVICE EVALUATION

We evaluated MESFET's, HEMT's, and digital process control monitors from electrical measurements, thermal characterization, and the application of environmental stresses (thermal shock and accelerated aging). To date, shelf life (no bias), DC, and RF bias aging tests have been performed on GaAs devices and structures. The present conventional approach is to use DC bias conditions for small-signal devices in which the currents are small and the consequent heating effects are likewise small, where-

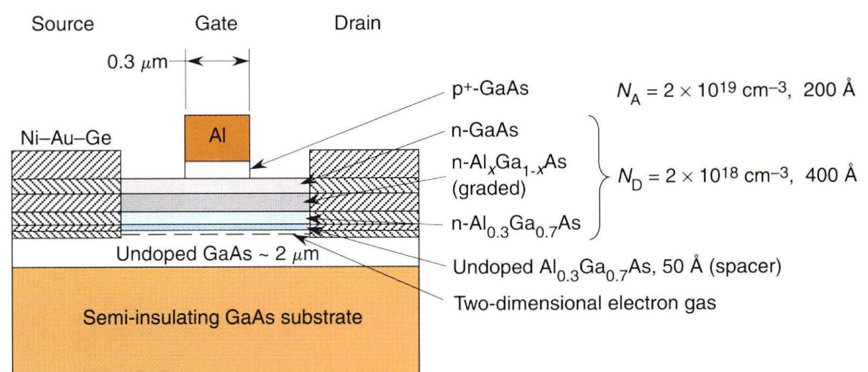


Figure 2. Cross-sectional view of a typical high-electron-mobility transistor grown by molecular beam epitaxy. N_A is the acceptor dopant level, and N_D is the donor dopant level. The lengths given in angstroms indicate the thicknesses of the layers.

Table 1. Failure mechanisms of GaAs compound semiconductors.

Failure mechanism	Acceleration factor	Accelerating conditions at failure site	Median life (h)	Failure site temp. (°C)
Field-effect transistors				
Sinking gate[a]	AE = 2.5 eV	245, 260, 275, 290, 310°C	$>1.6 \times 10^9$	150
Sinking gate[b]	AE = 1.34 eV	HTRB at 225, 250, 260°C RF bias at 200°C		
Burnout (breakdown)[c]	Unknown (early failure)	<150°C, <190°C, <225°C		
Au-Ga intermetallic[d]	24,000-hour test	T_{ch} = 140, 150°C		
Schottky degradation[e]		T_{ch} = 58, 190, 225°C		
W-Ni gate contamination[d]	4,000-hour test	T_{ch} = 83°C		
Interdiffusion				
Interconnect[a]	AE = 2.24 eV	250, 275, 300°C	$>8 \times 10^7$	150
Air bridge[a]	AE = 0.43 eV	200, 225, 250°C	$>2 \times 10^5$	150
Nichrome thin film[a]	AE = 1.03 eV	125, 175, 200°C	6×10^5	150
Electromigration				
Ohmic[a]	*N*-factor = 3.5 (203°C)	0.455, 0.91 mA/cm²		
Ohmic metal[e]	AE = 1.5 eV	<180°C, <240°C, <270°C		
Interconnect[a]	*N*-factor = 1.5 (300°C)	0.455, 0.91, 1.365 mA/cm²	$>8 \times 10^7$	150
Air bridge[a]	*N*-factor = 4 to 5 (250°C)	1, 2, 4 mA/cm²	$>2 \times 10^5$	150
Nichrome thin film[a]	*N*-factor = 3.0 (200°C)	2.5, 5.0, 7.5 mA/cm²	6×10^5	150
Gate metal voiding[c]	AE = 1.5 eV	T_{ch} = 150, 190, 225°C		
Gate metal voiding[e]	AE = 1.18 eV	T_{ch} = 180, 240, 270°C		
Integrated circuits				
Microwave amplifier[f]	AE = 1.75 eV	225, 240°C	8.4×10^6	150
Digital counter[g]	AE = 1.65 eV	260, 275°C	3.5×10^6	150
MMIC switch (sinking gate)[h]	AE = 1.3 eV	DC bias at V_{ds} = 8 V, 50% I_{dss}, T_{ch} = 225, 245, 260, 290°C		

Note: Blank entries indicate that the data were not available. MMIC = monolithic microwave integrated circuit, AE = activation energy, *N*-factor = current density exponent, HTRB = high-temperature reverse bias, RF = radio frequency, T_{ch} = channel temperature, V_{ds} = drain-to-source voltage, I_{dss} = drain-to-source saturation current. Table was prepared by W. Roesch of Triquint Semiconductor for the Electronic Industry Association JC-50.1 committee on GaAs reliability.

[a]Data are from Roesch et al., U.S. Conference on Gallium Arsenide Manufacturing Technology, Nashville, Tenn. (8–10 Nov 1988).

[b]Data are from Ersland et al., IEEE Gallium Arsenide Integrated Circuit Symposium, Nashville, Tenn. (7–9 Nov 1988).

[c]Data are from Russell et al., "Power GaAs FET RF Life Test Using Temperature-Compensated Electrical Stressing," in *Proc. 1986 IEEE International Reliability Physics Symp.*, Anaheim, Calif., pp. 150–156 (1986).

[d]Data are from Postal et al., "RF Operational Life Test of Power GaAs FET Amplifiers," in *Proc. 1983 IEEE International Reliability Physics Symp.*, Phoenix, Ariz., pp. 293–296 (1983).

[e]Data are from Riley et al., Gallium Arsenide Reliability Workshop, Portland, Oreg., Paper III.1 (13 Oct 1987).

[f]Personal communication from Rubalcava et al., TQS (Jun 1988).

[g]Personal communication from Ingle et al., TQS (Apr 1987).

[h]Personal communication from Ersland et al., M/A COM (1988).

as RF bias conditions are deemed necessary for power devices to correctly simulate the duty cycle and its consequent heating. We judge that storage or shelf tests are of little use since no field is present in the semiconductor material. Failure mechanisms such as electromigration and interdiffusion are generally accelerated by the electric field in such devices.

Signal MESFET Evaluation

Three types of GaAs MESFET's were evaluated for long-term reliability. The HMF-0314 device is a signal MESFET with a gate length of 0.5 μm; the P35-1140 and NE-710 devices are similar transistors, each with a gate length of 0.3 μm.

Thermal shock tests of 1000 cycles between temperatures of −65°C and 150°C with fifteen-minute dwell periods were carried out to determine the integrity of the contacts to the GaAs. Samples were unbiased during environmental stress. Drain-to-source saturation current (I_{dss}), gate-to-source pinch-off voltage (V_{gsp}), transconductance (g_m), and leakage currents were monitored initially and after 250, 512, 750, and 1000 cycles of thermal shock. Pertinent results were the following:

1. After 1000 cycles of thermal shock, the following failure ratios were found with respect to the gate-to-source leakage current (I_{gs} > 10 μA): P35-1140 (0.3-μm MESFET), 2/4; NE-710 (0.3-μm MESFET), 1/8; and HMF-0314 (0.5-μm MESFET), 0/4.
2. All devices passed the package hermeticity test after completion of thermal shock. Package hermeticity is checked by a leak test.
3. After 1000 cycles of thermal shock, the P35-1140 transistors showed a 5% decrease in performance with respect to I_{dss}. The NE-710 and HMF-0314 transistors showed no significant degradation.

Before life testing, the devices were characterized over a −60°C to 100°C temperature range by measuring the variation in DC parameters such as I_{dss}, V_{gsp}, g_m, and leakage currents. The DC bias conditions for the life test were carefully established to produce junction temperatures of 200°C to 210°C in the transistors while in a constant-temperature oven. Before, during, and after the 1000-hour life test, we measured both DC and RF (S parameters) responses to be able to correlate any degradation in these two sets of data due to aging. The forward transmission scattering parameter is S_{21}, whose amplitude, when squared, is equal to the maximum available gain from an RF device.

Figure 3 shows that the HMF-0314 MESFET was the only one to suffer significant degradation in I_{dss} over the duration of the test. Figure 4 shows the substantial degradation of S_{21} for the HMF-0314 MESFET, which is significant and correlated with the considerable decrease in I_{dss} for the same device type. The NE-710 and P35-1140 MESFET's showed no significant degradation in either DC or RF parameters that was caused by the life test.

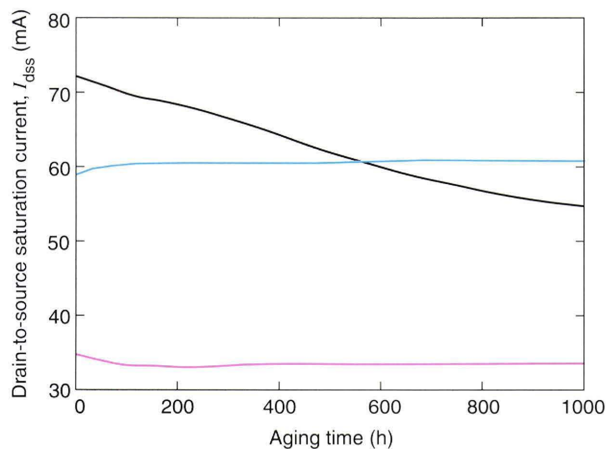


Figure 3. Drain-to-source saturation current as a function of aging time for three different signal metal-semiconductor field-effect transistors: HMF-0314 (black), P35-1140 (blue), and NE-710 (red).

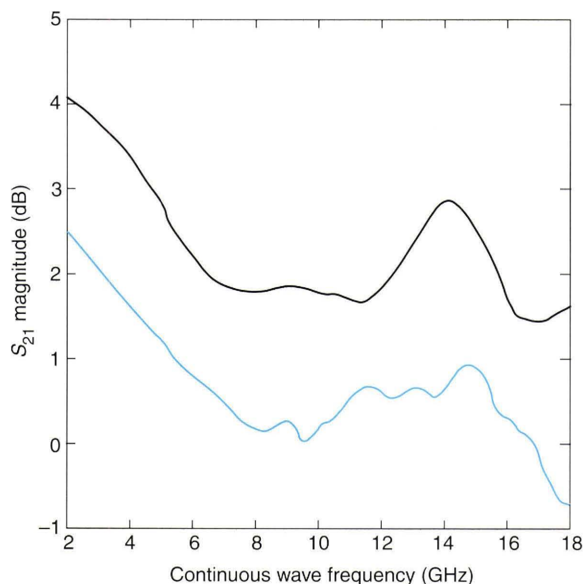


Figure 4. Frequency response of the forward transmission scattering parameter (S_{21}) magnitude, initially (black) and after 1000 hours (blue) of the life test, for the HMF-0314 device.

HEMT Evaluation

Accelerated life tests were also performed on three types of GaAs HEMT's: NE-202, MGF4302A, and FHX06FA. As for the signal MESFET's, the life tests were carried out in an oven at a temperature of 180°C to produce a channel temperature of 200°C in the HEMT's when DC bias was applied. The DC bias consisted of a drain-to-source current (I_{ds}) of about 10 mA at 3 V, which was carefully controlled by an active feedback loop to maintain a constant channel temperature during the test. This bias current is about 33% of the I_{dss} for each HEMT type. Five samples of each type of GaAs HEMT were subjected to the life test: DC measurements were made at 0, 25, 50, 100, 250, 500, and 1000 hours with an HP 4142B parameter analyzer; RF measurements were made at 0, 250, 500, and 1000 hours with an HP 8510 network analyzer. The findings were the following:

NE-202. The mean I_{dss} decreased from 29.6 to 22.9 mA for the five NE-202 samples as a result of the life test. This decrease represents an average degradation of 23% caused primarily by a 50% decrease in I_{dss} by one device. The other four devices had a mean decrease in I_{dss} of just 15%. No pinch-off voltage failures occurred for these HEMT's, and the magnitude of S_{21} degraded by less than 1 dB across the frequency range of 2 to 18 GHz (Fig. 5).

MGF4302A. These five devices exhibited wide scatter in their I_{dss} and transconductance data, even initially. One device exhibited a large increase in I_{dss} and g_m as a result of the life test, probably a kind of burn-in phenomenon. The other four devices, which showed more stable DC behavior, had less than 5% degradation in the magnitude of S_{21} across the 2- to 18-GHz frequency range after the 1000-hour life test (Fig. 6). Although no catastrophic failures were experienced, two of the devices did not pinch off I_{ds} to 100 μA with V_{gsp} as low as −5 V at the completion of the life test, thereby violating the V_{gsp} specification.

FHX06FA. The performance of these HEMT's was very unsatisfactory. One device would not pinch off after 25 hours of exposure; a second failed in a similar manner after 100 hours; and a third device failed after 250 hours. A fourth device showed a 57% negative shift in V_{gsp} at the completion of the 1000-hour test. Devices completing the life test also exhibited large increases in leakage currents.

Power MESFET Evaluation

A reliability study of FLC053WG (0.75 W) and FLM7785-8C (8 W) MESFET's was also conducted. Specifically, DC bias life tests of FLC053WG and FLM7785-8C power MESFET's were carried out, and a life test of an FLM7785-8C device with DC bias and RF drive was performed to detect any RF output power degradation that might occur.

The life test for FLC053WG devices was performed on a temperature-adjustable hot plate in an enclosed chamber. The test was run at a junction temperature of about 175°C for each device. The DC bias conditions were

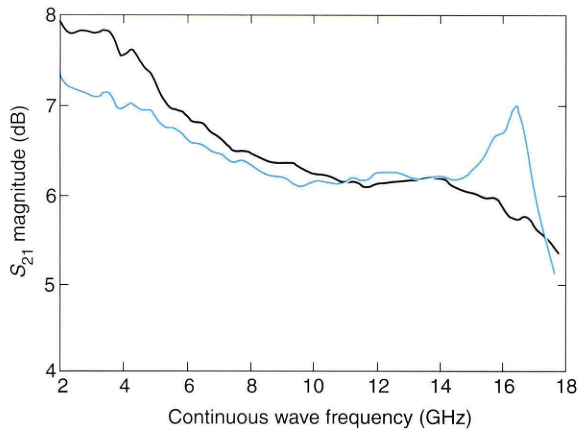


Figure 5. Frequency response of the forward transmission scattering parameter (S_{21}) magnitude, initially (black) and after 1000 hours (blue) of the life test, for the NE-202 device.

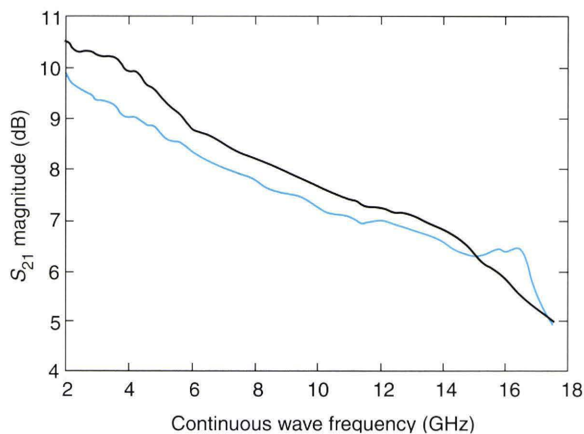


Figure 6. Frequency response of the forward transmission scattering parameter (S_{21}) magnitude, initially (black) and after 1000 hours (blue) of the life test, for the MGF4302A device.

as follows: I_{ds} = 60% of I_{dss}, and V_{ds} = 10 V. The V_{ds} of 10 V was derated from the absolute maximum of 15 V since the FLC053WG devices previously proved to be incapable of surviving more than 200 hours of the life test at the maximum V_{ds} bias.

The results of the life test for the FLC053WG devices showed that after 1000 hours of aging, the mean I_{dss} decreased from an initial value of 271.9 mA to 263.3 mA, a change of about 3%. One of the FET's remained unchanged, whereas the rest varied from 2% to 6%. No pinch-off voltage failures occurred. The gate-to-source leakage currents stayed quite constant. The S_{21} parameter (measured only for one MESFET) changed by 5.7% at a test frequency of 8.475 GHz.

Subsequent to the 1000-hour life test, step stressing was performed by incrementally increasing I_{ds} to determine whether the devices could tolerate higher levels. At 80% of I_{dss} with V_{ds} derated to the original 10 V, three of the five transistors ceased to function after less than forty-eight hours.

The test setup for the DC bias life test of the FLM7785-8C devices consisted of a temperature-adjustable hot plate, power supplies, temperature monitors, and associated mounting hardware. The DC bias conditions were the same as for the FLC053WG devices, and the junction temperature was kept at 175°C.

Two samples were tested. After 1000 hours of aging, the first sample experienced changes of 3.05%, 1.44%, 0.476%, and 26% in the I_{dss}, V_{gsp}, g_m, and S_{21} parameters, respectively. The changes in the same four parameters for the second sample were −11.9%, −2.4%, 1.9%, and 0.15%, where the minus signs indicate a decrease.

The purpose of the RF output power degradation test was to determine whether the FLM7785-8C power MESFET being used in a three-stage amplifier, which consists of one FLC053WG, one FLC253MH-8 (a 1.5-W MESFET), and one FLM7785-8C in cascade, is susceptible to a phenomenon called "power slump." Power slump is a condition in which a power MESFET exhibits a gradual decrease in output power over a period of time when driven into compression by a large microwave signal. (Compression is the state in which the output power of the device no longer increases linearly with increasing input power because of nonlinearities of the MESFET.) Power slump is believed to be caused by voltage breakdowns that occur when the microwave signal amplitude is at its positive or negative extreme.[10] At the moment a voltage breakdown occurs, a short current pulse exists. This repeated voltage breakdown current is what causes the observed output power degradation. The power slump susceptibility is dependent on the amplitude of the input RF drive signal.

The output-power life test of the FLM7785-8C power MESFET was conducted with DC bias and RF drive. The test was set up in accordance with the block diagram shown in Figure 7. The DC bias conditions for the driving three-stage amplifier were V_{gs} = −0.8 V, and V_{ds} = 9 V. The microwave generator was set at a frequency of 8.475 GHz and at a power level that enabled the amplifier to operate at about the 1-dB compression point. The DC bias conditions for the test device were V_{gs} = −1 V, and V_{ds} = 9 V; the operating junction temperature was estimated to be 85°C.

After more than 1000 hours of the life test, the MESFET remained operational with no apparent slump in the RF output power and no significant degradation of DC or RF parameters.

Evaluation of the Digital Process Control Monitor

In developing a beacon receiver, one approach implemented a custom-designed, digital, GaAs integrated circuit consisting of a phase accumulator, high-speed read-only memory, and a digital-to-analog converter. This custom integrated circuit is functionally known as a direct digital synthesizer. A digital GaAs foundry may be chosen to fabricate this device because of the low-power characteristics of its direct coupled FET logic process.[11]

The foundry process uses self-aligned enhancement and depletion (E/D) MESFET's with four types of metals for interconnection. This self-aligned process fabricates the n^+ ohmic contact region using the gate as a mask; therefore, the drain and source are aligned with the gate. The process control monitor includes E/D FET's with various gate lengths and widths, contact metals, gate metal, metal

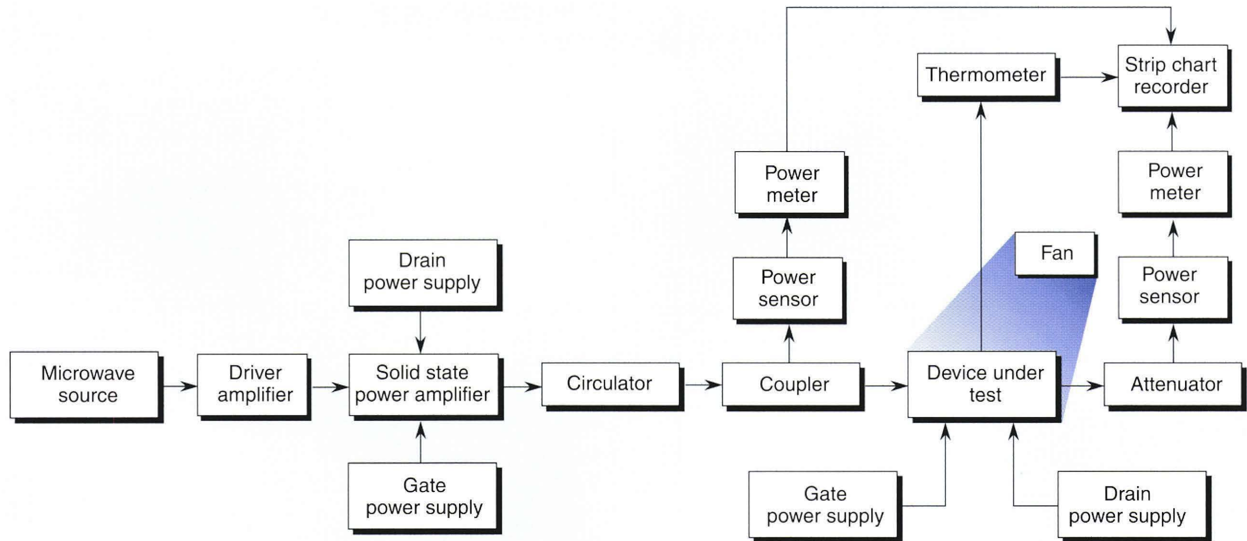


Figure 7. Test setup used in evaluating the susceptibility of the FLM7785-8C power MESFET (metal-semiconductor field-effect transistor) to power slump.

resistors, and so on. Our study focused on the active components in these process control monitors.

The E/D FET's were selected because their gate widths and lengths were close to the design requirements. For example, one inverter implementation uses a depletion FET (DFET) as an active load and an enhancement FET (EFET) as a level shifter. The drive capabilities of these E/D FET's can be boosted by careful sizing of the gate lengths and widths. We have investigated the uniformity of the threshold voltage (V_{th}) and I_{ds} for matched FET pairs, the variation of V_{th} and I_{ds} for perpendicularly aligned FET's, the transistor sizing effects on V_{th} and I_{ds}, and the thermal characterization of V_{th}.

The test results were compared with the appropriate design rules to observe the variance of the device parameters. A 1000-hour life test was performed where data were taken initially and after 100, 300, 500, and 1000 hours to estimate the long-term shift in the device parameters.

Ten packaged process control monitors (forty E/D FET's in all) were used for testing, and four packaged devices were used as controls. Since typical FET's have a power dissipation of less than 1 mW, the junction temperature of the die was estimated to be the same as the base plate temperature, 125°C. Threshold voltage measurements were made on all transistors over the temperature range from −30°C to +70°C.

The following observations were made:

1. Layouts of process control monitors are extremely compact, and the accessibility to the bond pads is poor.
2. The adjacent FET's (also known as "matched FET's") indicated excellent V_{th} uniformity and verified the repeatability of our experimental setup.
3. The perpendicular E/D FET parameters were the same to within 10% to 20% of the adjacent FET's.
4. The DFET's stabilized before burn-in, and the EFET's stabilized after 100 hours of burn-in (Figs. 8 and 9).

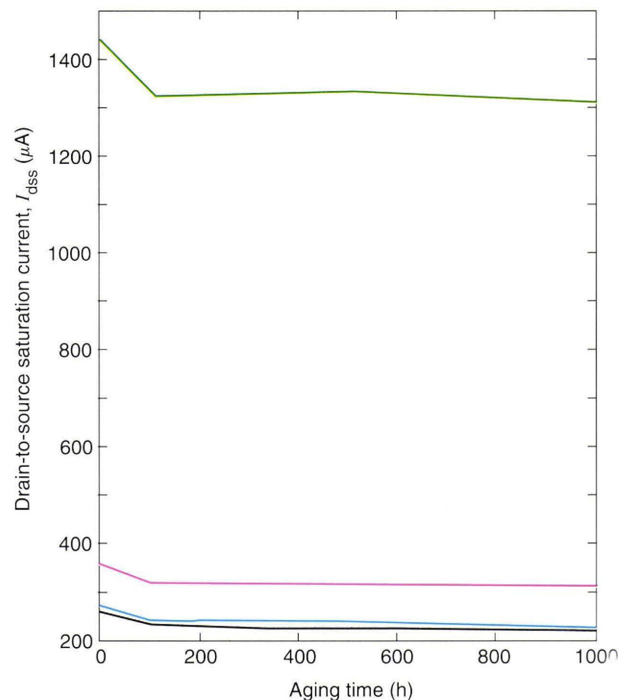


Figure 8. Degradation of four different enhancement field-effect transistors over the 1000-hour life test.

5. V_{th} varies by about −1.2 to −1.3 mV/°C. This change in V_{th} was found to remain constant over the entire temperature range (−30°C to 70°C), and it is consistent with the manufacturer-reported value of −1.0 mV/°C .[12]
6. I_{ds} scaled linearly with the gate width for the same gate length. This finding agreed with the theoretical result that I_{ds} is proportional to the ratio of the gate width to the gate length.[13]

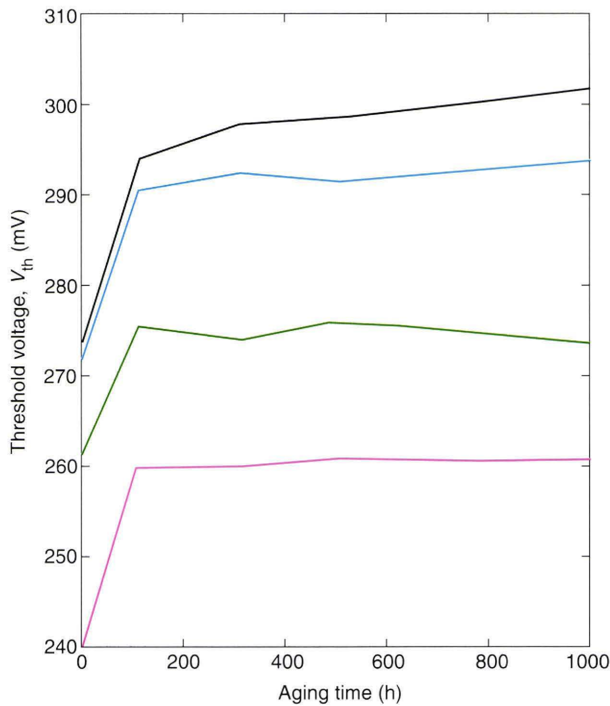
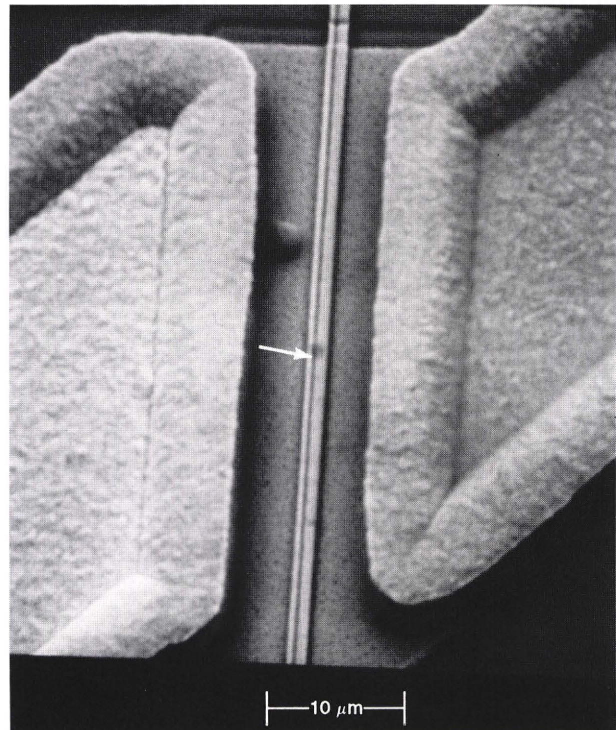


Figure 9. Threshold voltages of four different enhancement field-effect transistors as a function of time. The curves are color-coded to show correspondence to the four devices in Figure 8.



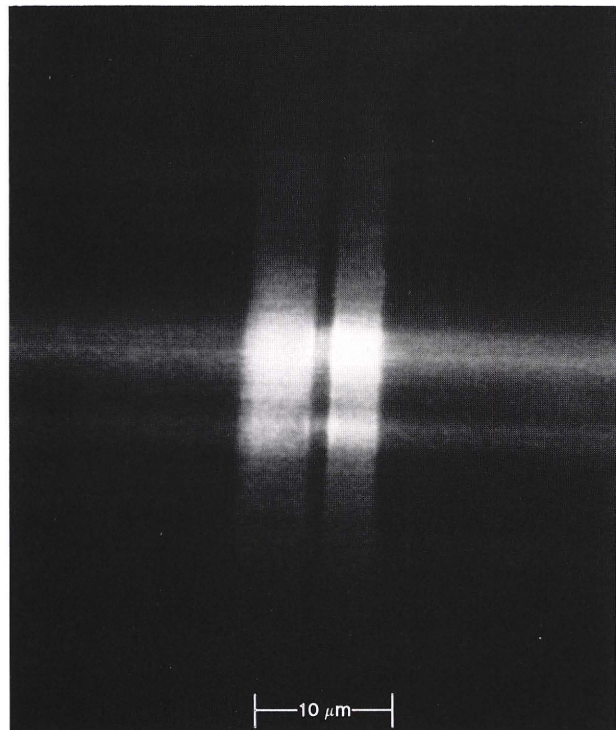


Figure 10. Photographs of a Fujitsu device that underwent a 1000-hour life test. The secondary electron image (top) reveals only a darkened area (arrow) at a point of gate-to-source current leakage seen in the source current image (bottom).

FAILURE ANALYSIS

The HEMT and power MESFET devices were analyzed for cause of failure. The analysis was performed with a scanning electron microscope (SEM) equipped with an ion pump and electrical feed-throughs so that transistors could be observed in an active state and in a clean environment if the device was still working. The SEM included an X-ray detector for microanalysis. The SEM images were made by exploiting two distinct signals. The more common method of collecting the secondary electrons emitted from the sample surface was employed to image all examined devices. When an active device was in the microscope, the source current from the transistor itself was fed to an ancillary preamplifier and used directly to make the photographs. As discussed later, this process produces information and details not available in the secondary electron mode. X-ray microanalysis was useful for determining the local compositions of the variety of structures or unusual areas on a device under scrutiny.

HEMT Failure Analysis

Both failed and control HEMT devices were subjected to failure analysis. Transistors of this sort from Fujitsu, Mitsubishi, and NEC corporations were examined. A control device from each maker was examined for comparison with the failed transistors. The control devices had only been characterized electrically and were not subjected to aging. In general, HEMT's that had failed parametrically were examined, although we also occasionally looked at catastrophic failures. The aged devices were subjected to a junction temperature of 200°C for 1000 hours. That investigation was described in detail in the literature.[14,15]

Figure 10 presents photographs of a Fujitsu FHX06FA HEMT that had undergone 1000 hours of aging. In the secondary electron image, one observes a barely noticeable darkened area along the gate metallization of the

transistor. In the source current image mode, a bright spot occurs, indicating a subsurface defect resulting in current leakage from the gate to the source. A similar pair of images is shown in Figure 11. Here, however, the secondary electron image gives no hint at all of trouble. The source current image reveals a dark spot, however, indicating a point of gate-to-drain current leakage.

Sometimes a surface defect was obvious, such as the one shown in the top of Figure 12, where an eruption along the gate metallization is clearly visible on another Fujitsu device. The localized eruption is associated with an expanded area of gate-to-source current leakage, as demonstrated in the source current image in the bottom of Figure 12. For the Fujitsu HEMT's, we observed that transistors with large initial leakage currents due to defect areas along the gate eventually developed into areas of increased current leakage that correlated with an inability to electrically pinch off the transistor.

The control MGF4302A device from Mitsubishi had an intriguing area in the central gate region that caused the HEMT to stop conducting when a 20-keV electron beam penetrated the area and the gate potential was 0.05 V more positive than the pinch-off voltage. This switching effect did not happen with 10-keV beam energy, indicating that the anomaly responsible for the effect was deeper than 500 nm, as determined by Monte Carlo calculations of electron beam penetration. This depth corresponds to a defect in the 2000-nm undoped GaAs buffer, making it appear as if current is leaking through the buffer. This defect did not appear to affect the electrical characteristics of the HEMT.

Investigation of an NE-202 control HEMT did not reveal anything unusual, and the transistor seemed to behave as designed. Analysis of an NE-202 transistor that experienced a catastrophic pinch-off voltage failure during the life test revealed two extraneous pieces of material along the edge of the gate. This material appeared to have resulted from a processing problem during manufacture. A source current image of the same region revealed a gate-to-source current leakage area just above one of the extraneous pieces of material. Another NE-202 transistor had a 50% decrease in I_{dss} during the life test; that is, it suffered a parametric failure after 1000 hours of aging. The analysis indicated an anomaly in a region along the gate for electrical conditions under which the transistor should have been turned off. The transistor suffering the catastrophic failure had leakage currents 10 times larger than those of the transistor that failed parametrically.

Other investigators have reported similar failure mechanisms for GaAs HEMT's. Buot et al.[16] proposed a mechanism leading to subsurface burnout in GaAs HEMT's in which a highly-positive-temperature coefficient region is heated so that thermal runaway occurs in the presence of an electric field; this region bridges two metallic filaments with different potentials that have been formed by interdiffusion of metallization with the GaAs and AlGaAs semiconductor layers. Anderson et al.[17] pointed out that compound semiconductors such as GaAs typically have 1000 times more flaws or lattice dislocations than silicon has. This fact alone enhances migration and interdiffusion due to weak bonding. Thus, we conclude that the subsurface defects causing failure in the HEMT's were either latent defects present originally in the GaAs material or created during the aging test by the thermal runaway/bridging phenomenon, or a combination of both.

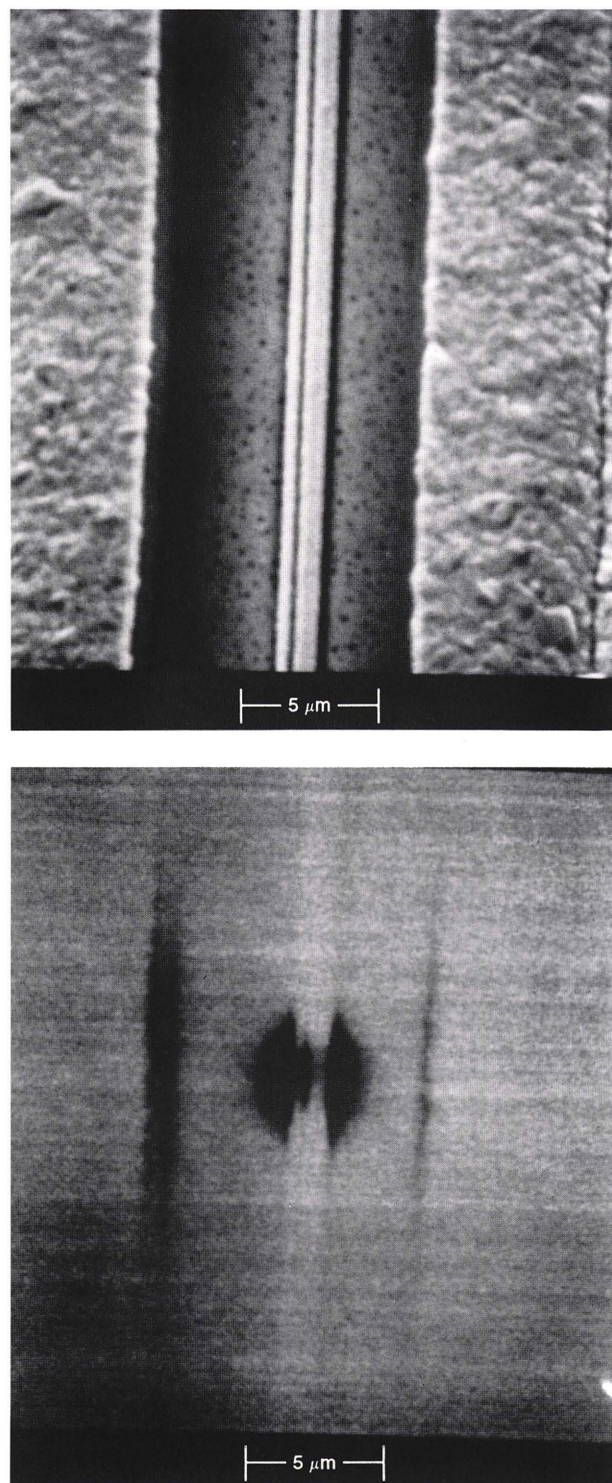
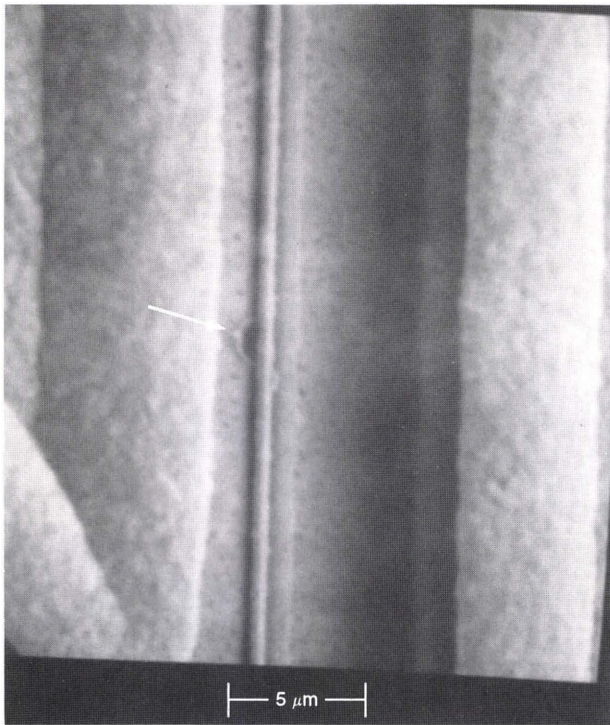


Figure 11. Secondary electron image (top) and source current image (bottom) of a gate-to-drain leakage current defect (darkened area along gate metallization) in another area of the Fujitsu device shown in Figure 10. The secondary electron image has no distinguishing characteristic.



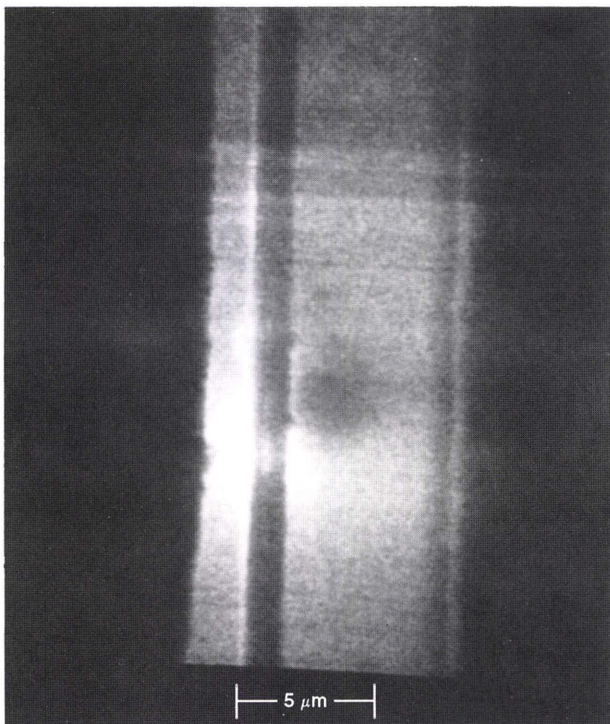


Figure 12. The secondary electron image (top) shows a large blown-out area (arrow) on the left side of the gate metallization. The source current image (bottom) shows leakage over an expanded region associated with this defect.

Power MESFET Failure Analysis

The lids were removed from five FLC053WG power MESFET's, and the devices were examined with the SEM. Three of the devices ceased to function and had undergone burnout failure, as shown in Figure 13. One of the transistors had an extensive network of filaments growing on top of the residual Au metallization, as shown in Figure 14. X-ray microanalysis of the filaments on the Au revealed the spectrum shown in Figure 15; a substantial amount of As is seen, but no trace of Ga is present. The other two failed MESFET's had As associated with the Au but, again, no Ga. This failure is consistent with the long-term burnout mechanism described by Wemple et al.[6] that was referred to earlier in this article.

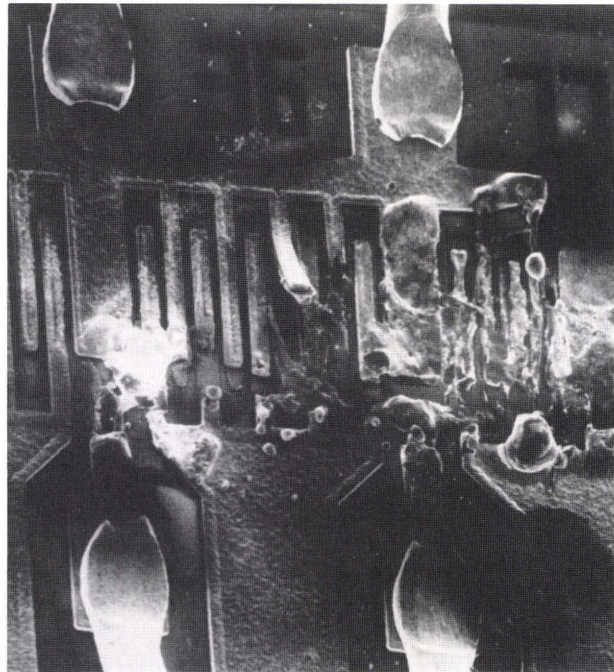


Figure 13. Metallization of a power MESFET (metal–semiconductor field-effect transistor) after failure (5-kV acceleration of electrons, 20° off vertical, 300× magnification).

SUMMARY

As a result of our space qualification testing and associated failure analyses, we have found that the signal GaAs MESFET's are reliable enough for space applications; digital GaAs process control monitor performance indicates that digital GaAs devices can also be used for space applications with some burn-in to ensure stabilization; power GaAs MESFET's require substantial derating (25%–35%) of specified maximum parameters to be considered for long-life space use; and GaAs HEMT's are presently not mature enough for space systems.

If not derated, the power GaAs MESFET's exhibit a long-term burnout mechanism detectable by the As meshwork observed on the surface of the transistor during failure analyses—a phenomenon observed by others.

The phenomenological model that emerges from the HEMT failure analysis is that small defects, some of them in subsurface regions and indicated by high leakage currents on unstressed control devices, may cause localized overheating. The localized hot spots eventually erupt during DC biased accelerated life testing, creating large defect areas observed at the surface of the HEMT's in the gate region. The observation of these large defect regions

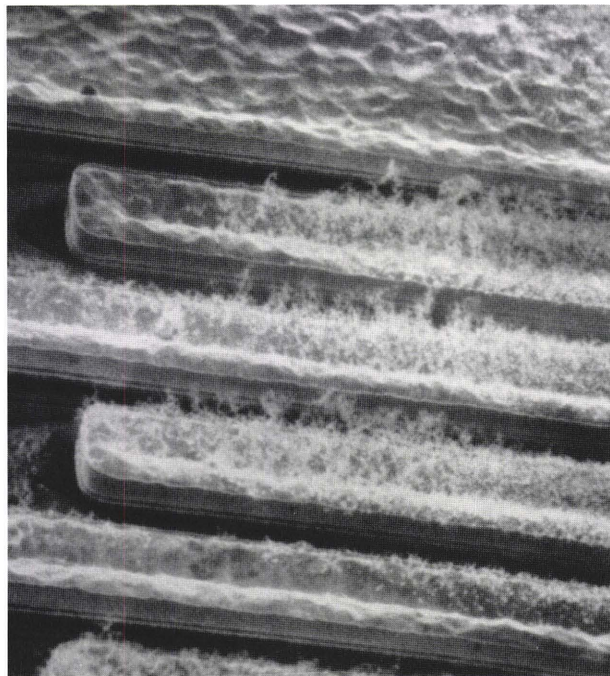


Figure 14. Meshwork growth on metallization of a power MESFET (metal-semiconductor field-effect transistor) (5-kV acceleration of electrons, 45° off vertical, 2000× magnification).

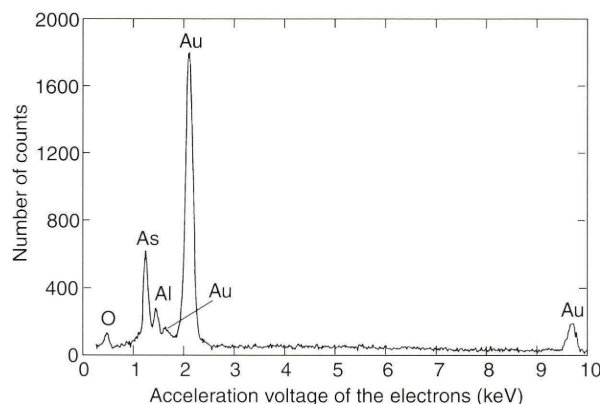


Figure 15. Chemical composition of metallization of power MESFET (metal-semiconductor field-effect transistor) shown in Figure 14.

is correlated with the loss of gate control and the inability to pinch off the HEMT's. Our life test experiments indicate that initial gate-to-source and gate-to-drain leakage currents should be less than 1 μA for successful results. Manufacturers' specifications for these parameters currently range from 10 to 50 μA, where V_{gs} ranges from −2 to −3 V.

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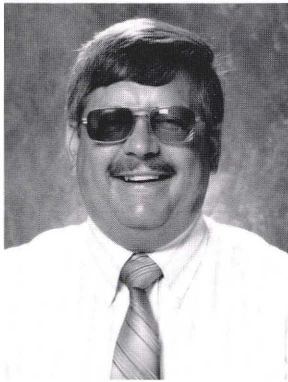

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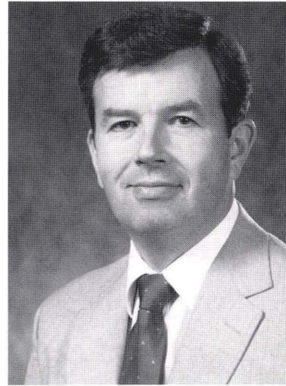

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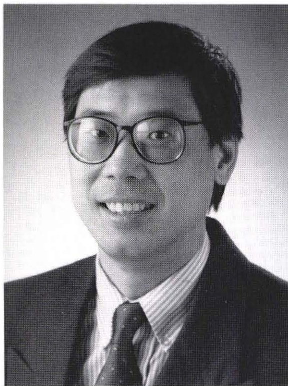

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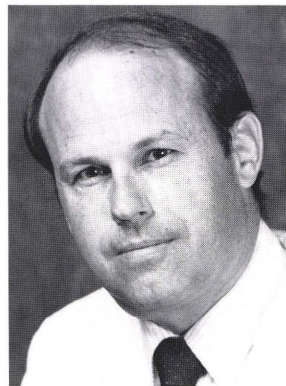

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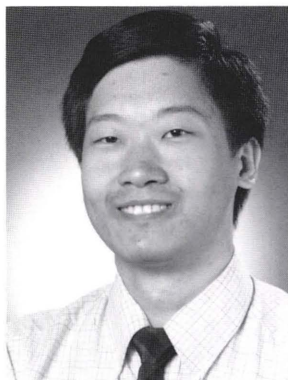

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