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MODELING FOR ELECTRONIC PACKAGING AT APL

In the expanding world of modern electronics and integrated circuits, the need for high-density, high-performance electronic circuit packaging is paramount. Key to any successful electronic packaging activity is the ability to model and analyze electrical, mechanical, and thermal system behavior before actual system design and fabrication. Details of an APL-developed set of computer-based models that allow the design and performance verification (electrical, mechanical, and thermal) of complex, high-speed (100-MHz clocks) digital circuits are described and applied to a high-performance radar signal processing circuit.

INTRODUCTION

The use of complex, high-density, very large scale application-specific integrated circuits in today's fast, high-performance systems requires careful attention to all aspects of electronic packaging. This includes the minimization of electrical losses and signal interferences, the elimination of excess thermal buildup, and the selection of proper materials and structural configurations to ensure mechanical integrity over the specified operational environment. To design efficient packaging structures, one must evaluate (and effectively model) the performance requirements, not only at the integrated circuit level, but also at the board and system levels. Package, board, and system-level models are not widely available and, except for a few open literature examples,[1,2] exist only as proprietary software. In what follows we describe an integrated set of computer-based models that allow the design and performance verification of complex, high-speed (100-MHz) digital circuit packages and boards. The models are based on several techniques, including finite element and difference, boundary value, analytical or Green's functions, transmission line, and circuit compaction or density.[3] These techniques can be used to predict electrical (impedance, signal rise and fall times, frequency response, crosstalk), mechanical (joint and board-level stresses), and thermal (temperature profiles and thermal resistance) performance. They can also be used to develop design guidelines for package selection, board layout, and circuit partitioning.

In a previous article[4] we described in detail the thermal and thermomechanical modeling, analysis, and testing of electronic packaging systems. Thus, the focus here will be the interdependence of the software and its use to predict layout density and electronic performance parameters.

Table 1 summarizes the model information, including the analytical technique, the origin of specific software codes, and the major parameters calculated. On the basis of *a priori* application of this software and its analytical results, rules for the electronic design of very large scale integrated (VLSI) circuits can be generated to ensure the successful performance of the system at implementation. Examples of these design guidelines for various chip technology families and common package and board-level structures are presented. We also discuss the specific application of these models and design guidelines for a digital, radar signal processor using surface-mounted packaging technology on dense, large-area (> 130 cm^2), multilayer, thick-film circuit boards.

SOFTWARE

The creation of software for electronic packaging engineering is time-consuming and costly. It requires not only extensive programming but also a well-devised and executed experimental validation plan. Thus, to minimize cost and have working code on-line as soon as possible, the packaging engineer must use all existing software tools (e.g., commercial, university, government). New software should only be written when the required software does not exist or is deemed too costly to acquire or operate. APL created at least six software packages (Table 1) to fill holes in the externally available software. These packages included code for the generation of circuit density (e.g., Rent's Rule[3]), skin resistance, crosstalk, electrical circuit parameters, rise time, and thermal resistance. For thermal and thermomechanical analysis, extensive use was made of computerized engineering workstations with commercially available finite-element pre- and post-processors (e.g., PATRAN[5]) in conjunction with finite-element analysis software (e.g., NASTRAN[6]), and finite-difference analysis software (e.g., SINDA, NET 5) on a mainframe computer. Commercial circuit and transmission-line analysis tools[7] were also used with internally generated software, which was written in Fortran[8] and designed to

Table 1. Computer-aided design and analysis tools for package and board-level modeling.

Analysis type	Parameters calculated	Model basis	Software origin
Thermal	Steady-state and transient temperature	Finite-element method	PATRAN/NASTRAN
	Thermal resistance	Finite-difference method	SINDA
	Thermal contours		NET 5 (JHU/APL)
		Analytical methods (e.g., Green's function)	JHU/APL
Thermomechanical	Displacements Stress Strain Deformed shapes Thermal/mechanical loads	Finite-element method	PATRAN/NASTRAN
Electrical simulation	Crosstalk Pulse shape	Analytical methods	SPICE
	Signal delay Overshoot	Coupled transmission lines	JHU/APL
Electrical parametric	Resistance, inductance, capacitance, conductance, impedance S parameters	Finite-element method	PATRAN/NASTRAN JHU/APL
	Skin resistance	Analytical methods	JHU/APL
		Boundary-element method	JHU/APL
		Coupled transmission lines	SPICE
		S-parameter analysis	Touchstone
Circuit density	Average wire length Number of leads Circuit density (lines per inch) Rent's Rule exponent	Analytical methods	JHU/APL

run on a personal computer. The software development activity also identified basic requirements for a completely integrated software suite for VLSI packaging design.[9]

Finite-element and finite-difference methods are especially useful for engineering analysis and modeling of large, complex, board-level systems. The formulas of the finite-element technique[10] and its associated software[6] can be used to model thermal, mechanical, and some electrical performance, simply by changing the finite-element grid elements and perhaps the boundary conditions. Chip carriers, pin grid arrays, and certain quad flat packages are particularly amenable to this type of analysis because of their eightfold symmetry, as shown in Figure 1.

CIRCUIT DENSITY

Some limited success in determining the wiring density for logic circuits has been achieved[3,11] by using the empirically derived Rent's Rule for device interconnections. This rule can be generalized for device packages and circuit boards. Approximating the wiring density before committing to a particular substrate technology can prevent costly redesign. When deciding whether a particular wiring technology is adequate to support the given circuit design, one must

1. Determine the maximum number of signal lines (vertical or horizontal) crossing any respective line on the circuit.
2. Determine the position of those lines where the crossings have the greatest density.
3. Determine the maximum lead length.
4. Determine, on the basis of maximum lead length, the design rules for parallel lead spacing as a function of the board technology, capacitive loading, and noise parameters.
5. Reduce wiring density caused by electrical vias (interconnections between layers of a multilevel substrate), thermal heat risers, etc.

The first three considerations depend primarily on the circuit design and the partitioning of the circuit into discrete integrated circuits. The last two depend strongly on the substrate wiring (board) technology itself and can

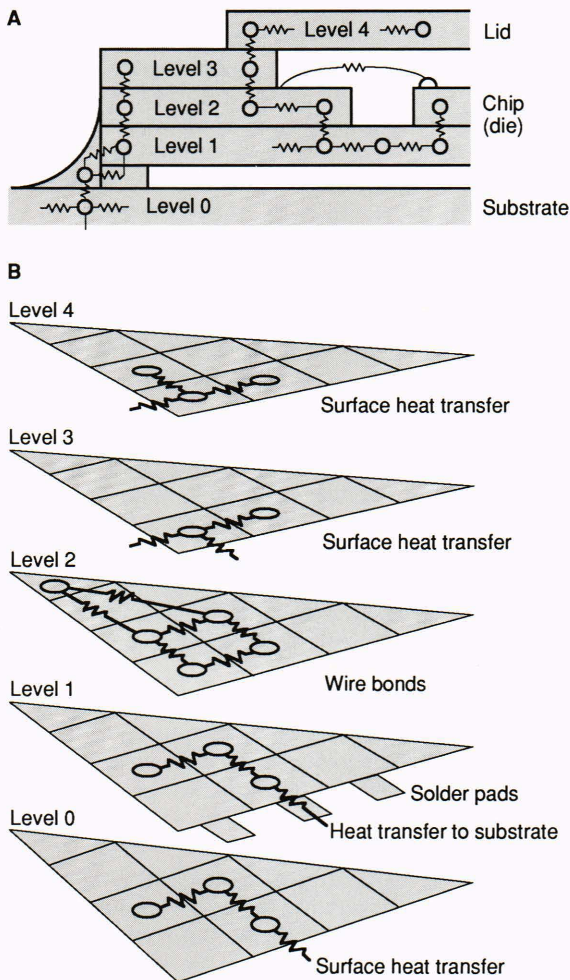

Figure 1. Finite-difference thermal modeling net for a typical ceramic chip carrier. **A.** Thermal network for chip-carrier package. **B.** Eightfold symmetry model of square chip-carrier package.

be used to evaluate the merits of a given technology against the design requirements.

Rent's Rule for multichip packaging states that the number of active leads P on a circuit (e.g., board, hybrid, etc.) containing g gates can be expressed as

$$P = ag^b \ , \tag{1}$$

where a is the average number of connections per gate, and b is the experimentally determined Rent's exponent. Equation 1 can be reformulated in terms of the ratio of package leads to chip pads

$$G = \sum_{i=1}^{m} N_i g_i = \sum_{i=1}^{m} N_i \ (P_i/a) \ , \tag{2}$$

where

G is the total number of gates on a multichip circuit card or module,

N_i is the number of type i components,

m is the number of different devices, and

P_i is the number of active leads on device i.

The total package lead count P_T for the circuit board is

$$P_T = aG^b = \left[\sum_{i=1}^{m} N_i \ (P_i)^{1/b} \right]^b \ . \tag{3}$$

In actual circuit application, the number of package inputs and outputs and the number of active pins are known, but the exponent b is unknown. This Rent's exponent can be determined through the iterative relation

$$1/b = \log \left[\sum_{i=1}^{m} N_i \ (P_i)^{1/b} \right] / \log \ (P_T) \ . \tag{4}$$

This expression will converge as long as the total number of pins in the package P_T is greater than the number of pins on any one active device or discrete package.

For example, we extend the model described by Schmidt[3] to estimate the maximum lead density for circuit cards with package pins on all four sides as shown in Figure 2A. The chip set includes two 120-pin and six 20-pin devices. The total number of package pins is 176, yielding a Rent's Rule exponent of appproximately 0.5. To estimate the maximum number of signal lines crossing any horizontal (or vertical) line drawn across the circuit card, we assume that the maximum number of traveling (crossing) lines will occur at the point where there are $G/2$ gates above and below (or left and right), that is, $y(G/2)$ and $x(G/2)$, respectively. Thus, the maximum number of leads crossing any horizontal line P_h is

$$P_h = a(G/2)^b = (½)^b \ P_T \ . \tag{5}$$

Since the number of leads leading to the package pins located beneath (or above) this line will not affect the wire congestion in the vertical direction, we must reduce the number of leads by a factor of $1 - (P_T'/W)$, where W is the total number of substrate leads, and P_T' is the number of package leads available to the $G/2$ gates accessible without crossing over the imaginary line. Thus, the maximum number of vertically going leads is

$$P_h = (½)^b \ P_T \ (1 - P_T'/W) \ . \tag{6}$$

If we assume an average of 1.25 line segments per device pin, for a total of 450 substrate leads and a Rent's Rule exponent of $b = 0.5$, the maximum number of leads crossing the line in Figure 2A is about 100. Because of the symmetry of the package pins and the device placement, the maximum number of leads crossing any vertical line should be about the same as any horizontal line, with each side of the imaginary line being similar. If the devices were asymmetrically distributed as shown in Figure 2B, the maximum number of leads would depend on which side of the line you were considering. The term P_T' in the correction factor would differ, depending on the gate and package lead distribution. If $P_T' > P_T/2$, the correction factor would be $[(1 - P_T/2)W + (\text{excess package pins})/W]$. Therefore, Equation 6 is correct when $P_T' \leq P_T/2$.

THERMAL ANALYSIS

Finite-element and finite-difference thermal analysis[12] can be used to calculate package and board-level temperatures for various chip configurations and power dis-

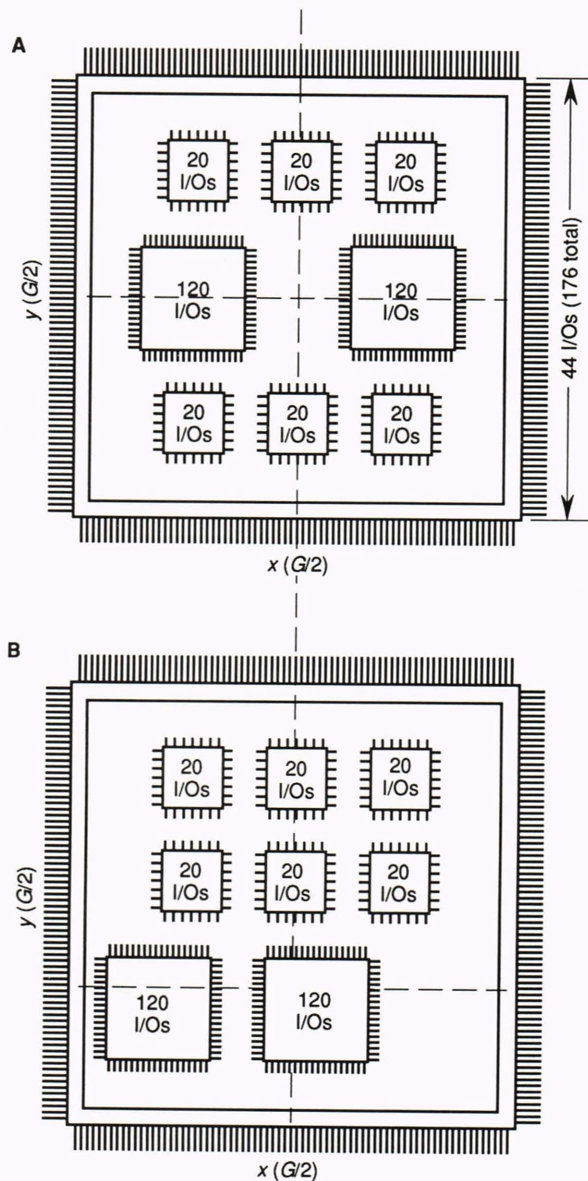

Figure 2. Multichip hybrid module and coordinate lines *x* and *y*, with a Rent's Rule exponent of about 0.5. **A**. Symmetrical. **B**. Asymmetrical. (I/O = input/output.)

sipations. These methods as described previously[4] are particularly useful for estimating junction temperatures of integrated circuits. From these temperatures, we can determine whether additional heat sinking is required. A typical thermal resistance from the die bond to the substrate for a large, leadless chip carrier will be 14 to 16°C/W depending on die size. The junction-to-base thermal resistance of silicon VLSI devices can range from 6 to 9°C/W. Thus, the total junction-to-substrate thermal resistance for heat conduction through solder joints can be as high as 25°C/W. Many of the high input/output VLSI packages contain thermal risers or grid patterns for direct attachment to the substrate. Calculations show that if chip power dissipation exceeds 2 W, direct heat sinking will be required to avoid excessive junction temperatures. With leadless chip carriers, direct attachment of the package bottom (under the die cavity) to the substrate can reduce the overall thermal resistance of the package to 1°C/W (excluding, of course, the chip junction-to-base thermal resistance). Both solder and thermally conductive adhesives have been shown to make effective, low-thermal-resistance heat riser interconnections.[3]

THERMOMECHANICAL ANALYSIS

Many packaging requirements can be satisfied by using multilayer circuit boards with surface-mounted devices. The most significant problem associated with surface-mount technology is the integrity and reliability of the solder joints. Thermally induced mechanical strains in the solder joints resulting from temperature cycling, power cycling, thermal shock, or initial solder reflow can contribute to a significant reduction in joint lifetime. Reactions between the solder and the package or board metallization can also lead to unwanted intermetallic growth and a subsequent loss of service life.[13] (Substrate metallization–solder alloy interactions can be evaluated by using an accelerated thermal aging technique in conjunction with a solder ball shear test as discussed in Ref. 2.)

Finite-element methods can be used to predict the strains in solder joints. The design of the optimal minimum-stress solder joints has been described previously (Ref. 4). Displacements can be estimated for various package and board-level elements under conditions of either power cycling or temperature cycling. These displacements, when used in Coffin–Manson equations[14,15] along with physical parameters of the system, can produce estimates of fatigue lifetime. Analysis indicates that under temperature cycling, long solder pads are preferable to short ones, and the standoff height (package to board) should be about 125 μm. The longer bonding pad allows the solder joint to have low fillet angles[4] while still providing sufficient height for cleaning after reflow. Power-cycling fatigue resistance can be improved by fabricating large-volume joints with lower standoff height (50 μm). The large joint reduces stress concentrations while providing a larger joint cross section to minimize absolute stress density. Large joints (high fillet angles) may lead to bonding pad delamination under temperature cycling.[4]

ELECTRICAL ANALYSIS

The selection of a substrate technology for a particular application of a high-speed device depends on the specific characteristics of the device technology, such as impedance, noise immunity, and rise time. Device technologies especially suitable for moderate- to high-speed applications include: high-speed complementary metal-oxide–semiconductor logic, advanced low-power Schottky transistor–transistor logic (ALSTTL), and emitter-coupled logic. For example, if ALSTTL were selected, a major design concern might be the characteristic impedance of the circuit traces. Low-impedance lines connecting bipolar logic forms can cause significant propagation delays and loss in noise margin. As line lengths and frequencies increase, the problem worsens significantly. Finite-element model-

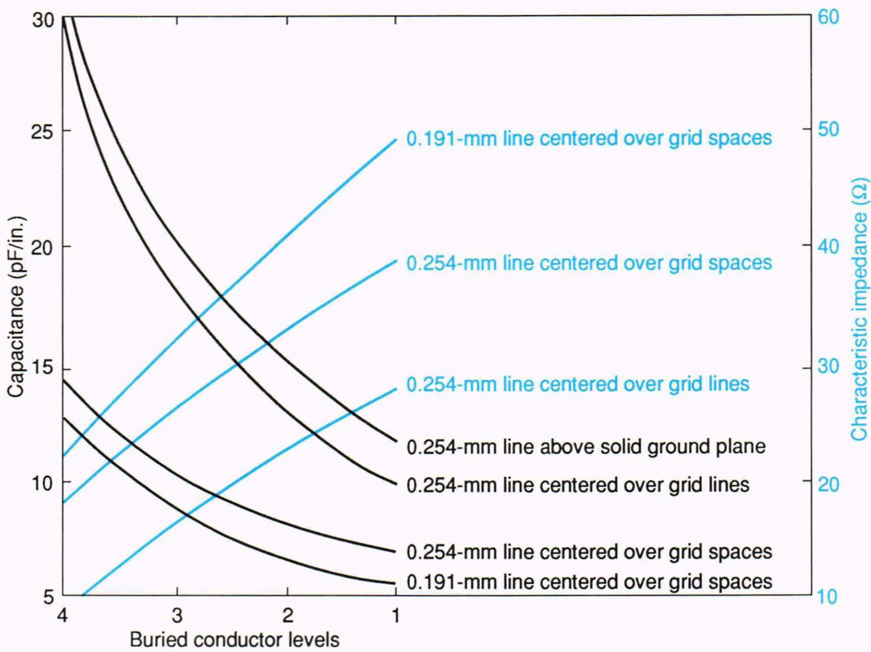

Figure 3. Calculated signal line capacitance and high-frequency impedance (100 MHz) for a multilayer thick-film ceramic circuit board with a gridded ground plane (0.38-mm lines on 1.29-mm centers). A 25.4-μm-thick dielectric (ϵ_r or relative permittivity = 10) between conductors is assumed. The buried conductor level numbers indicate inverse distance from the ground plane (i.e., 4 closest and 1 farthest removed).

ing techniques can be used to develop design guidelines for increasing the characteristic board impedance. These design guidelines[16] focus on three key elements: (1) reducing the overall capacitance of the critical signal lines, (2) providing adequate power supply decoupling of switching transients, and (3) ensuring low-impedance ground returns. Typical results from a finite-element parametric analysis are shown in Figure 3.

At high frequencies, distributed-element modeling is required. For lossless, or nearly lossless, transmission lines, the analysis is handled most conveniently with a simple Simulation Program for Integration Circuit Engineering (SPICE) transmission-line model. Pertinent circuit parameters are contained within the element definition statement, and the transmission line behaves like a simple delay element with a prescribed amount of attenuation. For a "lossy" transmission line, the characteristic impedance is complex.

An example of a useful application of SPICE simulation is shown in Figure 4. Figure 4A represents a situation wherein a 40-MHz shift register on a printed circuit board was used to generate a measured pulse output on a thick-film digital circuit board containing high-speed devices. Some of the clock lines were exceedingly long ($\geq$20 cm), and the capacitance was quite high (10 pF/cm), because of the close proximity of these lines to the underlying ground plane and the high dielectric constant of the material. In addition, the conductor lines were fabricated from a high-resistivity conductor material. Figures 4B and 4C represent the elements applied to create a SPICE model used to simulate Figure 4A. Figure 5 shows the results of the simulation and the actual board measurements. Improved performance (simulation) was achieved by adding more layers of dielectric between the signal line and ground to reduce line capacitance and by using a high-conductivity trace material.

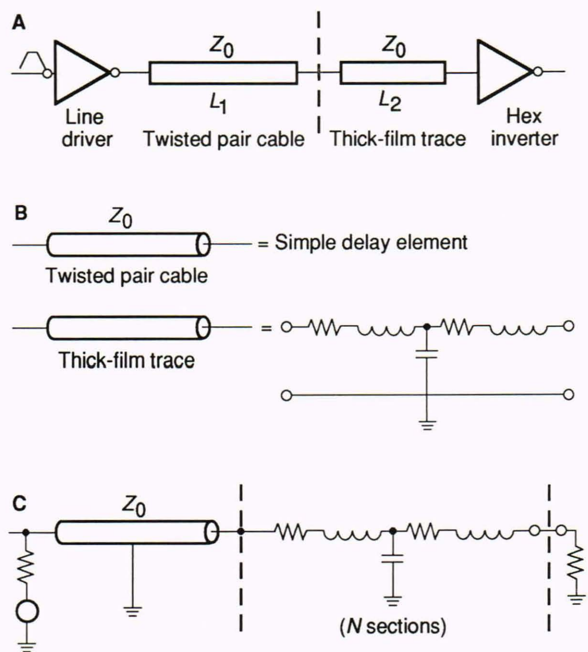

Figure 4. Model of SPICE (Simulation Program for Integration Circuit Engineering) used to simulate high-speed pulse propagation in thick-film circuitry. **A.** Interconnection model for the SPICE simulation. **B.** Circuit models for the major circuit elements (twisted pair, thick-film trace). **C.** SPICE circuit model. (Z_0 = characteristic impedance of signal line; L = length of signal line.)

The results of these improvements, shown in Figure 6, indicated lower pulse distortion; rise times were less than 10 ns, compared with the 25 ns shown in Figure 5.

For rise times in the subnanosecond regime, the device-to-package interconnects may introduce transmission-line

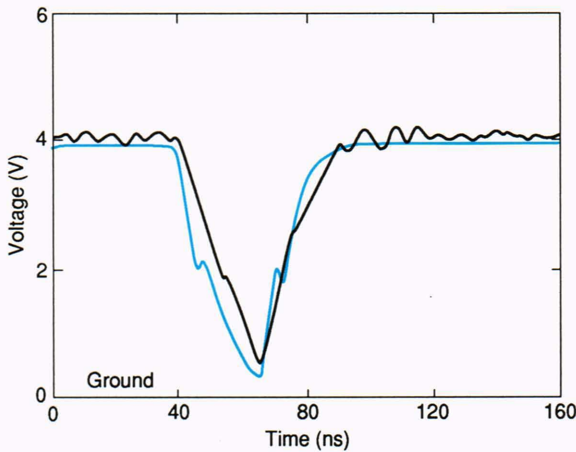

Figure 5. A low-impedance thick-film trace: simulated waveform, colored curve; measured waveform, black curve.

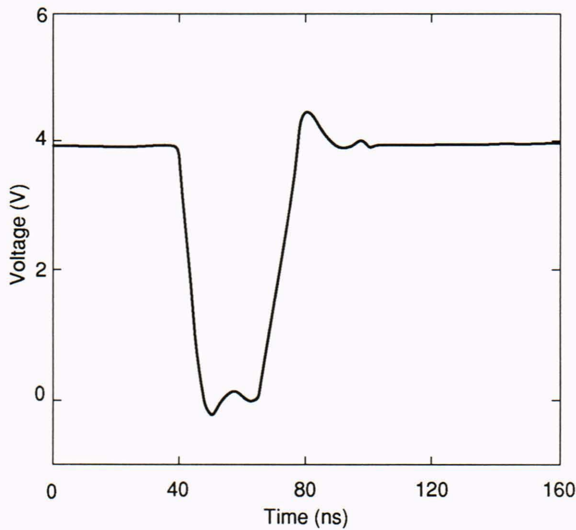

Figure 6. Simulated waveform for a high-impedance, low-resistance, thick-film trace.

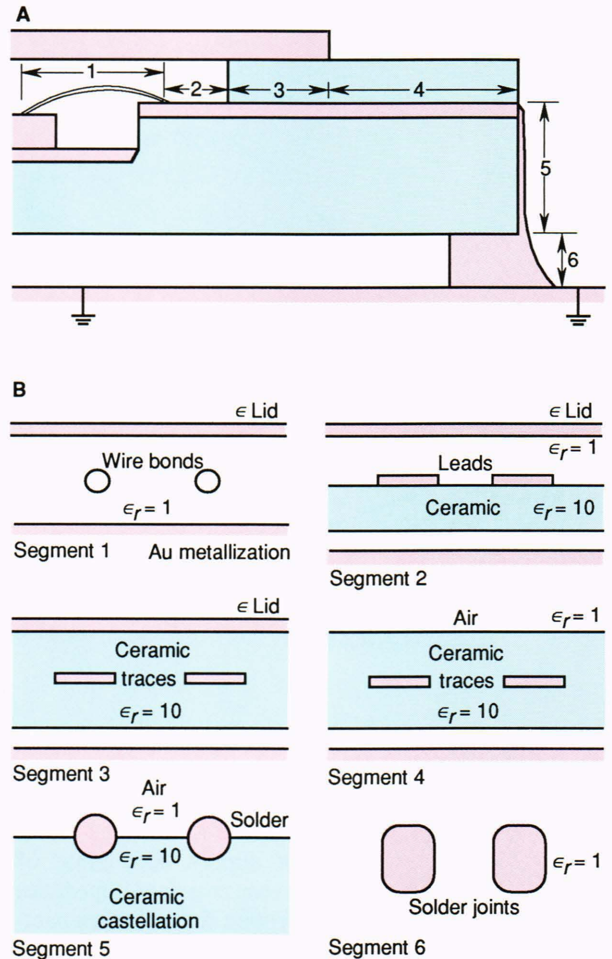

Figure 7. A representative ceramic chip-carrier lead. **A.** Signal path. **B.** Model segments. (ϵ_r = relative permittivity.)

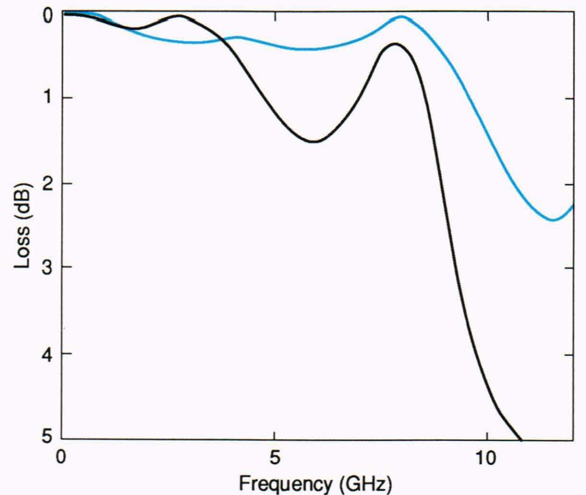

Figure 8. Forward gain plot as a function of frequency for the corner pin of a 68-pin chip carrier with internal wire bonds (black curve) and 50-Ω TAB chip package interconnects (colored curve).

effects that could ultimately limit the useful frequency of a particular package style. For VLSI high-speed applications, modeling the effects of package leads is essential for determining the suitability of various package types. In Figure 7, the signal path for a typical chip-carrier lead is shown schematically. Each of the six segments is represented by an individual transmission-line model. Figure 8 shows the results (forward gain plot) of the analysis on a leadless chip-carrier corner pin terminated in 50 Ω. The plot shows that the −3-dB point is well beyond 9 GHz, although significant degradation occurs just above 4 GHz. Replacing the wire bond with 50-Ω microstrip TAB (two-layer tape, with one layer reserved for a ground plane) produces a significant improvement. Figure 9 shows the performance of a pin grid-array lead as a function of pin termination position. Here, the substrate lead ties into the end of the pin, and the leadless chip carrier and the pin grid array are nearly equal. When the signal trace is connected to the pin near the location where the pin was brazed to the package, however, the performance is quite different. This configuration assumes an unter-

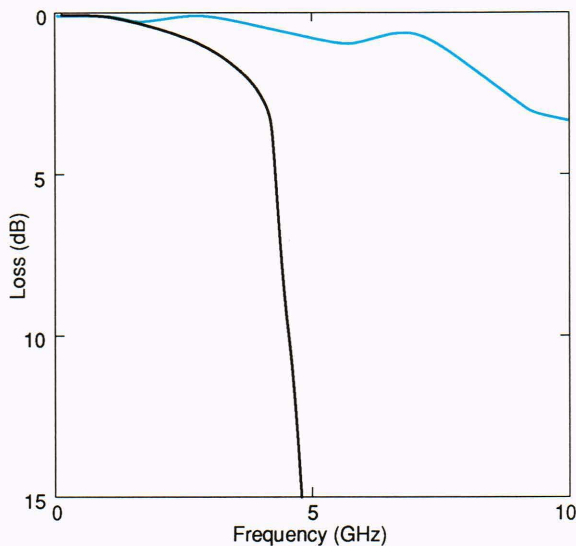

Figure 9. Forward gain plot as a function of frequency for a 68-pin grid array structure, with lead pin terminated at the bottom portion of the pin (colored curve) and lead pin terminated near the package (black curve).

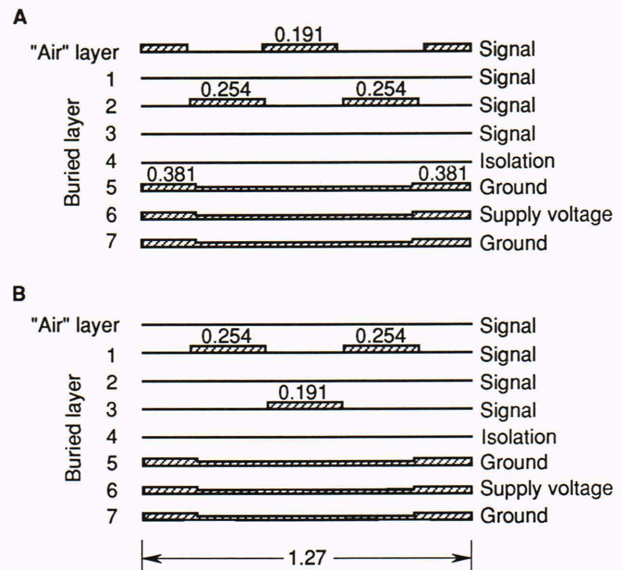

Figure 10. High-density, low-capacitance conductor configuration for multilayer thick-film signal layers with ground and power grid plane. Dimensions are in millimeters. Detailed construction is presented in Ref. 16. **A**. Signal line configuration for north-south-traveling signals. **B**. Signal line configuration for east-west-traveling signals.

minated stub length of 3.8 mm. Performance can be improved by using 50-Ω TAB and by reducing the length of unterminated stubs.

The electronic packaging analysis tools were applied to the design and subsequent thick-film construction of a high-speed radar digital signal processing board,[16] wherein the signal lines were routed over the gridded (power or ground) plane spaces. The power and ground grids were 0.38-mm lines on 1.29-mm centers. All signal lines were of the covered microstrip form. The maximum number of buried levels was prescribed, regardless of the number of conductor levels required for a particular circuit realization. Triple printing of the dielectric (≥ 38-μm total thickness, Dupont 5704) was done at all layers to reduce the capacitance loading. Vias were nominally 0.40 mm square, and via fill artwork was used to ensure reliable layer-to-layer metallization contact. Typical cross-sectional construction is shown in Figure 10.

High-speed lines and long lines were restricted to the top level (air layer) and the first and second buried levels. A minimum line width of 0.19 mm was used on these lines. Critical lines on the air layer had an impedance of at least 45 Ω, which ensured proper device performance even on long lines. Overlapping parallel lines were avoided except for a few short lines. Both gold (Dupont 5715) and platinum/gold (EMCA 6171) conductors were used on the top layer. The higher-resistivity platinum/gold was printed over the gold conductors on all pads for chip-carrier solder attachment.

The dimensions of the rectangular circuit board were 9.15 cm × 16.5 cm, and the connector spanned almost the entire width of the long side. This form factor was selected to minimize the line length for high-speed clock signals going on and off the board. In addition, the wide connector significantly reduced the effect of wire congestion in the center of the substrate. The dielectric constant of the insulating material was approximately 8 instead of the usual 10 associated with typical thick-film dielectrics. All of these factors resulted in an extremely low (for thick film) wiring capacitance. No single trace had a measured capacitance to ground in excess of 35 pF, even for traces as long as 23 cm.

Pulse rise and fall times for the ceramic board clock signals are shown in Figure 11. Here, the input waveform represents the signal at the input of a hex driver on a test set driving a 1.07-m length of twisted pair and a 15-cm ceramic circuit trace (the longest clock line). The output waveform represents the clock signal at the input of the device termination on the ceramic board. The clock pulses shown in this figure indicated no significant degradation in the pulse or rise time.

SUMMARY

Significant improvements in system circuit performance can be achieved by optimizing the system design through the application of effective electronic packaging, modeling, and analysis tools. Devices with high-speed inputs/outputs coming on or off the circuit card should be placed as close to the edge connector as possible to reduce critical line length. Circuit compaction analysis indicates that significant reductions in circuit density can be achieved when circuit-edge connections are made as physically wide as practical and placed on two or more edges of the circuit card. Lower circuit densities mean less crosstalk, higher line impedances, reduced power densities, greater space available for heat risers or sinks, ease of fabrication, and greater ease of cleaning. Control of line impedance is essential for ensuring high-speed performance. Analysis shows that the dual strip-line configuration is ideal for multilayer circuit board applications,

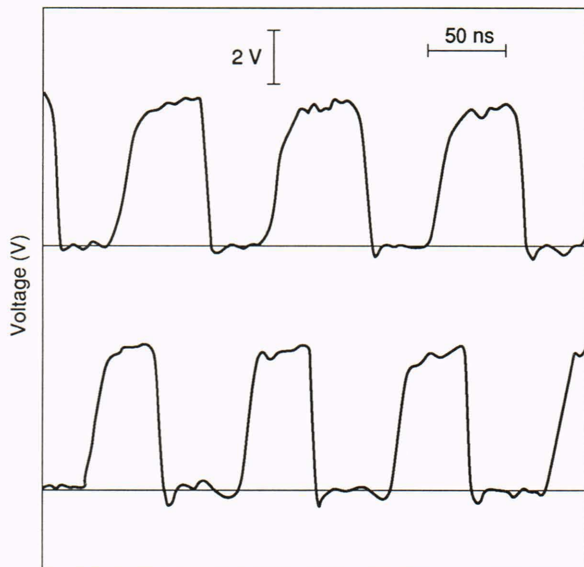

Figure 11. Waveform (top) at the point of a high-speed device driving a twisted pair (1.07 m in length) and a long thick-film trace (15 cm), and the waveform (bottom) at the input of the termination device.

although for thick films, for example, impedance may be too low for certain high-speed device technologies.

A set of design software and computer protocols has been created for the effective package and board-level electrical, thermal, and mechanical modeling of VLSI electronic systems. These models have been validated by extensive simulations and experimental testing. On the basis of the validated models, design guidelines have been established for the creation of large-area, high-speed surface-mount electronic assemblies using very large scale integrated circuits. For example, the design guidelines have been successfully applied to the design and fabrication of a multilayer thick-film board assembly using leadless ceramic chip carriers. This board has been operated at frequencies greater than 80 MHz.

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