

DIGITAL SIGNAL PROCESSING FOR SPACECRAFT ALTIMETERS

In 1975, Seasat-A first provided APL the opportunity to design a spaceborne radar altimeter. Since then, signal-processing electronics technology has developed rapidly. The longer mission goal of the Geosat-A altimeter required improvements to the Seasat-A design. The TOPEX instrument, which has been under development since 1981, incorporates a dual-frequency design. The Laboratory's most recent altimeter program, SALT, makes use of high-performance specialized circuitry to meet design requirements of half the power, mass, and volume of the Geosat-A design.

INTRODUCTION

A radar altimeter is a short-pulse radar that measures the distance between the satellite orbit and a subsatellite point on the ocean surface. This range may be determined to a precision of a few centimeters. If the orbit is known, the altimeter range measurements allow one to determine precisely the shape of the ocean surface along a subtrack line under the satellite. The two primary outputs of an altimeter are the precision height, from which the ocean geoid and surface topography are determined, and the ocean wave-height estimate. The strength of the received signals provides a measure of ocean surface reflectivity, from which wind speed may be inferred.

A radar altimeter comprises two major subsystems: an RF section and a digital signal-processor section. The digital signal-processor section digitizes radar returns and performs all processing necessary to accomplish real-time tracking of the ocean's surface and to derive selected oceanographic data. An altimeter signal processor may be partitioned into functional units, as shown in Figure 1.

The basic function of the waveform sampler is to digitize the in-phase and quadrature video returns and store the time-domain samples for processing by the digital filter bank.

The digital filter bank provides a spectral analysis of the video returns that are digitized by the waveform sampler. Because the radar pulse is frequency-modulated, this spectral information provides range information for tracking and data for analysis of the ocean surface characteristics.

The adaptive tracker is a microcomputer that performs height tracking, automatic gain control, and wave-height estimates, as well as telemetry data formatting, interpretation and execution of commands, and control of the altimeter mode sequencing between acquisition, track, and calibration states.

The synchronizer generates timing waveforms on the basis of a digital countdown from an 80-MHz oscillator. As the result of instructions from the tracker, con-

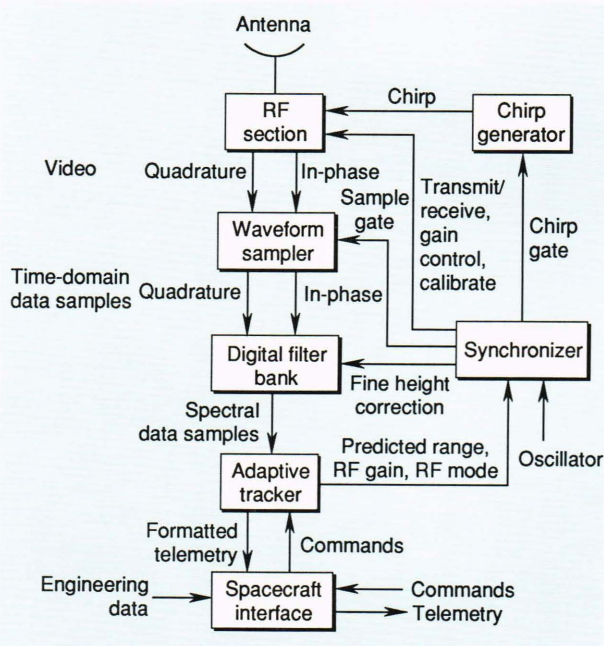


Figure 1. Block diagram of a radar altimeter.

control signals are passed to the RF section. Those signals set up the desired signal conditions and mode switching as a function of the current mode of operation (acquisition, track, or calibration).

The digital chirp generator is designed to drive a single-sideband modulator to produce a linear frequency sweep, known as a chirp pulse. In a single-sideband modulator, the chirp pulse is split into in-phase and quadrature components that are applied to two linear, bipolar modulators.

Digital and some analog interfaces between the radar altimeter and the spacecraft are provided by the spacecraft interface electronics, which also receives commands

for altimeter configuration and sends out telemetry data from the altimeter.

GEOSAT-A

Development of the Geosat-A altimeter began in late 1981. Geosat-A was designed as a stand-alone radar altimeter satellite, tailored to improve geodesy. It was to be built and operated by APL. With the requirement to deliver the altimeter only 18 months after go-ahead, the design borrowed heavily from that of its predecessor, Seasat-A.

The signal-processor design (Fig. 2) was an extension of that of Seasat-A, although several major improvements were made. The transmit pulse length of the altimeter was increased from 3.2 to 102.4 μs to accommodate a more reliable, but lower-power, traveling-wave-tube transmitter design. Because of this change, the dispersive delay line that was used in Seasat-A to generate a 3.2- μs linear frequency-modulation chirp was replaced with a digital design that generated a 102.4- μs chirp pulse. The continuous-wave, acquisition-mode detection circuit was redesigned and moved from the synchronizer to the waveform sampler. The synchronizer was redesigned to accommodate the new, longer-pulse radar timing.

The design of the digital filter bank was not changed, although more highly integrated circuits had become available. The availability of high-speed, parallel, analog-to-digital converters significantly improved the waveform sampler subsystem design. The waveform sampler was completely redesigned to use more reliable, large-scale integrated circuits wherever possible. These parts were used to reduce the integrated circuit count from 85 to only 18, and direct-current power was reduced with no power cycling required.

The longer mission goal of Geosat-A (36 months versus 18 months for Seasat-A) required a careful review of parts reliability and survivability in a radiation environment. The radiation-sensitive 8080 microprocessor from the Seasat-A adaptive tracker design was replaced by the less sensitive 8085 microprocessor. The acquisition, track, and calibration algorithms in the adaptive



Figure 2. The Geosat-A signal processor. The design is an extension of that of Seasat-A, although it incorporates several major improvements.

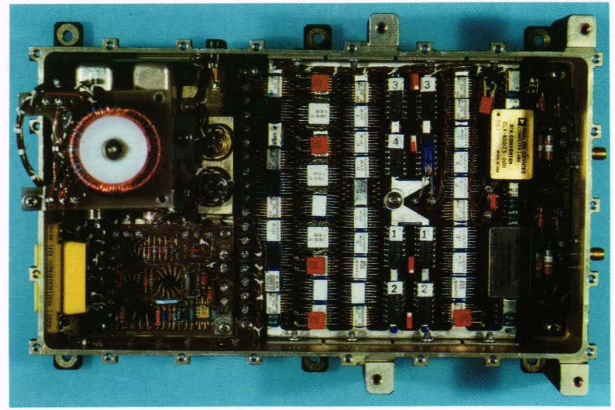


Figure 3. The Geosat-A digital chirp generator with its cover removed. The power-conditioning section is on the left, and the digital-to-analog converters are on the right. In subsequent altimeter designs, the electronics for the entire center section was replaced by a single gate array integrated circuit.

tracker were redesigned on the basis of in-flight Seasat-A experience.

The Geosat-A chirp generator (Fig. 3) provides a fixed linear frequency sweep over a 40-MHz band, from -20 to $+20$ MHz. A parabolic phase-progression modulation, which was developed within the digital section by accumulating the output of a counter at an 80-MHz clock rate, is, in effect, the integration of a linear ramp function. The parabolic phase-progression output is used to address sine and cosine nonvolatile programmable read-only memories that provide the corresponding modulating values. Digital-to-analog conversions of these values yield the in-phase and quadrature signals; these signals drive the single-sideband modulator, which produces the chirp signal.

The Geosat-A radar altimeter has been providing continuous worldwide oceanographic data, including sea-state information and ocean topography, since early 1985.

TOPEX

Since early 1981, a dual-frequency altimeter with a variable pulse repetition rate has been under development for the NASA ocean topography experiment (TOPEX) spacecraft. The TOPEX altimeter interleaves Ku- and C-band pulses (i.e., it transmits one frequency while it receives another) and has a Ku-band pulse repetition frequency of more than 4 kHz. This new altimeter was proposed to satisfy requirements for providing 2-cm precision ranging despite the effects of ionospheric propagation error.

TOPEX Filter Bank

The TOPEX digital filter bank is required to perform a complex 128-point fast Fourier transform (FFT) every 107 μs to support the high pulse repetition rate and two transmit frequencies; in Geosat-A, 980 μs was available to perform a 64-point transform. The processing throughput requirement of the TOPEX filter bank is therefore about 36 times that of the Geosat-A unit. In addition,

the TOPEX filter bank must store and process returns from two radars.

An FFT algorithm implementation proved adequate to meet the processing requirements, but the complexity of the timing and control circuitry for an FFT is costly in total parts. Some early design and breadboard work was done in 1981 and 1982, and work on a TOPEX advanced technology model was initiated in 1983. This design is now being implemented in the TOPEX flight program, which began in 1987. The current TOPEX filter bank contains 184 bipolar integrated circuits and dissipates about 18 W.

Several single-chip digital signal-processing circuits became available between 1983 and 1987, but none was fast enough to meet the TOPEX requirements. Some single-chip FFT circuits that can perform even faster than the current TOPEX filter bank circuitry are now appearing, however.

TOPEX Adaptive Tracker

The TOPEX adaptive tracker must perform more than 5 times the computations that the Geosat-A tracker performs. Reliability requirements still dominate the microprocessor selection process. In addition, the radiation environment, an important constraint in applying digital circuits to space systems, is better understood.

The effect of ionizing radiation is to generate unwanted carriers in semiconductor devices. A single, high-energy charged particle can strike a critical node and leave behind an ionized track, resulting in an erroneous signal, or even a phenomenon called latch-up. Latch-up is a low-impedance, high-current path from the power supply rail to the ground. It may occur when a four-layer-diode parasitic path exists in bulk complementary metal oxide semiconductors. If this path is activated by photocurrents generated by ionizing radiation, latch-up occurs. The accumulation of radiation can permanently alter the electrical properties of the semiconductors.

The final choice for TOPEX was between a microprocessor implementation of the military standard 1750A architecture and the Intel military certified M80186. The M80186 was selected on the basis of proven reliability, adequate radiation tolerance, and availability of superior software development tools.

TOPEX Tracker Software

The TOPEX tracker software controls nearly all aspects of the altimeter operation. The software interprets and executes commands, formats and synchronizes science and engineering telemetry streams, and implements numerous test and calibration modes. Using the radar returns, the software calculates error measurements and then adjusts both the tracker height and receiver gain settings. These adjustments are made separately to both the Ku- and C-band channels.

During normal operational modes, the adaptive tracker has about 30 ms to calculate the height errors and make corrections to the heights and automatic gain control values. During this 30 ms, the tracker must also service interrupts from the synchronizer, load commands, and format telemetry. Because of this processing load, an efficient method of coordinating tasks is essential.

Further complicating the software design is the in-flight reprogramming requirement. The design is required to be able to replace all of the flight software. Because of the size of the system and the uncertainty in the uplink bandwidth, the system is designed to allow individual software modules to be uploaded. Also, because of the length of the mission and the reprogramming ability, the software must be maintainable and fully documented.

TOPEX Synchronizer

The synchronizer, which must support dual frequencies, variable pulse repetition frequencies, and high-speed rate compensation calculations, is more than 3 times as complex as that of Geosat-A. The advancement from Geosat-A to TOPEX involved dramatic changes to the synchronizer, not only in concept, but also in circuit technology. The complexity of the synchronizer grew significantly as a result of having to provide control signals for a dual-frequency radar altimeter with a variable pulse repetition frequency. The synchronizer needed to generate control signals that would accommodate the interleaving of Ku- and C-band transmitted pulses. The result is that a burst of 38 Ku-band and 10 C-band pulses can be transmitted and received in about 8 ms.

To a great extent, the synchronizer is under tracker control. The tracker permits the variation of both the pulse repetition frequency and the total number of Ku- and C-band pulses in a burst. It also governs the state of mode bits within the synchronizer, thereby allowing for the selection of Ku-band operation at 4 or 1 kHz and limiting the bandwidth of the C-band channel from 320 to 100 MHz. Other mode bits are used to force the overlapping of the transmit and receive cycles for instrument calibration and to inhibit key output control signals.

SALT

The special-purpose inexpensive satellite radar altimeter (SALT) is APL's most recent altimeter program. The SALT design was begun in late 1988 and will use three gate arrays: two high-speed arrays that were used previously on TOPEX and a lower-speed array that includes all of the remaining specialized signal-processor logic. In addition, the SALT electronics includes an ADSP-2100 single-chip, programmable, digital signal processor (Analog Devices); an 80C86RH radiation-hardened microprocessor; and very high speed integrated circuit memory.

The SALT signal-processor electronics is packaged on only two multilayer printed circuit boards. One board includes all the digital logic: the synchronizer gate array, the low-speed gate array, the ADSP-2100-based digital filter bank, and the 80C86RH-based adaptive tracker. The second board includes all the analog logic: the in-phase and quadrature analog-to-digital converters for digitizing the receiver output, the analog telemetry temperature- and voltage-conditioning amplifiers, the analog telemetry commutator, and the housekeeping analog-to-digital converter.

The SALT signal processor is required to be identical in function to that of Geosat-A, but its implementation

is to use only half the power, mass, and volume of the Geosat-A design. These demanding power, weight, and packaging goals mean that the SALT digital filter bank must be a completely new design. Fortunately, one of the many new programmable, digital signal-processor chips, the ADSP-2100, meets the reliability, radiation, and processing requirements of SALT.

Using a programmable processor with its highly regular structure reduces the entire filter bank design to about 20 integrated circuits. Goals of 2.5 W and 328 cm³ have been set for the power dissipation and physical size of the filter bank, respectively.

The ADSP-2100 runs at a clock rate of 20 MHz, which corresponds to an instruction rate of 5 MHz. The ADSP-2100 has several architectural features that make it particularly suitable for the filter bank function. Separate program and data buses allow the processor to fetch a coefficient from programmable read-only memory and a data sample from random-access memory at the same time that an instruction is executed out of an on-chip instruction cache memory. (Cache memory is memory that is transparent to the user. It improves the system performance by anticipating the likely reuse of stored data and instructions.) This parallelism speeds up the execution rate of the FFT considerably.

The independent data-address generators allow the ADSP-2100 to manipulate data arrays much more efficiently than a general-purpose central processing unit allows. The basic real-time requirement for the SALT digital filter bank is that its processing cycle must be completed in 980 μ s (one radar pulse repetition interval).

In addition to the ADSP-2100 chip itself, the SALT filter bank hardware design includes 1024 words of 24-bit instruction memory; 8192 words of 16-bit data memory; two 6-bit, flash, analog-to-digital converters; and a 512-byte-deep, first-in/first-out output buffer.

A significant feature of the SALT signal-processor design is the melding of a digital signal processor and a microprocessor within a single bus structure.

By maintaining the simpler Geosat-A type spacecraft interface and using the more compact TOPEX telemetry data acquisition design, the SALT spacecraft interface electronics is implemented on a single 20.3 \times 20.3 cm multilayer board, and its power dissipation is about 3 W.

GATE ARRAYS

Semi-custom, application-specific integrated circuits, or gate arrays, provide a way to reduce the volume, weight, and power requirements of an altimeter while dramatically improving its reliability.

The synchronizer and digital chirp generator subsystems within the altimeter contain circuits that operate at a maximum frequency of 80 MHz. Existing discrete integrated circuit technologies are either too slow to produce reliable operation at high frequencies or require too much power. To achieve the necessary operating frequency at lower power, the high-speed sections of each subsystem have been designed into gate arrays. These large-scale integration devices contain uniform arrays of logic gates with capacities ranging from 1000 to more

than 50,000 gates. The arrays are initially manufactured with an array of unconnected transistors. Manufacturers provide design engineers with a library of macros (or building blocks) from which they can construct their schematics by using a computer-aided engineering workstation. The macros are proprietary functional blocks (e.g., logic gates, adders, counters).

Following the manufacturer's specific design guidelines (design rules), the design engineer selects and interconnects the building blocks to form a complete system that implements a desired function. He or she enters and simulates the design on an engineering workstation, such as Mentor, similar to what would be done for a conventional design. After running a simulation of the design on the workstation by using manufacturer-supplied modeling information, the design engineer submits the circuit database to the manufacturer. The manufacturer then re-simulates the design and checks for compliance with all of the design rules.

If the simulation results agree with the design engineer's results, the integrated circuit is laid out; that is, the manufacturer generates the interconnection layers that are needed to implement the desired circuit. This task is performed on a layout workstation, resulting in the creation of a back-annotation file that is sent to the design engineer. The file contains propagation delay and timing information, which allows for a more accurate simulation (previously done with statistical modeling data) that more closely reflects how the actual device will perform.

The design engineer simulates the design once again and verifies proper circuit operation. After successful completion of all simulations and a directive from the design engineer, the manufacturer develops and delivers prototype parts. Once the design engineer tests and verifies the proper operation of the prototypes, the manufacturer produces the final parts in compliance with the quality-control requirements provided by the design engineer in the device specification.

Both the TOPEX and SALT designs make use of gate array devices. One of the arrays (Fig. 4) is designed to perform the high-speed operations of the synchronizer, making it possible to fit the TOPEX synchronizer on three 10.2 \times 15.2 cm boards. Including the gate array, the synchronizer consists of 135 integrated circuits and dissipates about 6.5 W. Nearly three times the circuit complexity of the Geosat-A synchronizer is packed onto three multilayer printed circuit boards requiring about one-third less area and an increase in power consumption of only about 0.5 W.

A second gate array implements the entire digital chirp generator function, except for the digital-to-analog converters. An improvement in the TOPEX digital chirp generator is the provision for selectable bandwidths, which begin at 40 MHz and decrease by factors of 2, down to 625 kHz, yielding seven selections (40, 20, 10, 5, 2.5, and 1.25 MHz, and 625 kHz). Selectable bandwidths allow for variable-resolution tracking, thus eliminating the need for a continuous-wave acquisition operating mode (as was implemented in Geosat-A). The variable-bandwidth selection is implemented in the TOPEX

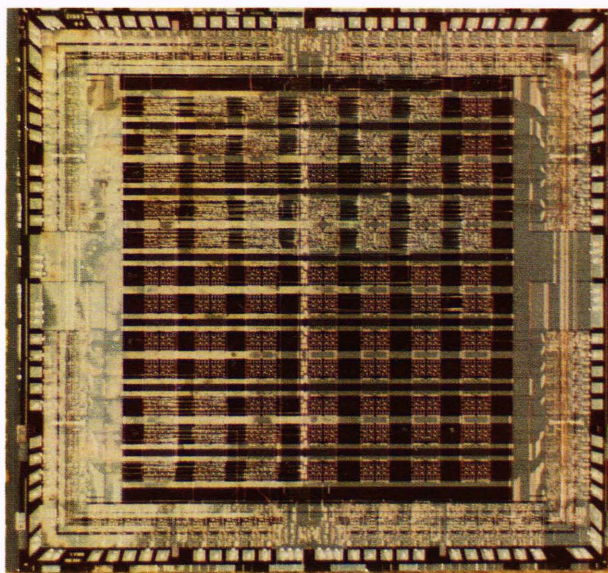


Figure 4. A single emitter-coupled-logic integrated circuit. This type of circuit makes up much of the high-speed digital circuitry needed to implement the synchronizer for a radar altimeter. By carefully observing the aluminum metallization tracks, one can see that only about 40% of the 1300 two-input gate equivalents are used.

chirp generator by controlling the integration rate and the starting value of the ramp.

The digital chirp generator array, consisting of 3500 gates, permits the entire digital portion to reside on a single chip, including the nonvolatile sine/cosine memories, which are implemented as Boolean expressions through combinational logic functions (instead of a canonical read-only memory configuration). The only components external to the gate array are the digital-to-analog converters, a 5-V regulator integrated circuit, and a few discrete components. The power dissipation is about 7 W. The size of the chirp generator has been decreased from a $29.8 \times 19.1 \times 8.9$ cm package (Geosat-A) to a $16.5 \times 10.2 \times 5.1$ cm package, an 83% reduction in volume (from 5066 to 858 cm^3). Figure 5 is a photograph of the TOPEX and SALT digital chirp generator.

In the SALT, gate arrays absorb a major portion of the digital implementation. A third array is incorporated in addition to the arrays used for the digital chirp generator and the synchronizer. It allows for the integration of the discrete TOPEX synchronizer logic functions onto a single chip, replacing more than 100 integrated circuits with a single device.

The SALT gate array implements the synchronization, acquisition, calibration, control, and timing in 4000 two-input gate equivalents. In addition, the design is improved because the interface logic and control logic are in the same location. The major change is a parallel address/data bus and its control to allow the tracker to communicate with the remaining sections of the altimeter.

The design is pin-limited; we ran out of package pins before we ran out of gates in the array. The array re-

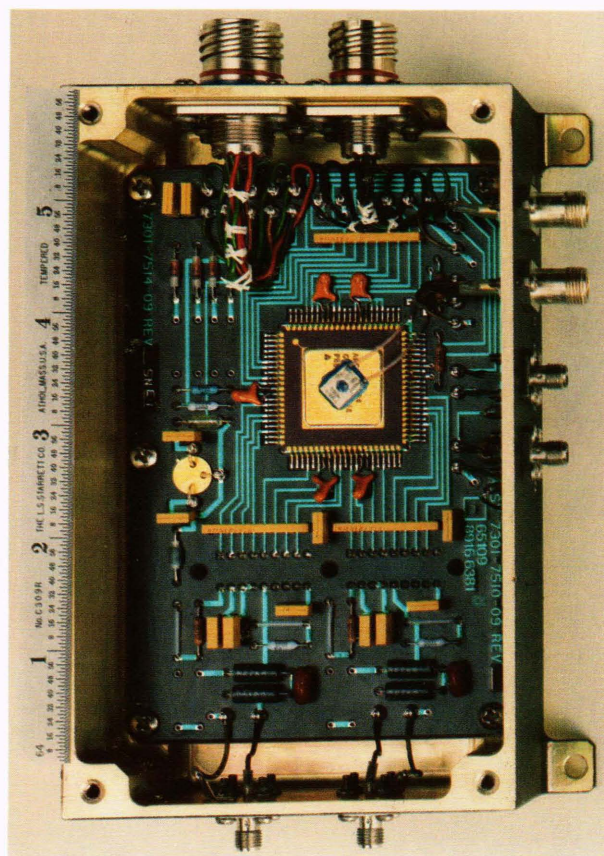


Figure 5. The digital chirp generator for TOPEX and SALT. The size and power dissipation of this generator are significantly reduced compared with those of Geosat-A. The reductions were accomplished primarily by using an emitter-coupled-logic gate array to implement nearly all of the digital logic functions. About 92% of the 3500 two-input gate equivalents are used.

quires a 196-pin integrated circuit package and occupies 4.8×4.8 cm, dissipates 0.4 W, and weighs less than 28 g.

The only disadvantage of a gate array is the need to finalize all design interfaces that affect the array before manufacture. Once production has begun, it cannot be changed without significant additional cost.

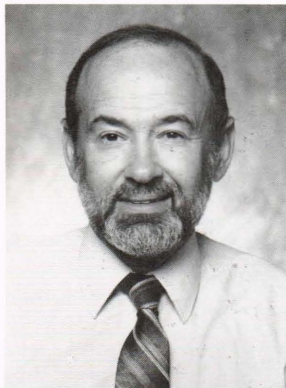
Future plans include the implementation of automatic test-pattern generation and in-house gate array manufacture. Although in-house arrays for prototyping will not be radiation hardened, the delivery time will approach two weeks rather than two months.

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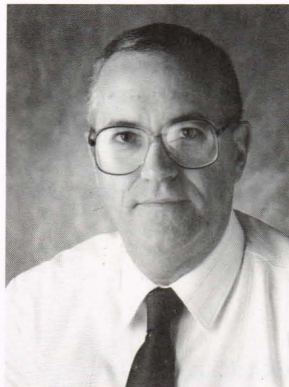
ACKNOWLEDGMENTS—The authors would like to acknowledge the contribution of Joe Phipps in the design of the Seasat-A high-speed waveform sampler. Others who participated in the design efforts were Ronald K. Burek, who designed the Seasat-A synchronizer; Deanna R. Ravenscraft, who designed the synchronizer gate array; B. Joy Hook, who designed the SALT tracker software; Jon C. Barnett, who designed the SALT interface; George J. Theodorakos, who designed the TOPEX interface; Susan C. Lee, who wrote the TOPEX software requirements document; and D. Gilbert Lee, Jr., who designed the first gate array chirp generator. This work was supported by SPAWAR and NASA.

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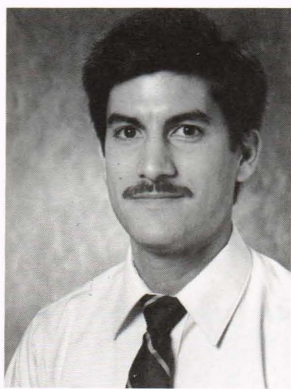
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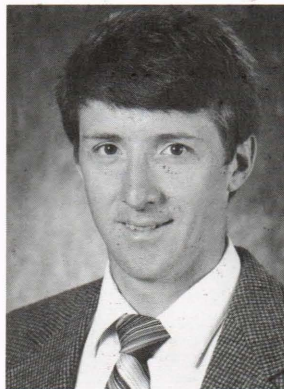
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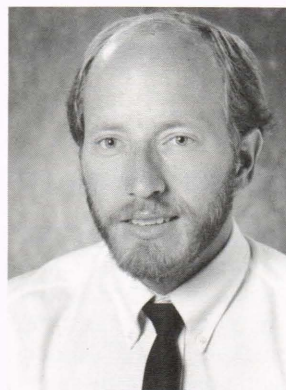


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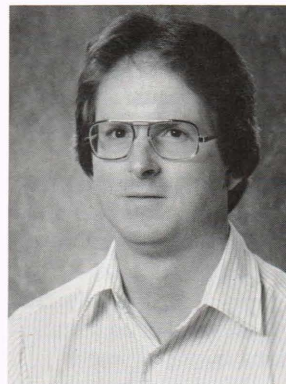


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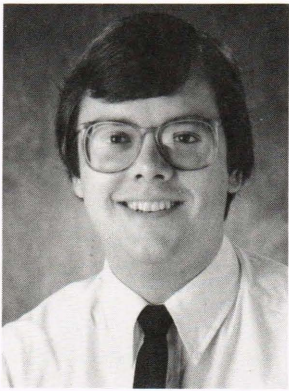
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portion of the digital chirp generator for TOPEX and SALT.

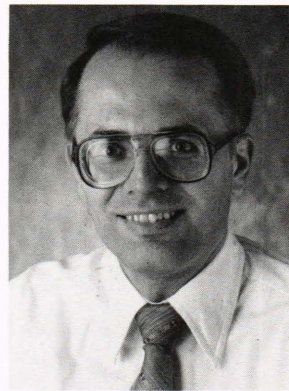


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