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THERMAL AND THERMOMECHANICAL ANALYSIS AND TESTING OF ELECTRONIC PACKAGING SYSTEMS

A comprehensive thermal and mechanical modeling and experimentation program in advanced packaging has led to the systematic thermomechanical analysis of very large scale integrated device packages, board-level structures, and surface-mounted electronic systems. Model validation and analytical results have been correlated with data from extensive experimental testing, and new techniques have been developed for the production of high-reliability, controlled-geometry solder joints for large leadless ceramic chip carriers.

INTRODUCTION

The successful implementation of very large scale integrated (VLSI) and very high speed integrated circuit (VHSIC) devices for surface-mounted applications will require the electronic packaging engineer to design packages, circuit boards, and systems that can accommodate the increased power dissipation associated with these complex, high-speed devices. Computer-assisted thermal modeling techniques can be used to evaluate design concepts and to predict junction temperatures under operational conditions. The mechanical integrity and fatigue life of soldered leads can be determined by thermomechanical analysis and testing of surface-mounted package and component interconnections.

APL's Microelectronics Group has been actively engaged in a comprehensive development study of advanced electronic packaging. The purpose of the study is to investigate computer-aided engineering methods and experimental testing procedures for the thermal and thermomechanical analysis of VLSI packages and surface-mounted microcircuit assemblies, including

1. The finite-element thermal analysis of leadless chip carrier packages and microcircuit assemblies,
2. The theoretical and experimental reliability assessment of leadless chip carrier soldered interconnections operating in either a power- or a temperature-cycled environment,
3. The evaluation of the finite-element method as a viable computer-aided engineering approach to both thermal and thermomechanical design.

This article discusses details of the technical aspects of the finite-element modeling and experimental testing of large leadless ceramic chip carriers under various operational scenarios.

THERMAL ANALYSIS OF SURFACE-MOUNTED PACKAGES AND COMPONENTS

The thermal design and analysis of integrated circuit assemblies is one of the most dynamic areas of technical investigation in the electronics industry today. The reliability of both microelectronic devices and their interconnections is critically dependent on operating temperatures. Thermal design thus is a premanufacturing step that is necessary to ensure adequate thermal management and long-term reliability. The finite-element method is the most widely used computer-aided engineering tool for both thermal and thermal-stress analysis. The availability of computerized finite-element preprocessors and analysis codes (e.g., PATRAN (finite-element preprocessor), NASTRAN (finite-element analysis code)) for model construction, automatic data generation, and the subsequent analysis of complex thermal models provides the rapid turnaround required for the evaluation of interactive design.

Modeling a complex hybrid microcircuit assembly for subsequent thermal analysis using finite-element methods is accomplished most economically by dividing the system into several smaller ones. Reducing surface-mounted components and packages to equivalent, lumped, heat-transfer elements by individually modeling each component (using a detailed finite-element model) can be a useful approach for transforming large complex circuit boards into relatively simple thermal-resistance networks. First, the procedure requires the numerical estimation of lumped thermal circuit parameters (e.g., thermal resistors) for individual surface-mounted components and packages. Then the substrate can be divided into finite elements, each bounded by nodal points to which the previously estimated component and package thermal resistors can be thermally connected.

The thermal analysis approach discussed here is shown schematically in Fig. 1. Each thermal path from the device junction to the ambient is represented by a series of thermal resistors, and each thermal resistance can be estimated from individual detailed finite-element models for the die, chip carrier, solder joints, etc. The device junction temperature can be estimated from the following relationship:

$$T_j = T_{amb} + (R_{tot})Q ,$$

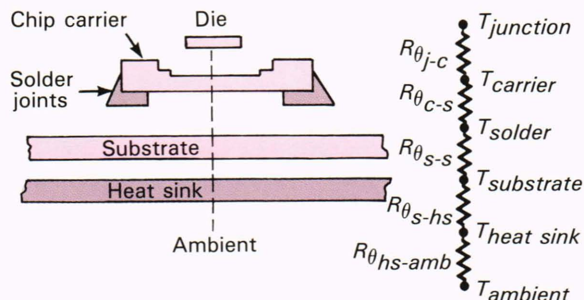

Figure 1—A typical thermal-resistance path from the junction to the ambient for a surface-mounted hybrid assembly.

where

T_j = junction temperature,
T_{amb} = ambient temperature,
R_{tot} = sum of the individual thermal resistances,
Q = power dissipated by the device.

THERMOMECHANICAL ANALYSIS AND TESTING OF LEADLESS CHIP CARRIER SOLDER JOINTS

Low-cycle fatigue life in surface-mounted solder interconnections has been observed primarily during extreme temperature- or power-cycle testing when there is a large mismatch in the temperature coefficients of expansion between the chip carrier and the substrate.[1] Recently, the cyclic strains induced by the differential thermal expansion that results from the power cycling of chip carriers and substrates with matched temperature coefficients of expansion has led to speculation concerning their reliability.[2] In addition, the significant stress on thick-film solder pads that results from the large, differential thermal expansion between the solder and the ceramic during thermal cycling has been cited as a significant contributor to the delamination of thick-film bonding pads from the underlying dielectric layer.[3]

THERMOMECHANICAL ANALYSIS OF TEMPERATURE-CYCLED SOLDER JOINTS

Bond interfaces for temperature-cycled solder joints on ceramic substrates can experience large strains because of the large difference between the temperature coefficients of expansion of the solder and of the ceramic. A finite-element method analysis was conducted to evaluate the magnitude of thermally induced stresses for various solder-joint configurations.

Figure 2 is an example of one of the finite-element method representations for a typical chip carrier solder joint. In order to account for the difference in the temperature coefficients of expansion of the solder joint and the ceramic, it was necessary to include the constraining ceramic of the substrate and chip carrier in the model. Calculations were performed to estimate tensile stresses at the thick-film bonding-pad interface when cooling the solder joint from +125 to −55°C. The stresses are believed to be the major cause of bonding-pad delamination. Various solder-joint configurations were tested to evaluate the effect of geometry on bonding-pad stresses (see Fig. 3).

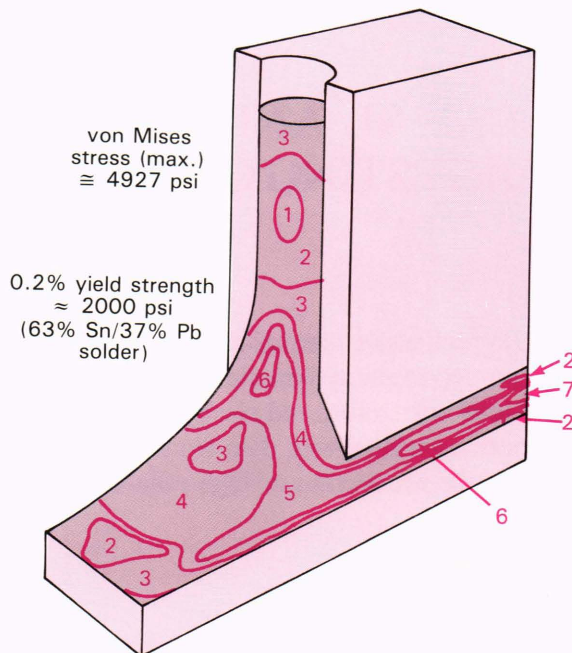

Figure 2—A finite-element model of a leadless ceramic chip carrier solder joint for a temperature-cycling stress calculation. Contours with numbers ≤ 2 indicate regions where the von Mises stress is greater than the 0.2 percent yield strength of solder.

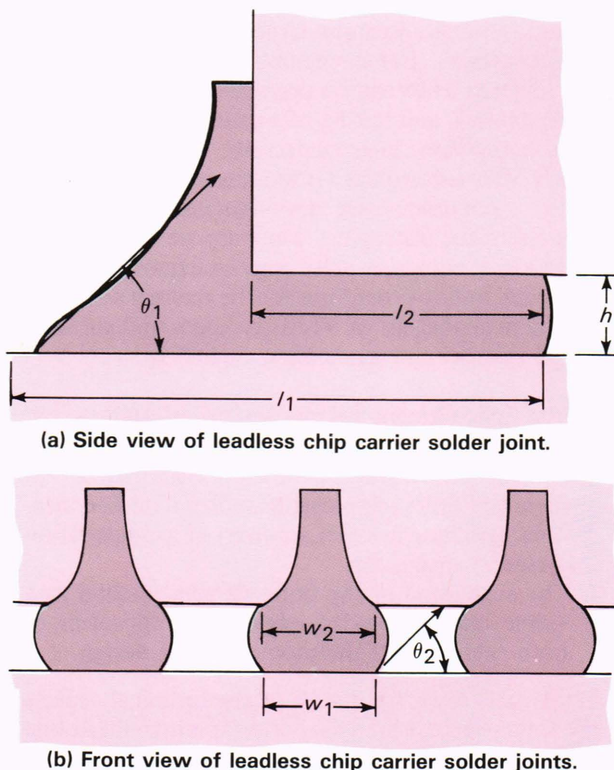

Figure 3—Geometrical design parameters for temperature-cycled solder joints.

The analysis led to the following conclusions regarding the effects of geometry on pad delineation stresses:

1. Increasing the wetting angle, θ_1 (Fig. 3), increases pad lifting;
2. Low standoff height h; $\theta_2 < 90°$; and large l, length, and w_1, width, increase the shear stress at the bonding-pad interface.

Tests of solder joints in shear, performed by Reimer and Russell,[3] have indicated that the joints on thick-film materials have a substantially higher fracture strength when loaded in shear than when loaded in tension, indicating that the primary consideration for designing a solder joint that is resistant to pad lift failure under temperature cycling is the reduction of the tensile stress component at the solder-bond interface. This can be accomplished simply by increasing either the wetting angle of the solder fillet, θ_1, or decreasing h.

Analyses of this kind for other surface-mounted packages and components will offer methods for fabricating reliable solder joints and will provide additional guidelines for inspecting the integrity of solder joints for high-reliability applications.

THERMOMECHANICAL ANALYSIS OF POWER-CYCLED CHIP CARRIERS

Leadless chip carrier devices dissipating significant amounts of power and operating in a cyclic power-on/power-off mode have exhibited fatigue cracking at soldered interconnections, resulting in electrical open circuits. A number of models of solder fatigue developed recently are based on the Coffin-Manson fatigue equation.[4] The semiempirical equation is given by the relationship

$$\Delta\gamma_p = CN_f^{-\beta} ,$$

where

$\Delta\gamma_p$ = plastic shear strain,
N_f = number of cycles to failure,
C, β = empirical constants to be determined from a nonlinear regression analysis of the experimental data.

For tin-lead solders, C is approximately 0.65 and β is approximately 2.0. The plastic shear strain, γ_p (assuming cylindrical solder joints and small displacements) is usually expressed as

$$\Delta\gamma_p = \delta l/h ,$$

where

δl = differential thermal expansion of the chip carrier and substrate,
h = height of the solder joint.

In order to use the Coffin-Manson equation to estimate fatigue life, a way to estimate the differential thermal expansion is required. Thermomechanical analysis using finite-element techniques provides a practical way to do this for power-cycled chip carrier assemblies.

The analysis requires two steps:

1. A thermal analysis to determine temperatures over the entire domain of interest (the chip carrier and substrate),
2. The subsequent evaluation of stresses resulting from the temperature distribution.

The finite-element-methods model used in this study to estimate the differential thermal expansion is similar to the one shown in Fig. 4.

The maximum differential expansion (assuming complete solder relations) for a 68-pin chip carrier was estimated to be about 2.8 micrometers for a chip dissipating 10 watts. Using the assumptions of cylindrical joint geometries and no stress concentrations, this is equivalent to a shear strain of 5 to 6 percent for solder joints with standoff heights of approximately 2 mils and to less than 1 percent for standoffs greater than 2 mils. The Coffin-Manson equation predicts fatigue life in excess of 1000 cycles when shear strains are maintained at less than 1 percent for tin-lead solders.

POWER CYCLING EXPERIMENTS

Effect of Joint Geometry

An initial power-cycling study was conducted to determine the sensitivity of joint design to the number of

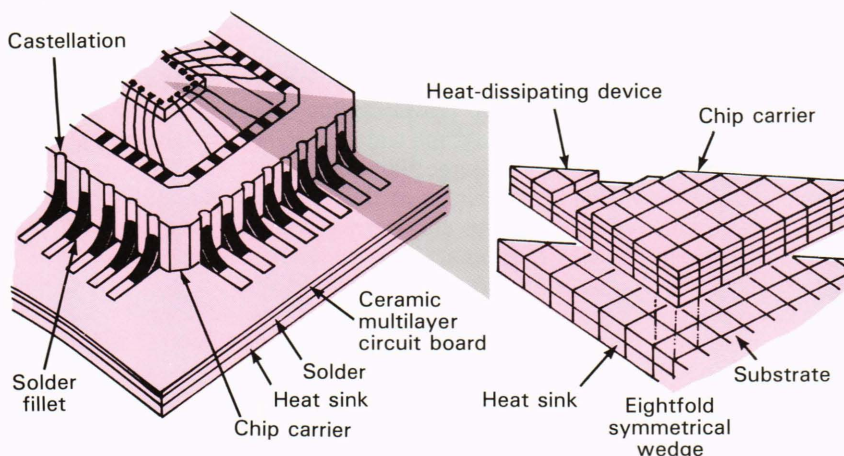

Figure 4—A finite-element thermal-analysis model for a leadless ceramic chip carrier.

cycles to failure. Eight chip carriers with four different solder-joint geometries were used. The parameters to be varied were standoff height (15 mils versus 2 mils) and fillet size (large versus small). Power cycling was simulated by attaching a 10-watt chip resistor in the chip carrier die cavity. The solder joints were daisy chained together to monitor changes in the electrical resistance that might occur as a result of a mechanical failure. The solder-joint temperatures remained at about 35°C throughout the test, and the cycle frequency was approximately 144 cycles per day.

After 5000 power cycles, only one of the eight samples had exhibited significant fatigue cracking that resulted in an electrical open circuit. Then, all the samples were removed and examined closely using scanning electron microscopy. The solder joints with low standoffs and large fillets exhibited superior fatigue resistance. Joints with high standoffs and small fillets exhibited signs of severe fatigue wear. These results contradicted estimates of fatigue life obtained from the Coffin-Manson equation, which had indicated a longer fatigue life for solder joints with high standoffs than for those with low standoffs.

These preliminary results indicate that the shape of the solder joint may be a primary rather than a secondary factor in determining useful service life for power-cycled chip carrier assemblies. Additional finite-element model analyses indicated that the effects of stress relaxation and stress concentrations can vary significantly with solder-joint shape. In addition, substrate and chip carrier warpage effects can be influenced significantly by the geometry of the solder joint. The effects can result in large increases in the tensile-strain component at the expense of, or in addition to, pure shear strain. Tensile strains enhance the harmful, time-dependent relaxation processes, thereby sharply reducing the useful service life of the joint.

Effect of Solder Temperature and Cycle Frequency

Additional power-cycling studies were undertaken to observe the effects of frequency and temperature on N_f. The solder-joint geometry was held uniform for 16 chip carrier specimens. Two temperature levels, 40 and 65°C, and two frequency levels, 96 and 288 cycles per day, were used. Power-dissipation levels for all the samples were varied. The subsequent strain estimates were based on finite-element thermomechanical calculations. In Fig. 5, N_f is plotted versus the strain range estimated by the finite-element method for all the samples. The results indicate that both the solder temperature and the power-cycling frequency are significant factors in the fatigue life of solder joints. Predictably, the effect of temperature at the higher frequency was less pronounced than at the lower frequency. This can be explained by considering the effects of creep and other stress-relaxation phenomena at solder temperatures above room temperature. At elevated temperatures, the time-dependent stress-relaxation processes are enhanced. As the dwell time is increased, additional stress relaxation can occur, resulting in a reduction in the ultimate fatigue life.

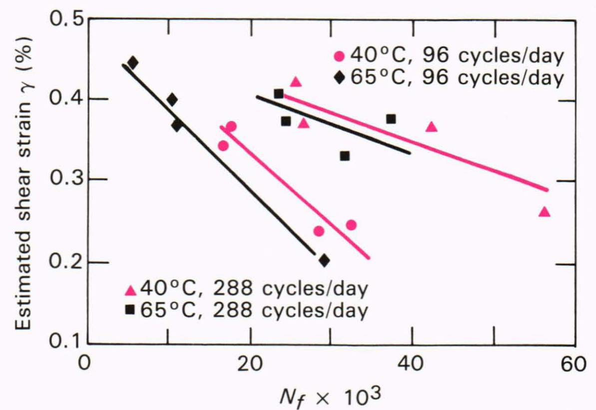

Figure 5—Results of power-cycling test to study the effect of temperature and cycle frequency on fatigue life.

DISCUSSION

Temperature-Cycling Effects on Solder/Thick-Film Interfaces

Analyses of chip-carrier solder-joint geometries suggest that long solder pads are preferable to short ones and that slightly elevated standoffs (approximately 5 mils) are preferable to high standoffs (more than 10 mils). The longer bonding pad permits solder joints to be fabricated with a low fillet angle while still allowing a joint with enough height to facilitate removal of flux after soldering. Also, as indicated in power-cycling experiments, increasing the fillet volume while keeping the solder standoffs relatively low increases the resistance of the joint to power-cycling fatigue.

Power-Cycling Effects on Chip Carrier Solder Joints

The results for both power-cycling studies and finite-element model thermal-stress analyses indicate that relatively large power dissipations are required to produce enough strain on soldered chip carrier leads to cause failure when they are mounted on matched thermal-expansion substrate materials. The reason for the relatively good power-cycling fatigue properties of the leadless chip carrier package is the rigid, cooler sidewalls that constrain the chip carrier from expanding, thus concentrating most of the strain in the ceramic package rather than in the solder joints.

The experiment to investigate the effect of solder-joint geometry on power-cycling fatigue resistance indicates that increased life can be attained by fabricating solder joints with large fillets and small standoffs. Studies of the finite-element method indicate that large fillet geometries reduce chip-carrier/substrate warpage and thus help to eliminate harmful tensile-strain components. The large fillet also helps to reduce stress concentrations while providing a larger cross-sectional area within the joint. Both factors tend to improve the fracture toughness of the joint.

Experimental results also dramatically demonstrate the effects of temperature and cycle frequency on the fatigue life of soldered interconnections. The frequency de-

pendence observed in the studies can be minimized by eliminating harmful tensile-strain components. Reducing tensile strain is probably the most effective way to reduce the effects of both temperature and frequency in low-cycle solder fatigue. Experimental studies on tin-lead solder alloys indicate that harmful stress relaxation can occur much more rapidly during tensile strain hold than during comprehensive strain hold.

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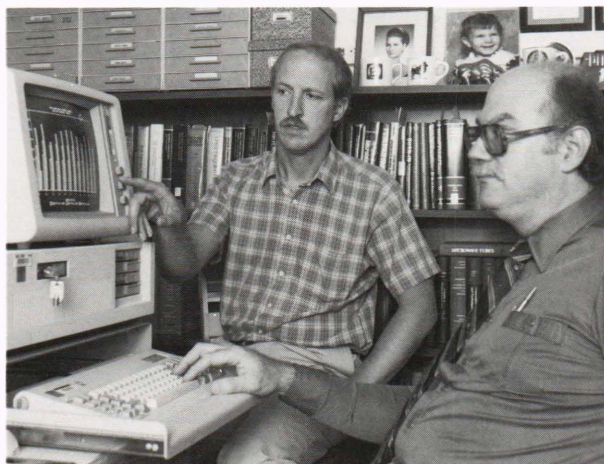

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