TRIAD INCREMENTAL PHASE SHIFTER

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The TRIAD experimental satellite carried a new digitally controlled electronic instrument that has the capability of keeping time in the satellite for weeks to a precision previously available for less than a day. This instrument is an electronic frequency synthesizer whose frequency transfer function (input to output frequency) can be remotely programmed to compensate for frequency and time errors caused by an aging and drifting reference oscillator. The design allows for frequency adjustment in incremental steps of 7×10^{-13} over a continuous range of ± 20 Hz. This report describes the design interfaces with the spacecraft, ground test results, and the tactics for operation in orbit.

Introduction

IN PREVIOUS SATELLITES IN THE TRANSIT PRO-gram, time and frequency were both derived from stable crystal oscillators, but only time was normalized to a predetermined value; the transmitter carrier frequency was allowed to drift with the frequency drift of the reference oscillator. Time normalization was accomplished by subtracting or deleting pulses in the timing chain in a pattern that very nearly repeats every two minutes. The deleted pulses were at 104 kHz, corresponding to 9.6 microsecond time jumps, each deletion being denoted in the transmitted message format. As a result, the Transit system, for all practical purposes, has a design limitation of ± 5 μs in time keeping. Although, in principle, knowledge of these time deletions is provided, because of the logistics in providing complete data and the instrumental difficulties of recovery, the use of this tim-ing has never been promoted as a means of time transfer.

In order to eliminate or reduce this limitation, the time deletion system provided on TRIAD has a 200 nanosecond unit size, intended primarily for initialization of the satellite time system, with the frequency normalized by an incremental phase shifter (IPS) performing the function of an electronic frequency synthesizer. The time deletion circuit is not activated and the pattern is not identified in the message format when the IPS is used. The normalized frequency precedes the RF multiplier chain for the transmitter carriers and precedes the divider chain for the timing system.

To provide 2-minute time marks in previous Transit satellites, the reference oscillator frequency was selected to be $5 [1 - (80 \pm 2) \times 10^{-6}]$ MHz and the timing chain had the divisions shown
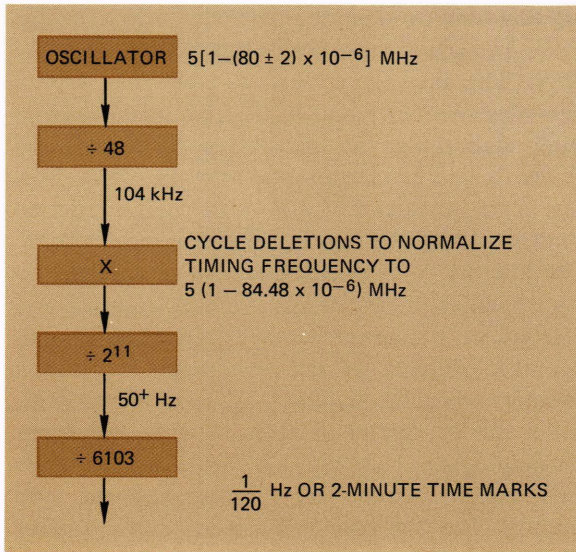
Fig. 1—Previous Transit timing chains.

OSCILLATOR: $5[1-(80 \pm 2) \times 10^{-6}]$ MHz

÷ 48

104 kHz

X — CYCLE DELETIONS TO NORMALIZE TIMING FREQUENCY TO $5(1-84.48 \times 10^{-6})$ MHz

÷ 2^{11}

50^+ Hz

÷ 6103

$\frac{1}{120}$ Hz OR 2-MINUTE TIME MARKS

in Fig. 1. The TRIAD system provided redundant methods of operation pending the successful demonstration of IPS in orbit, and a provision was also made for operating the satellite at a new frequency outside the operationally assigned channel during the testing of the DISCOS system.

Internal to the IPS package are RF switches that allow the Oscillator #1 signal to either bypass or not bypass the IPS circuits. Likewise the Oscil-
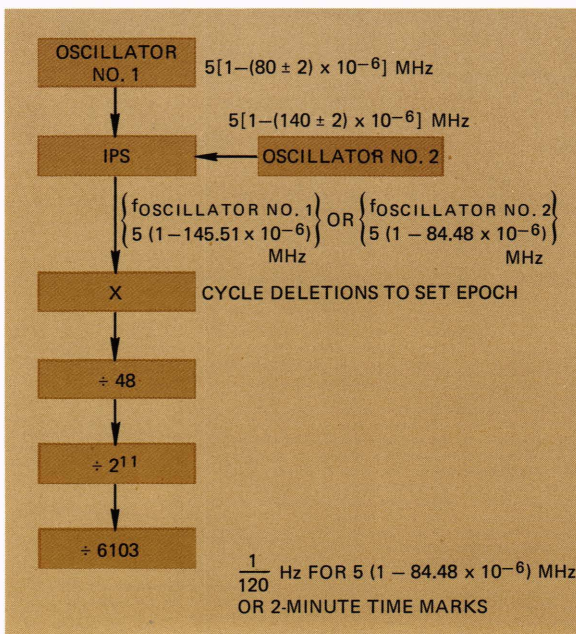

OSCILLATOR NO. 1: $5[1-(80 \pm 2) \times 10^{-6}]$ MHz

$5[1-(140 \pm 2) \times 10^{-6}]$ MHz

IPS ← OSCILLATOR NO. 2

$\begin{cases} f_{OSCILLATOR NO. 1} \\ 5(1-145.51 \times 10^{-6}) \end{cases}$ OR $\begin{cases} f_{OSCILLATOR NO. 2} \\ 5(1-84.48 \times 10^{-6}) \end{cases}$
MHz   MHz

X — CYCLE DELETIONS TO SET EPOCH

÷ 48

÷ 2^{11}

÷ 6103

$\frac{1}{120}$ Hz FOR $5(1-84.48 \times 10^{-6})$ MHz OR 2-MINUTE TIME MARKS

Fig. 2—TRIAD timing chain.

lator #2 signal can either bypass or not bypass the IPS circuit. With this combination of circuits and oscillators, the system can operate on either the new frequency channel or operational channel without IPS by using the bypass. On the other hand, IPS can be initially tested in orbit in the new frequency channel and later operated on the operational frequency channels by selections of the proper reference oscillator. The timing chain for TRIAD is shown in Fig. 2. Note that the primary differences are in the position in the chain of the deletion operation and the addition of the IPS.

Principle of Operation

The principle of operation employed in the IPS is to provide 200 equally spaced phases over the span of 2π radians of a 5 MHz signal and then to electronically switch sequentially through these phases as shown in Fig. 3. If the electronic switch scans all 200 phases in one second, the smoothed frequency seen on the switch arm is one hertz higher or lower in frequency depending on whether the switch sequencing is toward advanced phases or toward retarded phases respectively. If the electronic switch advances one phase step in a time determined by dividing the 5 MHz input frequency by N, it is clearly observed that the frequency synthesizer has a unique transfer function. Unfortunately, the resolution in frequency adjustment for N adjusted by ± 1 unit was unacceptably coarse, so a system of alternating between N and $(N + 1)$ was devised; temporary operation at $(N + 1)$ is referred to as γ deletions in the text that follows. The alternating between N and $(N + 1)$ is maintained at the highest rate possible so that although the frequency is alternating between two values, all users on the ground have finite bandwidths and will integrate the received signal to the mean frequency. For one unit in N, the frequency adjustment is 3 or 4×10^{-7} in frequency; there are 2^{20} steps (1,048,576) between N and $(N + 1)$. Therefore it takes $(N \times 2^{20})/f_o$ seconds to realize the maximum frequency resolution (approximately fifteen seconds).

Detailed Design

A simplified block diagram of IPS is shown in Fig. 4. Referring to this diagram, the input RF signal from the reference oscillator enters the delay line and is picked off at one and only one
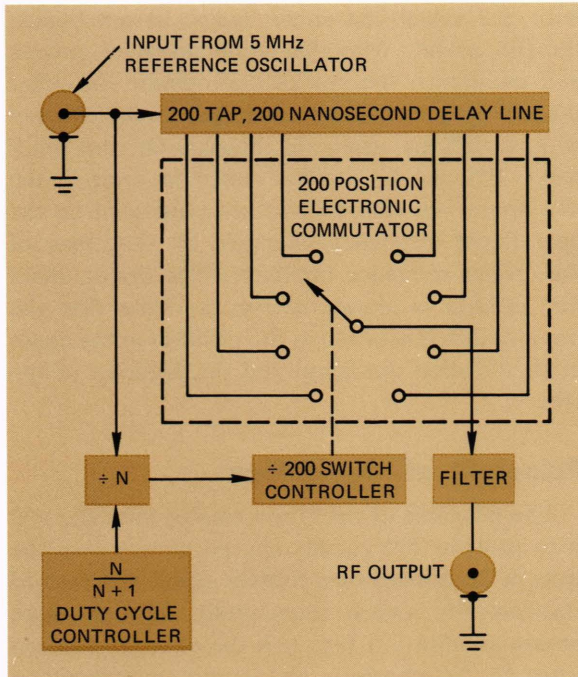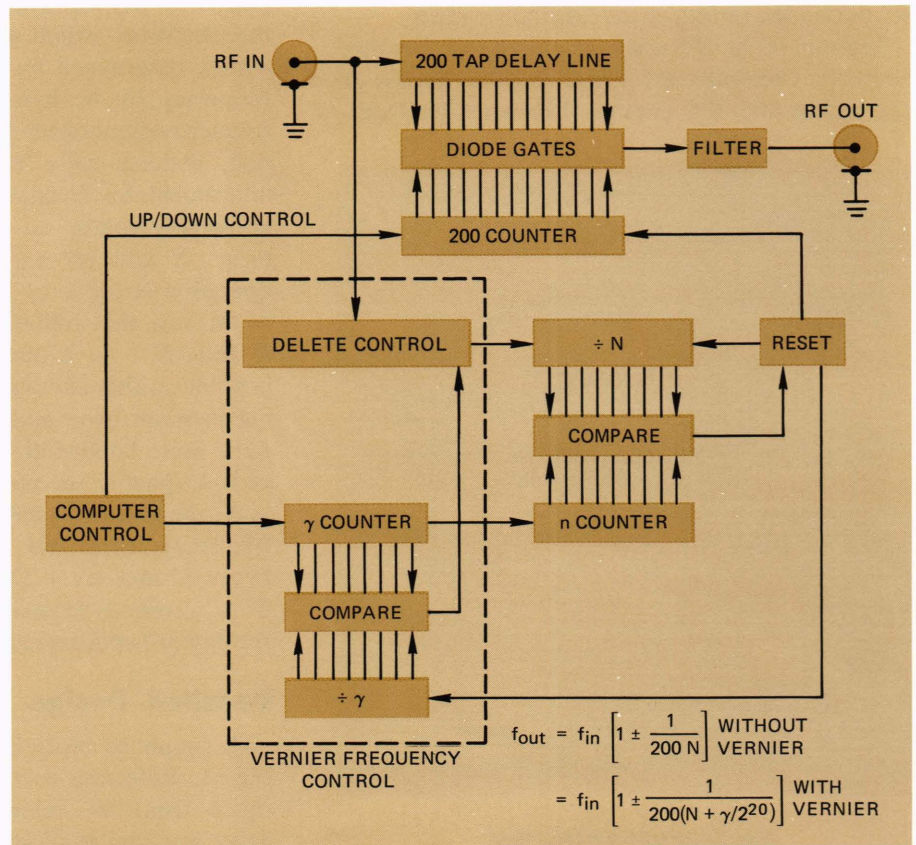
Fig. 3—Principle of operation of IPS.

tap at a time by digitally controlled diode bridge gates. The signal flows out of the diode gates to the filter. The filter is a narrow band-pass crystal filter designed to pass the desired signal derived from smoothing the phase-stepped signal and reject the initial carrier put into the delay line. The input RF signal also goes through a deletion control circuit and into a 7-bit, N-divider circuit. The number N by which this divider operates on the RF signal is selected and remotely inserted into a reference n counter. Comparison circuits monitor the contents of the N divider and the n counter; when the numbers agree in all bit positions, the N divider is reset to zero and starts dividing again. The reset also advances the diode gate switch position by incrementing the 200 counter. The 200 counter is an up/down counter to provide respectively either a higher or a lower frequency in the RF output; the up or down condition is set by an external signal from the spacecraft computer. In addition to the above functions, the reset signal increments a 20 bit γ divider. Each time the γ divider is incremented, comparisons are

Fig. 4—Simplified block diagram of IPS.

$$f_{out} = f_{in}\left[1 \pm \frac{1}{200\,N}\right] \quad \text{WITHOUT VERNIER}$$

$$= f_{in}\left[1 \pm \frac{1}{200(N + \gamma/2^{20})}\right] \quad \text{WITH VERNIER}$$

made with the contents of a γ counter for any bits that have a transition to equality. Note that these comparisons are made by comparing the least significant bits of one with the most significant bits of the other; the number of matches is identical regardless of the order in which the comparisons are made, but the distribution in time is astoundingly different. For the method chosen, the comparisons (or deletions that cause the divide by N circuit to look like a divide by $(N + 1)$ circuit) are distributed as uniformly as a binary counting device can achieve over the period required for the divide-by-γ to process 2^{20} divide-by-N resets.

The contents of the γ counter and n counter are set by pulses provided remotely by the spacecraft computer. Pulses are clocked into the γ counter with controls set to count up or count down. When 2^{20} counts are reached in either direction, the overflow increments the n counter one unit in the corresponding direction. The computer control of these numbers enables the IPS to correct not only for frequency bias but also for linear or quadratic functions of frequency drift in the reference oscillator. If very precise time-keeping is desired, the computer can alternate or duty cycle the IPS between two sets of values for greater time resolution than provided by the smallest resolvable frequency increment.

The frequency of the output signal generated by the IPS is a specific function of the input frequency. Without the vernier control, the relation is given by

$$f_{out} = f_{in} \left[1 \pm \frac{1}{200\,N} \right]. \qquad (1)$$

When the vernier frequency control is used, the relation is given by

$$f_{out} = f_{in} \left[1 \pm \frac{1}{200 \left(N + \dfrac{\gamma}{2^{20}} \right)} \right], \qquad (2)$$
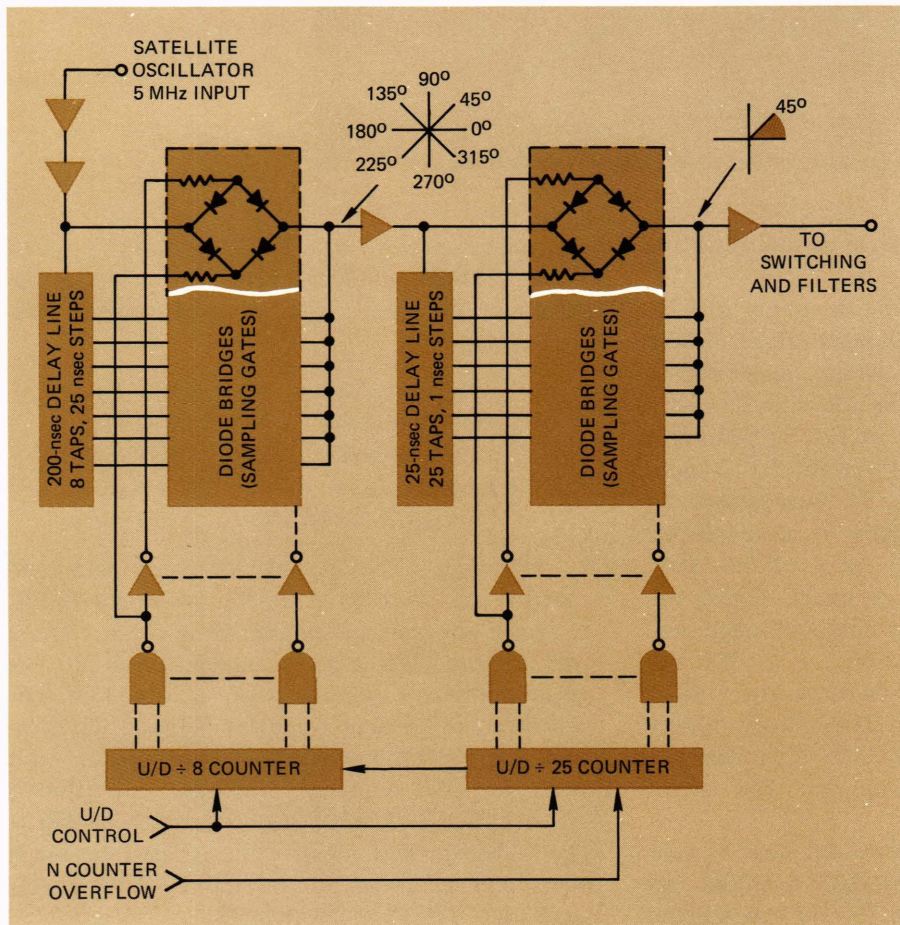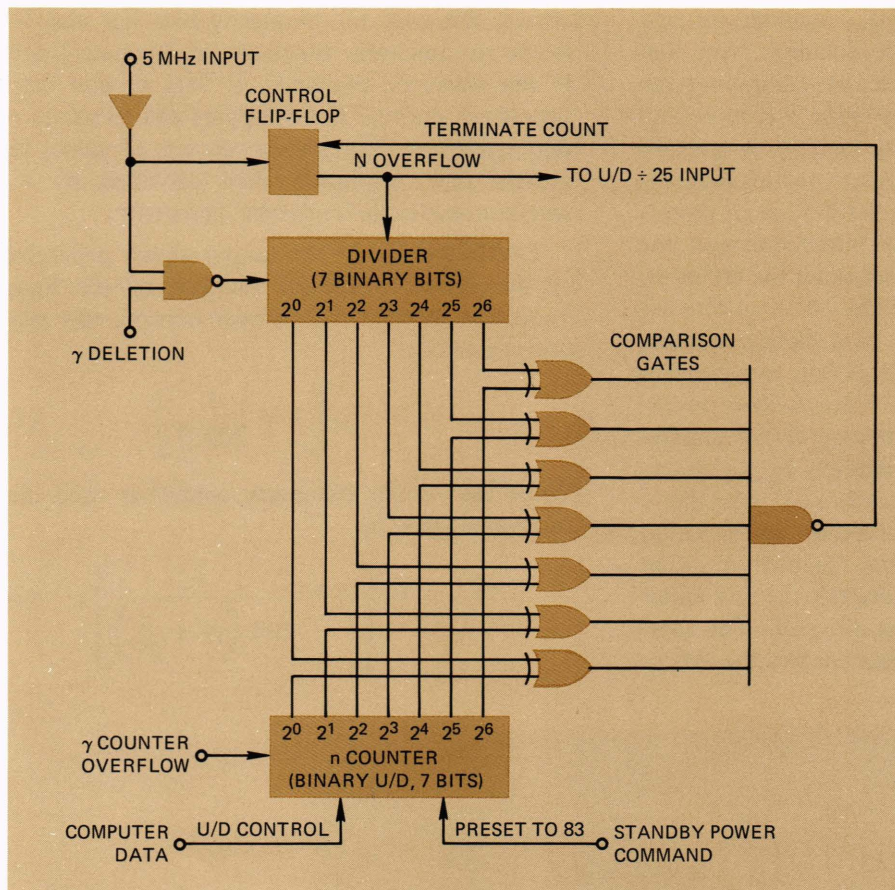

Fig. 5—Diode gates.

Fig. 6—*N* and *n* counters and controls.

where N and γ are the numbers contained in the N and γ counters.

Diode Gates—For economy in circuits and increased reliability, the 200 phases of the 5-MHz signal are generated by providing eight phases spaced 45° apart as inputs to a 25-tap, 25-nanosecond delay line as shown in Fig. 5. The eight phases are provided by eight taps on a 200-nanosecond delay line in steps of 25 nanoseconds. In this way the work of 200 gates is accomplished by $8 + 25 = 33$ gates. The detail of the diode gating is also shown in Fig. 5; digital signals impressed across the bridge of diodes through current limiting resistors turn on the diodes and provide a low impedance path between the delay line tap and the next circuit. These diode bridges pass an analog 5-MHz signal and switch from one tap to the next in much less than one microsecond.

Filter—The narrow-band crystal filter is centered in its pass band at the desired output frequency. There is one filter for the operational frequency centered at 5 MHz − 84.48 ppm and one at 5 MHz − 145.51 ppm. The general properties of the filters relative to their center frequency are:

3 dB bandwidth	± 100 Hz
>10 dB rejection	± 200 Hz
>15 dB rejection	± 300 Hz
Insertion Loss	3.7 dB
Impedance IN/OUT	50 ohms

N **Divider**—The divide-by-*N* circuit and comparison circuits to the *n* counter are shown in Fig. 6. As a convenience in initializing the *n* counter for using the IPS, a preset number is set into the *n* counter every time the power is turned on. The number is 83 which is midway between the nominal numbers used—76 and 90. The number 76 is used to raise reference Oscillator #2 from 5 $[1 - (140 \pm 2) \times 10^{-6}]$ MHz to 5 $(1 - 84.48 \times 10^{-6})$ MHz. The number 90 is used to lower Oscillator #1 from 5 $[1 - (80 \pm 2) \times 10^{-6}]$ MHz to 5 $(1 - 145.51 \times 10^{-6})$ MHz.

Pseudo-Symmetric Time Distribution of Deletions (γ Functions)—The computer-controlled up/down binary γ counter holds a maximum of $(2^{20} - 1)\gamma$ deletions. The fixed interval of 2^{20} N counter overflows takes approximately 15 seconds and is considered the minimum integration time over which the finest resolution of the system may be seen. Within this interval the vernier IPS distributes, in evenly spaced time positions, the total quantity of γ held in the γ counter.

Figure 7 shows the γ counter, comparison counter, and the associated comparison gates in a simplified logic diagram.

The comparison counter is the same length as the γ counter and is clocked continuously by the overflow of the N counter. Since the γ functions are keyed to the N counter, this arrangement gives synchronism to the distribution scheme. Comparisons between the γ and comparison counters are made at the bit level by a cross comparison, i.e., highest order of one to the lowest order of the other, and continue in this manner throughout the length. Each bit comparison independently inserts γ deletions in its time position in an uninterrupted repetitive cycle. The γ counter remains at the same count unless a change in frequency or epoch is desired, in which case the comparison timing eliminates the possibility of erroneous comparisons.

The following example illustrates the γ distribution scheme employed. Assume, as shown in Fig. 8, that a γ count of 63 is held statically in the γ counter. This number, as shown in powers of 2, contains 2^0, 2^1, 2^2, 2^3, 2^4, and 2^5, which would place the first six bits of the γ counter in the "one" state.

Assuming the γ register contained 63 and the comparison counter started at 0, the first comparison would be made at 2^{15} counts. This is compared with the 2^5 bit in the γ counter. The comparisons and subsequent γ deletions occur continuously every 2^{15} counts. The next comparison will be at the 2^{16} count, and since it occurred at the 2^{15} count overflow it would be positioned between 2^{15} counts at alternate counts. The 2^{17}, 2^{18}, 2^{19}, and 2^{20} bits are compared with and distribute the respective 2^3, 2^2, 2^1, and $2^0\gamma$ values in an identical format.

Since all binary levels of γ counts are generated independently, they are combined or "OR'ed" to give a total of all levels evenly positioned as shown in Fig. 8. In the above example the combined levels give equally spaced γ deletions for each 2^{14} count minus the first count after t_0. It follows that $(2^6 - 1) = 63$ and $2^6 \times 2^{14} = 2^{20}$.

To summarize, the 63 γ deletions would delete one 5-MHz pulse from the input to the N counter, changing its count modulus from N to $(N + 1)$
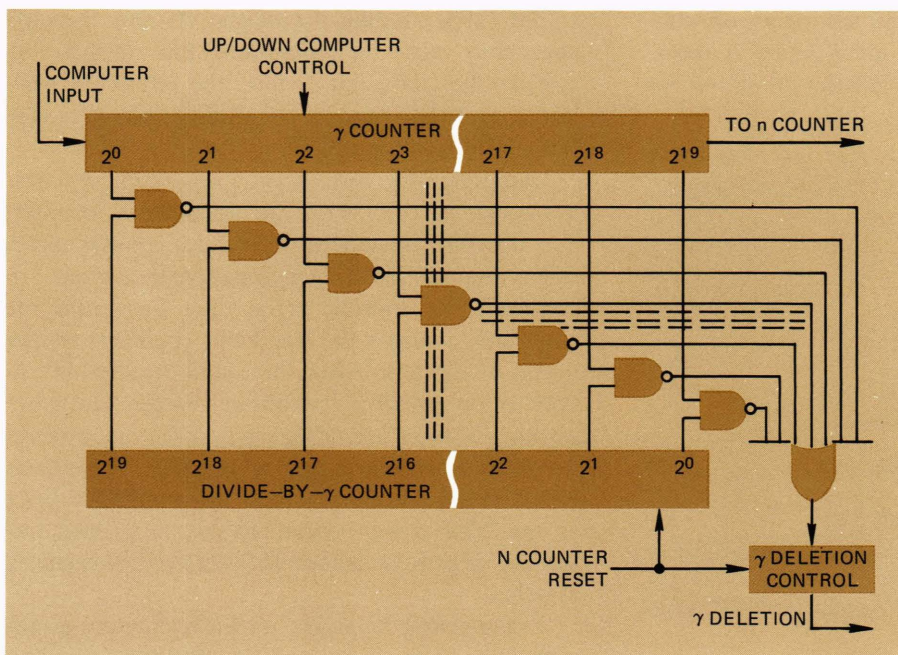

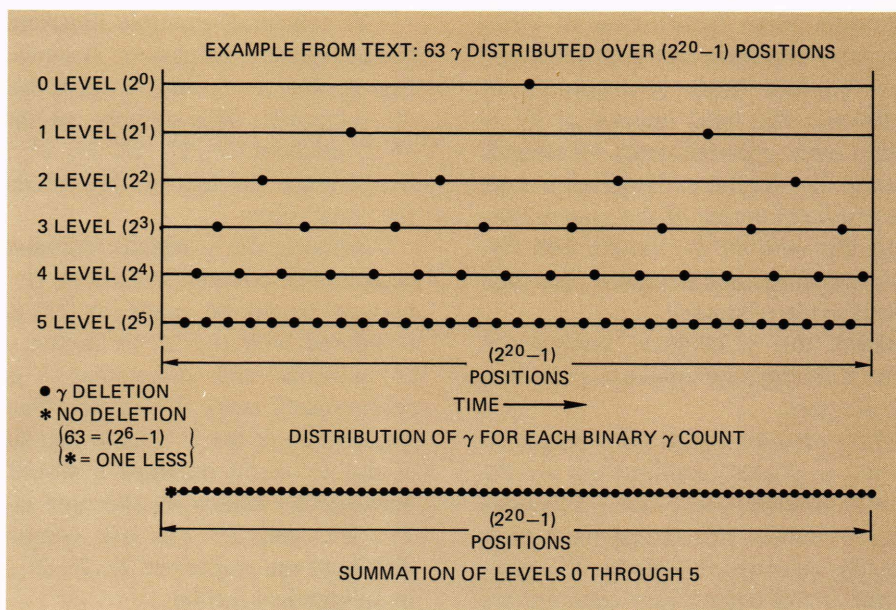Fig. 7—Gamma counter, divide-by-γ circuit, and deletion control.

Fig. 8—Binary pseudo-symmetric distribution of γ deletions.

63 times over the 15-second interval. Thus, the N count is effectively changed to N plus the fraction $63/2^{20}$ for the integration time. The process for each succeeding interval is identical if the γ count remains unchanged.

Another way of looking at the effects of the N-counter and γ-counter effects is to observe the 5 MHz input signal phase as a function of time. In Fig. 9, the effects of resets of the N divider show up as transitions in phase as the risers on stair steps. The length of time a given phase is transmitted to the output filter is the time required for

a divide-by-N circuit to go through its count and be reset. When the γ-deletion pulse appears, the constant phase period is extended by the period of the input 5 MHz signal which is shown in Fig. 9 as a γ deletion time. After the 200th step, the phase drops to zero and the steps sequence through again.

IPS Interfaces

The IPS module interfaces in the TRIAD spacecraft with the computer, the telemetering system, the command system, the reference oscillators, and the frequency multiplier/phase modulator (FM/ϕM) module.

Computer-IPS Interface—The computer communicates directly with the up/down γ counter. The overflow or underflow of the γ counter increments up or down respectively the binary n counter. The transfer serial data line from the computer controls the up/down condition of the γ and n counters. After the initial "power off" to "power on standby" condition change, the states of the γ counter are arbitrary and the n counter is preset to a predetermined value (83). The adjustments to the γ and n counters are completed prior to the "full power mode" to ensure proper frequency alignment before IPS drives the on-board systems.

Telemetering Interface—Two telemetering tell-tales have been assigned to the electronics portion
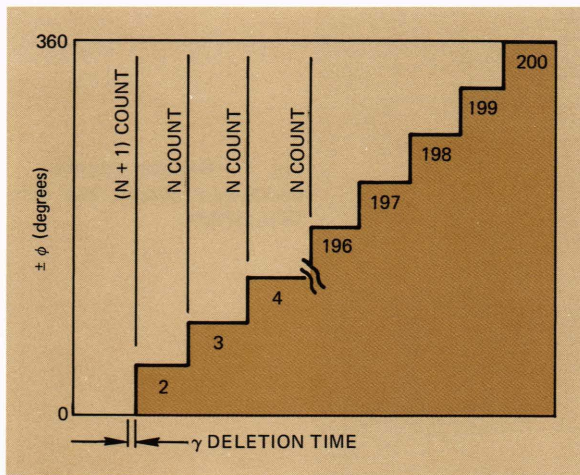

Fig. 9—Deletion of input pulse.

of the IPS: one defines the first bit of the data and remains in the "one" state for this time; the second contains the 32 data bits.

The data from the γ and n counters are parallel shifted, four bits at a time, into a four-bit parallel input (serial output) shift register. The TM frame signal from the telemetering electronics controls the sequence of the parallel shift by incrementing a five-bit binary counter in the IPS. The frame signal also controls the serial shift of the four-bit register, the output of which goes to the TM electronics.

The following lists the assigned TM channels, telltales, and commands for the IPS package:

TM Channel
  IPS Temperature (8 bits)

Telltales
  1. Oscillator #1 (−145.51 ppm IPS Filter)
     Oscillator #2 (−84.48 ppm IPS Filter)
  2. IPS Full Power ON
     IPS Full Power OFF and IPS Bypass
  3. IPS TM Marker Bit
  4. IPS TM Data (32 bits)
  5. IPS Standby Power ON
     IPS Standby Power OFF

Command Interface
  1. Oscillator Select #1 (−145.51 ppm IPS Filter)
     Oscillator Select #2 (−84.48 ppm IPS Filter)
  2. IPS Full Power ON
     IPS Full Power OFF
  3. IPS Standby Power ON
     IPS Standby Power OFF

Satellite Oscillator and FM/φM to IPS Interface—Figure 10 shows the signal flow from the IPS to the FM/φM and from the satellite oscillator to the IPS.

The selection of the −140 ppm or the −80 ppm oscillator is made by the command system through ground control. Since the IPS must accommodate both oscillators, provisions are made for both inputs in the IPS electronics. A buffer circuit with an input resistive summation network accommodates either input while the other oscillator provides a moderately high impedance in the "power off" mode. The buffer is a one-stage transformer coupled output amplifier with an output impedance of 50 ohms and will drive the IPS electronics when the IPS is "on" and drive the cable, through the "bypass" relay, when the IPS is "off". The FM/φM electronics package contains a similar summation network, but three individual amplifier stages drive the FM/φM electronics, the PRN, and the memory/computer electronics.

IPS Adjustment Procedures

There are two operational modes for the IPS; they are:

1. The adjustment to compensate for satellite oscillator long term frequency drift.
2. The adjustment of epoch timing marks (2-minute marks) to a degree of accuracy greater than the present 200-nanosecond lumped time adjustments.

Frequency Adjustment—The resolution for one γ deletion in the IPS system is in parts in 10^{13}. Satellite oscillator long term drift has been typically parts in 10^{11} per day. In correcting for this first order drift curve the IPS system, through computer control, would be updated at the rate of

Fig. 10—IPS-oscillator and IPS-FM/φM interface.
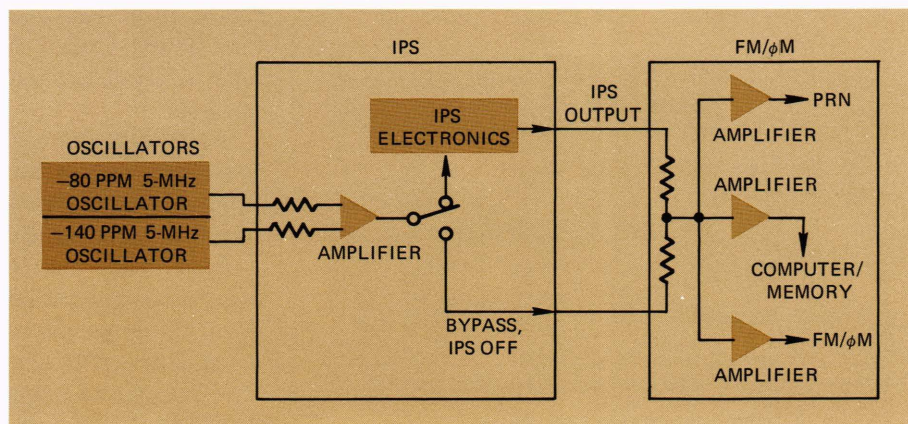
100 γ functions per day. Considering the 720 2-minute marks occurring each day, this would represent a rate approximately equal to a γ function for each fourteen minutes.

IPS may be commanded to perform a smoothing γ rate function (the rate of which will be second or third order) to provide a first order corrected frequency curve as illustrated in Fig. 11.

Epoch Adjustment—The TRIAD timing system has a cycle deletion process for adjusting time under computer control to the nearest 200 nanoseconds. The IPS system can be used to refine this adjustment to a resolution of better than one
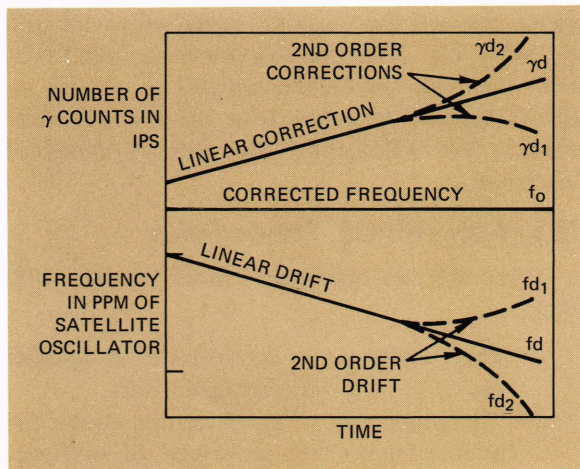
Fig. 11—First and second order distribution of γ for the correction of first and second order frequency drifts.

nanosecond. The procedure is illustrated in Fig. 12. The IPS is commanded through the computer to go to an offset frequency, there to dwell until the epoch error is reduced to zero and then commanded back to provide a frequency that accumulates no time error.
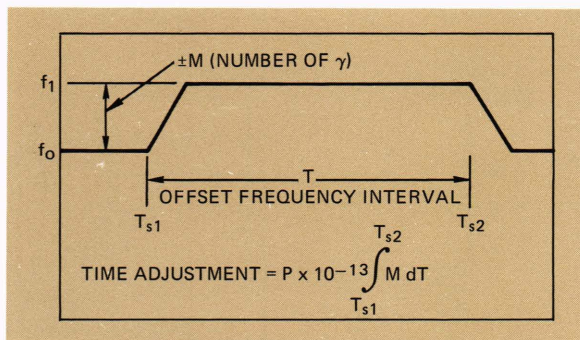
Fig. 12—Epoch adjustment.

Ground Tests with IPS

Tests were performed on combinations of cesium frequency standards, laboratory crystal oscillators, the TRIAD flight reference oscillators, and the IPS. The instrument noise in the IPS was determined by the setup shown in Fig. 13. IPS plus a divider provided one clock. Another divider provided the other clock. Both clocks were driven by the same stable cesium frequency standard. The difference in time between these two clocks showed an instrumentation noise of about 300 picoseconds.

Long Term Aging—The aging rate of the TRIAD oscillator to be used with IPS to generate standard satellite time was determined over a 30 day test with the oscillator in a laboratory vacuum chamber. At best, 7 or 8×10^{-11} per day was attained, or about five microseconds per day for timekeeping.
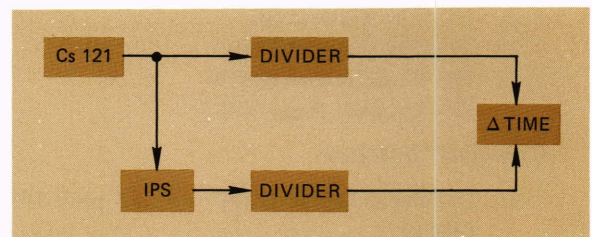
Fig. 13—Cesium (SN 121) versus IPS (offsetting cesium (SN 121)) instrumentation noise.

Long Term Aging Corrections—When two cesium frequency standards were used to drive two clocks, with the frequency of one standard adjusted by IPS to the frequency of the other standard, as shown in Fig. 14, the difference in accumulated time was under the best case observed to be less than ten nanoseconds error in four hours. Under the worst case observed the time accumulated ten nanoseconds difference in one hour.

When a laboratory oscillator replaced the IPS controlled cesium standard of Fig. 13, the best result obtained was a time error of 100 nanoseconds accumulated over three days.

Tests made on the TRIAD flight oscillator over a 30 day period showed that the best that could be done was about 200 nanoseconds over seven hours. The problem in keeping any better time was due to frequency jumps that occurred in the TRIAD oscillator. These jumps were as large
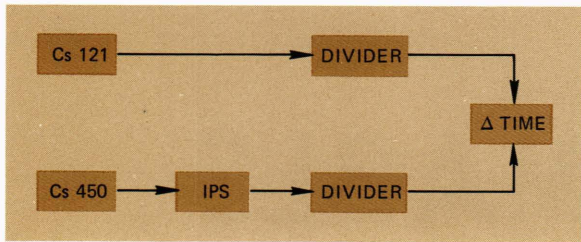
Fig. 14—Cesium (SN 121) versus cesium (SN 450) IPS controlled best case.

as 5×10^{-11} and occurred as infrequently as one in two days or as frequently as four in one day.

Short Term Frequency Stability—The short term frequency stability of a clock driven by an oscillator with and without IPS was measured against a quality rubidium frequency standard. The IPS was observed to modify the inherent short term stability of the oscillator for periods less than five seconds averaging time as shown in Fig. 15.

In-Orbit Tests with IPS

During the post-launch operations, the IPS device was exercised and performed the precise frequency translations commanded by the computer. The epoch setting process was fully confirmed and refined time adjustments were being made when the spacecraft malfunction occurred that suspended use of the computer and the operation of the IPS in TRIAD. The IPS operation in orbit disclosed some operational problems that will be corrected in future models. For instance, switching between oscillators introduced a step in time of nearly three milliseconds because mechanical relays were used.

The IPS epoch adjustment experiments in the TRIAD post-launch operations were of two kinds. First, engineering checks were made to confirm the proper communication between the power, command, telemetry, and computer with the IPS. Second, known values were placed in the IPS to offset the frequency by a magnitude where confirmation could be made via downlink epoch pulses on the received satellite frequency.

The initial settings for frequency offset were large in magnitude since gross time adjustments were attempted for the four-day period. During
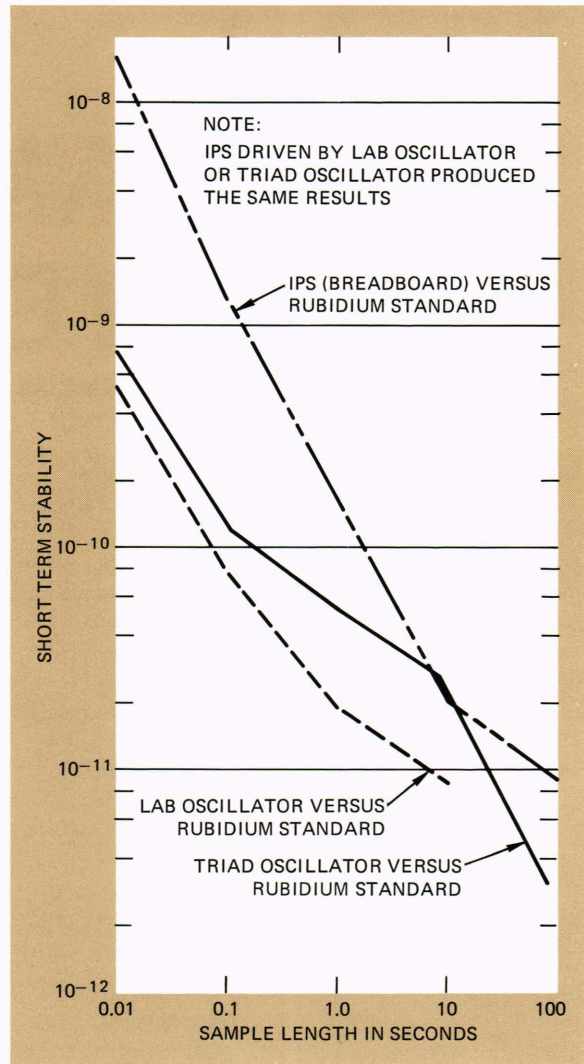

Fig. 15—Short-Term stability.

this time all computer programs and all modes of operation were confirmed.

The second series of tests was intended to refine the epoch steering to the nanosecond region. These tests were never completed because of the computer malfunction.

Conclusion

The Incremental Phase Shifter can adjust the frequency of a spacecraft oscillator, limited only by the ability to predict the rate of drift. IPS can adjust the time of a spacecraft clock, limited only by the ability to measure the time in the spacecraft from signals received on the ground.