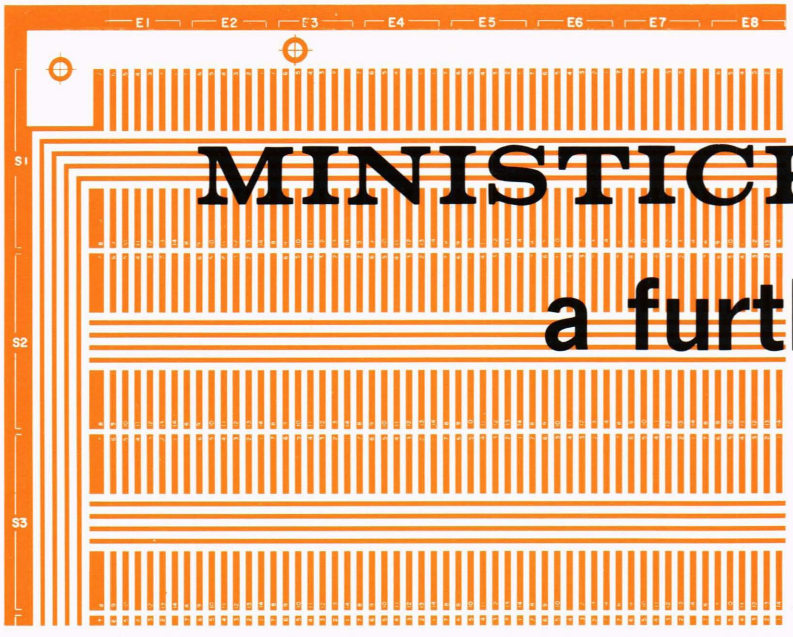

MINISTICK PAC

a further aid

Shortly after the proven success of the electronic integrated circuit (IC), it became apparent that the limiting factor in its effective use was going to be in the product design area. The introduction of the integrated circuit allows the circuit designer to think strictly in terms of logic functions rather than in terms of the conventional units of resistance, capacitance, and active elements. While this, in itself, does not necessarily lessen the task of the circuit and system designer, it does allow him to turn out rather sophisticated designs in short order, generally faster than packaging facilities can accommodate them. This situation, of course, increases the burden of the packaging engineer, and, at the same time, introduces new factors that are directly related to reliability.

The integrated circuit possesses a higher intrinsic reliability than an assembly of discrete components that performs the same logic function. Maintaining this potential reliability through manufacture and test poses a whole new series of problems by virtue of the delicate nature of the device. Typically, an integrated circuit is a small chip of silicon that has been converted into an electrically active device by the use of rather complex processes that are beyond the scope of this article. To afford maximum physical protection, the chip is hermetically sealed into a metal, glass, or ceramic case that contains an appropriate number of leads for communication with the outside world.

Several case styles are available from various manufacturers; but the one that appears to be gaining in popularity, due in part to its efficient use of space, is the so called "flat pack." A typical example is shown in Fig. 1. Note that as many as 14 leads, 0.004-inch thick by 0.015-inch wide, may be found on a case only 1/8-inch wide by 1/4-inch long. Obviously, these leads must not be broken; nor should they be subjected to any undue stresses at any time. This condition requires the design of special handling fixtures for use during test and appropriate tooling for use during manufacture. To achieve maximum reliability, the smallest number of connections possible should be made to each of the leads. Although the power dissipated in each unit is only a few milliwatts, the total heat generated by a large number of them placed in a small volume is a factor that must be considered in the engineering design.

With these considerations as a background, the task was to develop a satisfactory packaging system for use with integrated circuit flat packs. The system was to be completely defined in the form of process manuals and a small pilot line for the production of space vehicle electronic assemblies established. The task has been essentially completed. The packaging system evolved has been named "ministick," and will be described in some detail in this article. A pilot line is in operation and is currently being proven by the design and fabrication of a new type of memory for use in Navy Navigational Satellites.

KAGING to satellite reliability

C. F. Noyes

The introduction of the integrated circuit with its inherent reliability has offered a real challenge to the electronic product designer. An approach toward maintaining this reliability throughout the hazards of manufacturing and test has recently been developed at APL. This method, known as ministick, promises a significant reduction in the effort required to build and test electronic hardware, and is discussed in some detail in the accompanying article.

At the start of the project, a survey was made to determine the approaches being followed by others in the field. Of course there were many, but they can be reduced to three basic systems:

1. Modular "3D" systems, of which welded cordwood as currently used in APL space hardware is typical.
2. Conventional printed circuit boards.
3. Multilayer printed circuit boards.

The various modular systems are extremely rugged and basically reliable. They all suffer from a common problem, however, that derives from the fact that some type of encapsulation is required. Because of the rather complex assembly methods used, electrical tests must be performed at several levels of assembly to assure satisfactory performance during final tests. Each of these tests interrupts the assembly process and, of course, increases the manufacturing time. In addition, if trouble occurs after encapsulation, isolation and repair of the fault become extremely difficult. These difficulties were deemed sufficiently serious to warrant the consideration of a single-plane matrix that would accommodate the large number of wires required and at the same time simplify the manufacturing and test operations.

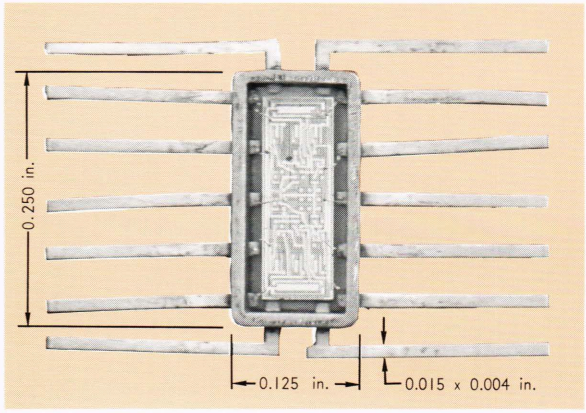

Fig. 1—Typical integrated circuit flat pack with cover removed.

A conventional printed circuit board offers design simplicity but does not permit efficient use of space. This type of circuit board was discarded in favor of the remaining approach, the multilayer printed circuit board. Ministick is basically a multilayer printed circuit board with variations that eliminate most of the problems inherent in conventional multilayer boards. Figure 2 illustrates the main difference between various types of boards. As seen in the illustration, the conventional multilayer board requires connections between circuit elements on layers that may be rather widely separated. There are several ways to accomplish this. The method shown in Fig. 2A is the simplest but least efficient from a space standpoint, and its use is generally limited to applications where few layers are required and soldering is acceptable. The method shown in Fig. 2B is more efficient in the use of space since the large access hole for a soldering tool is not required. Connec-

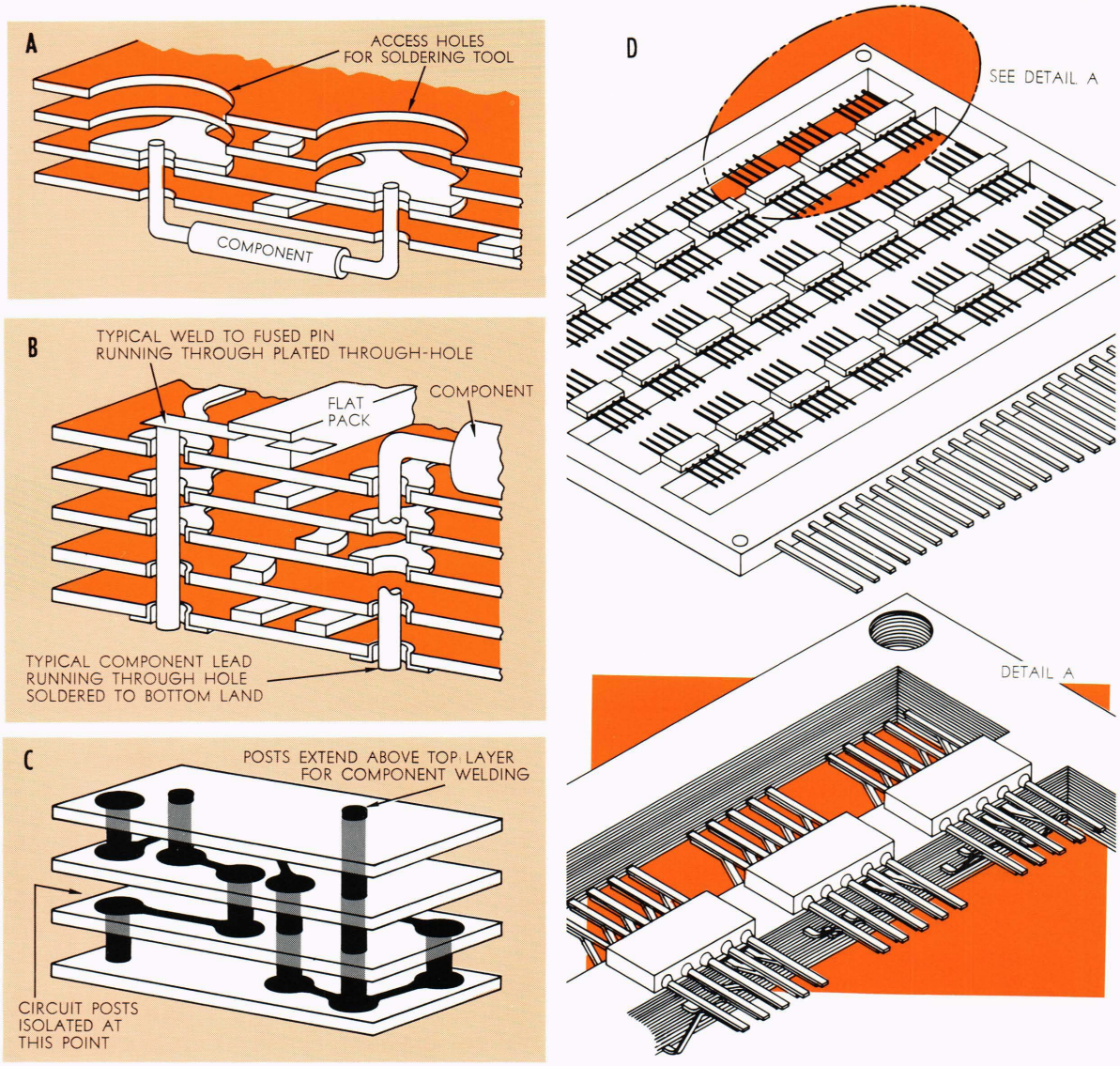

Fig. 2—Various circuit board design approaches.

tions between layers can be made by means of plating through the holes, thus forming a metallic bond between lands pierced by the hole and isolating other areas. Sometimes an indium-plated steel pin is pressed through the hole and, by a suitable fusing process, is made to contact all land areas. If this pin is allowed to extend above the top layer, a post is available to which component leads may be soldered or welded. Figure 2C illustrates the solid post laminate method. The individual layers are prepared and holes drilled at appropriate points. When the first two layers have been laminated together, they are placed in a plating bath that grows a "post" through the holes and establishes a bond where a metal land exists on the second layer. The third layer is then bonded in place and the plating process repeated. Where a hole in the third layer exists, the post continues to grow; where no hole exists, the post is stopped and the area above is now free to be used for other circuits. The process is continued, one layer at a time, until the board is complete. The components are finally welded or soldered to the posts appearing on the top layer.

These three basic methods are time consuming to design, the latter two because of the need to think in three-dimensional terms. In addition, the latter two are time consuming to produce because of the complex methods of interlayer connections. Yield rates on completed boards are disappointingly low. As in any controversial

area there are many opinions on the virtues and shortcomings of the various methods. The following is a summation of what are believed to be the major shortcomings of existing methods:

1. Existing multilayer boards are difficult to manufacture and difficult or impossible to repair.
2. The reliability of plated through-holes and fused pins has not been well established and is subject to question.
3. The time required to convert an engineer's circuit design into operating hardware is unreasonably long.
4. The recovery time from a last-minute design change, or an accident during test is excessively long.

The design approach shown in Fig. 2D, the ministick design, eliminates most of the above shortcomings. Reliability was uppermost on the list of requirements because of the design goal of a five-year operational life in orbit for the Navigational Satellites. Connections between components have been significant contributors to unreliable operation. Ministick has achieved an irreducible minimum of connections by the incorporation of two features:

1. No more than one connection is ever required for each integrated circuit tab.
2. No interlayer connections are ever required on a single board. A connection, in this case, is defined as the joining of two separate pieces of metal by any means.

The reasoning behind this approach is simply that regardless of the quality of any joint, if the joint can be eliminated, the overall reliability must be enhanced.

Conversion of an engineering design into operational hardware has been greatly simplified by close coordination of the "breadboard" and final designs. This was accomplished by the use of two devices:

1. A standardized format for the multilayer board was created, the form factor of which was dictated by the complexity of the system and the space available in the final package.
2. The system breadboard was constructed in this same format but generally on a larger scale for ease of wiring.

By this means, extremely close coordination can be maintained between the progress of the breadboard checkout and the configuration of the final package. This is accomplished by a very simple procedure:

The system engineer creates a logic diagram of his device and, in cooperation with the packaging engineer, breaks it into reasonable subsystems. For example, if the device will contain 600 integrated circuit packs and the packaging space available is a fairly large area with limited height, two boards containing 300 integrated circuits each or four with 150 each might seem attractive. Alternatively, if the space were more cubical, it might be desirable to use six 100-chip boards or twelve 50-chip boards. Other things being equal, the more chips (integrated circuits) that can be put on a board, the fewer connections will be required and, therefore, the higher will be the reliability. This situation, however, involves a tradeoff among logical break points in the electrical system, the size of the boards that can be handled in the manufacturing facility, the ability to test subsystems, etc.

When this tradeoff decision has been made, a logic diagram that will in turn define the content of each ministick board is drawn for each of the subsystems. A standard format for the multilayer board is developed; it will take the form of a matrix and will define the location of every possible circuit path on a given layer of a board. A typical format is shown in Fig. 3. Since the format is in matrix form, each connection can be defined by a three-unit number comprising the row (S), column (E), and IC tab position number. For example, 3-2-12 would define pin 12 on the second IC in the third row.

When the format has been selected, the packaging engineer goes to the subsystem logic diagram and groups the logical functions into available integrated circuits (subject to limitations placed on him by the design engineer and the reliability considerations). The integrated circuits are then annotated with respect to the position they will occupy on the matrix, and pin numbers are assigned. (See Fig. 4.) When this has been done, a tabular list is prepared, defining the terminations on every conductor within the board. It will readily be seen that from this point on the production of the complete multilayer board could be automated by transferring this list to punched tape which in turn would activate appropriate machinery. Currently, however, this tabular list is given to two people, each of whom is careful to use no information other than that contained in this list:

1. A technician reporting to the design engineer who wires the system breadboard previously mentioned.
2. A design draftsman who produces the artwork for the ministick board.

These two men working independently, but in parallel, will produce identical circuits. When the breadboard is completed, it is used by the design engineer to prove the validity of the logic design. If any system changes are necessary, they are very easily incorporated into the ministick board layout by a modification to the tabular list. Such close coordination between the two design activities results in the availability of a piece of prototype hardware very shortly after approval of the breadboard design.

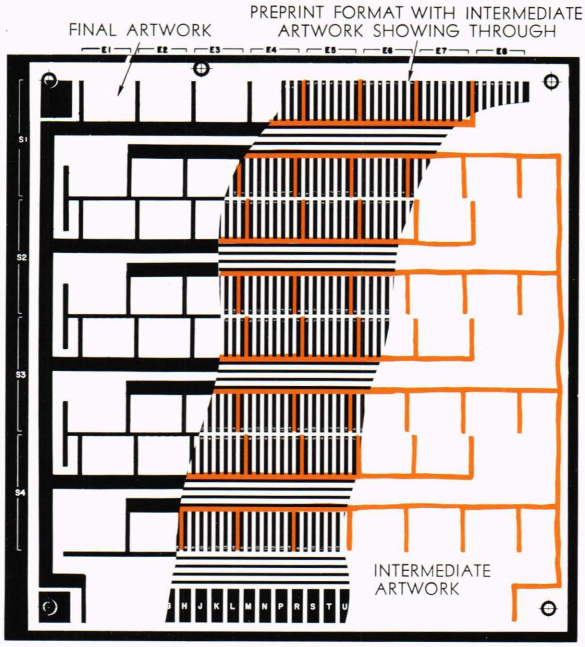

Fig. 3—Method of producing artwork for individual boards.

To produce the artwork from which an individual board layer is eventually made, a draftsman uses two aids: the matrix format shown in Fig. 3; and the tabular list of required conductors.

The format is placed on a light table, and a sheet of translucent paper is taped over it. From the tabular list, the draftsman selects the first group of numbers representing one connection and makes a colored mark on the translucent paper at the appropriate point. He continues until all terminations in this particular conductor group have been marked, at which time he interconnects them following the guide lines on the format. Relating this to a typical cable he has now accounted for the equivalent of n−1 wires, where n is the number of terminations. This process is repeated, carefully considering each conductor group on the tabular list, until no more groups can be placed without encountering a crossed line. As each group is located, the layer number is entered in the left column of the list. This provides a permanent record of the location of each conductor, and assures that duplications do not occur. The sheet of translucent paper, which is called the intermediate artwork, is appropriately coded and set aside.

Using a second intermediate artwork sheet, the draftsman locates the first conductor on the list that is not identified by a layer number and repeats the entire process until he has accounted for all of the conductors. Each sheet is identified by layer number.

Experience has shown that there is little or no correlation between the number of integrated circuits on a board and the number of layers required. Boards containing 24 chips have been built with 11 layers, some with 32 chips have required as few as seven, and a current design using 120 chips requires only 16 layers. It has also been found that laborious studies concerning the placement of chips on a board are not warranted. The draftsman quickly develops an ability to group the circuits in a logical pattern and further refinements make little difference in the total number of layers required.

The final artwork is prepared by the use of a special taping format which is a standard mylar preprint shown in Fig. 3. A light-table overlay is made with the matrix format on the bottom, the appropriate piece of intermediate artwork taped in register over it, and a taping format taped in register on top. The colored pencil lines that are seen through the stackup represent conductors that are required on the finished layer, and their precise location is determined by the white lines showing through from the bottom layer. The draftsman is provided with tape that is precisely the same width as the white lines on the matrix format. He now lays the tape in the designated areas, being very careful to cover accurately the white lines. This process is, of course, repeated for each piece of intermediate artwork, and the resulting taped sheets represent the final artwork. Photographic reductions of these masters form the basic ingredient used in the production of the multilayer boards.

Among the features that are unique to ministick are the "windows" in the board into which the integrated circuit tab connections extend. Since the windows pass completely through the board, it becomes necessary to pierce both the metallic and dielectric parts of the layers. Re-

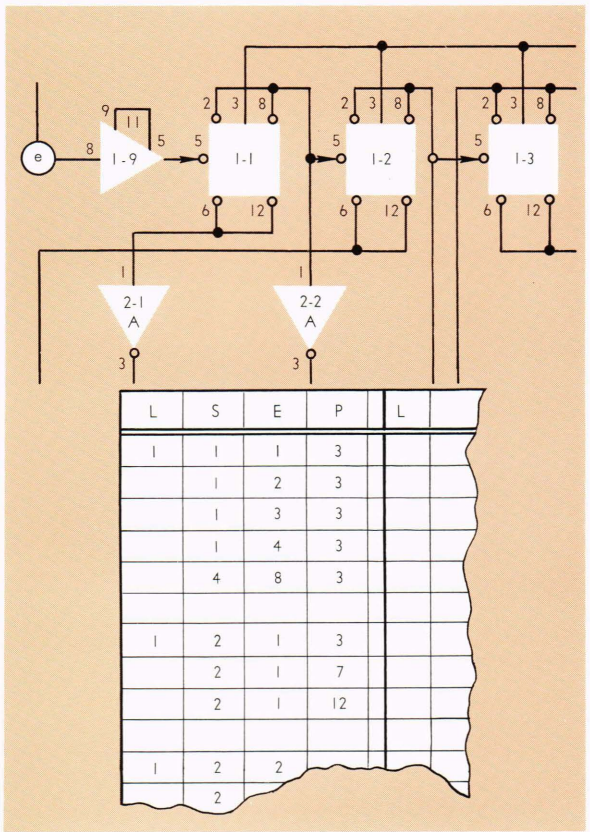

Fig. 4—Typical logic diagram and tabular list of conductors for use in circuit design of multilayer boards.

moving unwanted metal from a metal clad dielectric sheet is a simple process; conventional printed circuits have been made by a photochemical etching process for years. Removal of the dielectric can be done by a similar process, but several undesirable features are introduced. Mylar (DuPont trademark), for example, can be chemically milled (etched) by the use of hot sulphuric acid, which poses no serious problem. Mylar, however, is not mechanically suited to the job because of its tendency to warp, its extreme flexibility, and its relatively soft texture. There are other homogeneous plastic materials available, but all have similar mechanical characteristics.

To provide the mechanical features desired, an epoxy impregnated glass cloth is ideal; but chemical removal of unwanted areas in a laminate requires the use of extremely unfriendly etchants such as hydrofluoric acid. Since the use of such chemicals seemed undesirable, the decision was made to fabricate the dielectric/metal substrate by mechanically cutting the window pattern in epoxy glass cloth and subsequently bonding it to the metal sheet. In the relatively small quantities used to date, the glass cloth has been cut by hand with a sharp knife; however, for larger quantities, it would be economically feasiable to die-punch the sheets.

Part of the design draftsman's job is to provide appropriate tooling designs to aid in manufacturing and to maintain precise alignments where required. In this case, tooling is required to establish the window pattern in the dielectric material and to hold it in proper registration with the photonegative during subsequent operations. Additional tooling is required to maintain alignment of the several layers making up the board during the final lamination process.

Fabrication of the ministick multilayer board is accomplished in four steps which will be described in some detail:

1. *Production of substrates.*

During this process, the basic substrate is formed by bonding the appropriate dielectric material to a sheet of metal. The dielectric, in this case, is a sheet of glass cloth that has been impregnated with epoxy resin and cured to the "B" stage. The dielectric is 0.004-inch in thickness, is dry to the touch, and can be handled without undue caution. The required number of these sheets are sheared to the size dictated by the drawing, stacked, clamped to a template that accurately locates the tooling holes, and drilled. They are then individually taped over a template and the pattern is cut, using a steel straight-edge and a sharp knife.

The metal used is Kovar (Westinghouse trade name), an alloy of cobalt, nickel, and iron. It was chosen because of its ease of welding, good chemical milling properties, and relative toughness. Its least desirable attribute is its relatively high electrical resistivity. A conductor 0.004-inch thick and 0.020-inch wide has a resistance of about 0.1 ohm/inch; but, since the current involved in the majority of cases is negligible, no problem exists. In the case of power and ground leads, the conductors are appropriately widened to lower the resistance. The substrates are sheared to size, stacked, and tooling holes drilled from the same template used for the "B" stage sheets. These Kovar sheets are degreased, scoured with an abrasive detergent cleanser, and thoroughly dried.

The bonding of the dielectric to the metal is accomplished by use of a bonding jig. A sheet of the "B" stage is lowered over the tooling pins, and a sheet of Kovar is dropped

over it. In practice, several substrates are made at one time by interleaving each substrate with a material to which the "B" stage will not bond. When loaded, the top plate of the jig is put in place and the assembly is placed in the laminating press. This press is basically a pair of electrically heated platens that can be forced together by hydraulic pressure.

The epoxy resin, being cured to the "B" stage, will liquefy at a temperature of about 330°F and flow onto the Kovar, forming an excellent bond. After about 2 or 3 minutes at this temperature, the epoxy begins to gel, at which time the pressure between the platens is raised to about 5 psi and held for 40 minutes. During this time the resin is fully cured. After cooling and removal from the jig, the substrates are ready for the chemical milling process.

2. *Formation of the individual layers.*

Chemical milling is a relatively new industrial process which is based on the photoengraver's art. In this process, a chemically resistant photographic image is formed on the surface to be etched; subsequent exposure to a suitable etchant removes all material not protected by the image.

To form the image, the substrate is carefully cleaned, dried, and dipped in a photosensitive lacquer such as KMER (Eastman Kodak trademark). After being thoroughly air dried and baked, this substrate is attached to the appropriate artwork negative and held in proper register with the dielectric pattern by the tooling jig. Exposure to a high intensity light, such as a carbon arc, for about 2 minutes polymerizes the lacquer in the clear areas of the negative, making it impervious to the developing solution. This developer can be likened to a paint remover that softens the lacquer in the unexposed areas of the substrate and allows it to be washed off in running warm water.

The substrates are now placed in a chemical milling machine that exposes them to a spray of ferric chloride heated to about 125°F. Complete piercing of the metal, which is 0.004-inch thick, occurs in about 7 minutes. The completed layer now appears as in Fig. 5. Note that all the circuitry lies on the dielectric areas of the layer just as in a conventional printed circuit board, but that tabs extend beyond the dielectric into the window areas. These are the tabs that are eventually welded to the IC tabs.

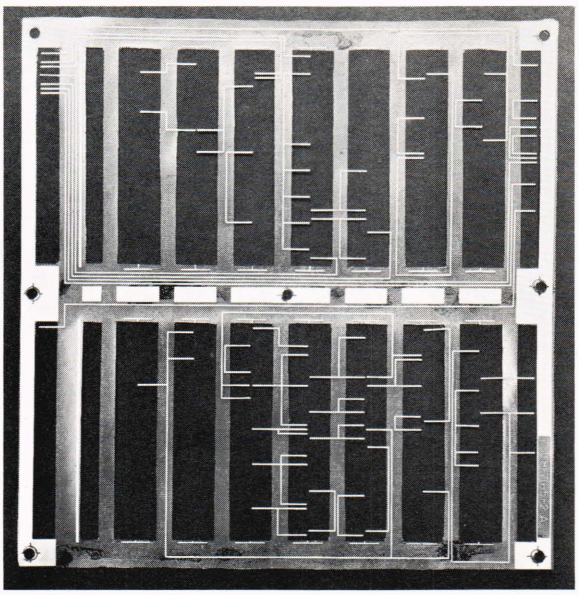

Fig. 5—Completed layer ready for lamination into final board.

The photoresist is removed from the metal areas by a suitable solvent, and the layers are now ready for lamination into the final board.

3. *Lamination of the multilayer board.*

Final lamination is essentially a duplicate of the bonding part of step 1 in this series. The layers are placed on the same jig, each being interleaved with a sheet of the "B" stage sheet used in step 1. Bonding of the entire stack is accomplished at the same temperature and pressure used in the substrate bonding process. This is possible because the process is dependent upon temperature and force per unit area. The area is the same regardless of the number of layers, and the heat transfer characteristics of the materials are such that the center of the stack reaches the proper curing temperature during the 40-minute cycle. After the finished board is cooled and removed from the press, it is lightly clamped between two heavy sheets of metal and placed in an oven heated to about 250°F for 1 hour. It is then removed from the oven and allowed to cool to room temperature while still clamped. This annealing process relieves any internal stresses that may have existed within the board, and prevents warping.

4. *Assembly of components.*

Attachment of the integrated circuit modules to the ministick board is accomplished by use of the welding setup shown in Fig. 6.

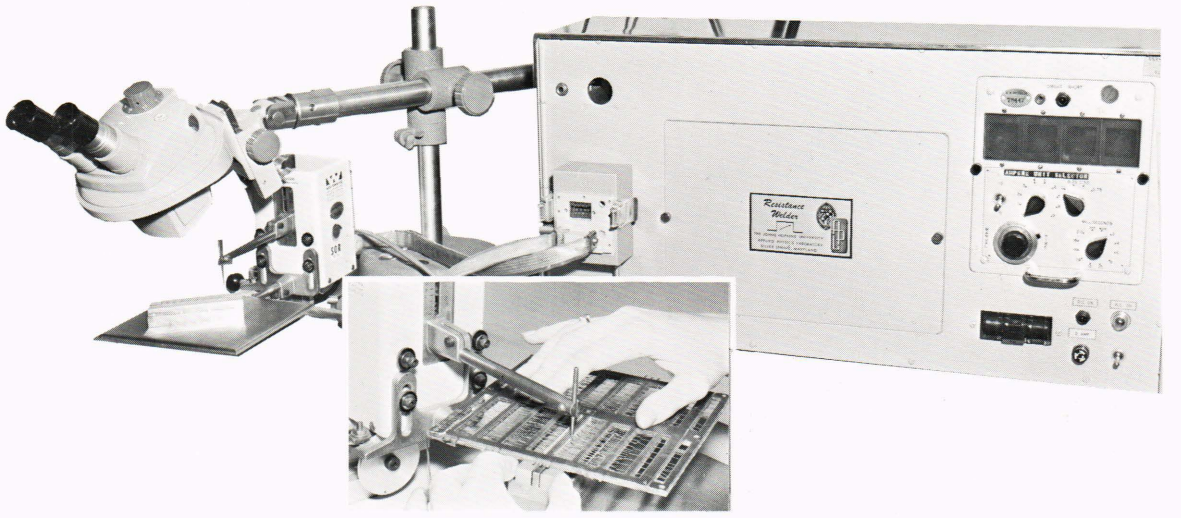

Fig. 6—Welding setup, showing detail view of welding head, chips, and fixture.

The integrated circuits are secured in place, one "stick" at a time. The chips are placed upside down in the pockets seen in the fixture (see detail in Fig. 6) with their tabs aligned by the combs along the edges of the pockets. The location and type of each chip is determined by the assembly drawing of the board. To aid in holding the chips in place, an adhesive is sprayed through a suitable mask onto the "stick" areas of the board after which the board is carefully lowered over the loaded fixture. The tabs on the board are guided in place by combs. A firm pressure on the "stick" will cause the chips to adhere, after which the board is carefully removed from the fixture. This procedure is repeated until all sticks on the board have been loaded, at which time the assembly is checked against the drawing to assure that all chips are of the proper type and in the proper location. As seen in Fig. 6, the welder is slightly modified by the substitution of a copper plate for the lower electrode, and an extension of the upper welding tip. Just as in loading the board, the integrated circuits are welded one stick at a time. The board is inverted and one of the sticks lowered into the welding fixture. The assembly is placed on the copper table, and using an optical aid, the first tab is positioned under the welding tip. As the tip is lowered by pedal pressure, it bends the ministick tab which is guided by the comb on the fixture, into contact with the IC tab. A slight additional pressure fires the welder and completes the weld. The operator progresses in this manner down one side of the stick and back up the other side. The process is repeated for all sticks.

This describes in general terms the production of a single ministick board. As stated earlier, no interlayer connections are ever required on a single board. In a system that requires more than one board, some means for multiple board interconnections must be devised; and these methods are limited only by the environmental demands of the system and the ingenuity of the designer. By and large, the use of conventional connectors is avoided. This means that for space use, one is generally limited to split pin wire wrap interconnections or welded joints.

Sample ministick boards have been made in which the external connections were in the form of split pin wire wrap terminals along one edge. A "mother board" was made, using ministick design techniques that contained the mating half of the wire wrap pins plus all interboard connections. Figure 7 shows such an arrangement.

For less critical ground equipment application, a current design uses a standard 8 x 4 matrix (4 rows of 8 chips each) that terminates in a commercial spade type connector. The socket half of the connector will be mounted on a mother board which will carry the interboard wiring. Such an arrangement makes for easy replacement of a faulty board. In this case the slightly lowered reliability introduced by the connector is a small price to pay for field serviceability.

Each board is a testable entity within itself.

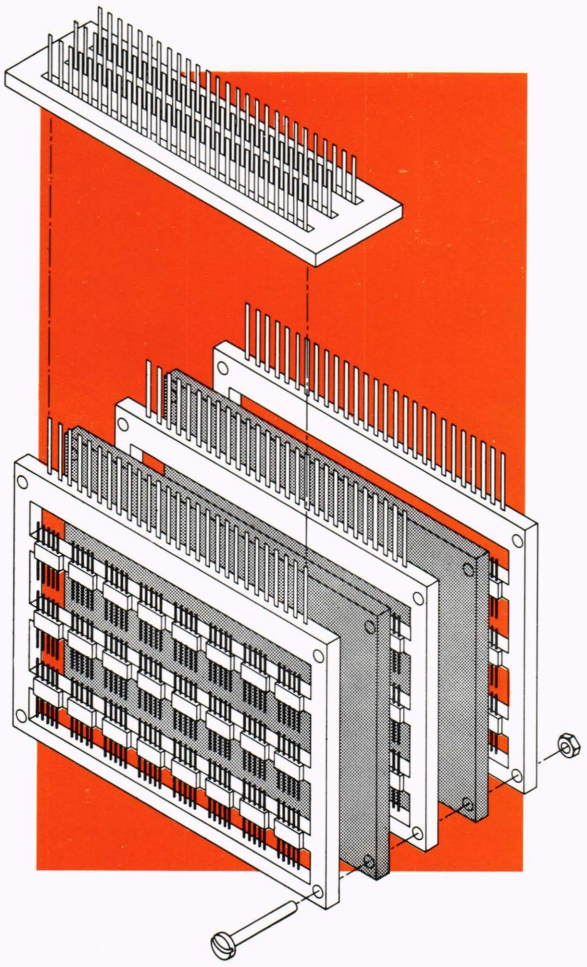

Fig. 7—Typical ministick board interconnection method.

Since all components are in a single plane and all circuits accessible to a test probe, the test time for an assembly is very short.

The ministick technique is being put to its first practical use in the Navy's Navigational Satellite. In the present satellite design, the memory—which has a capacity of 25,000 bits—occupies about one half the total volume allocated to electronics. By a combination of circuit redesign and ministick packaging, the memory has been reduced to about one third of its present volume, and the weight by a similar ratio. Storage capacity and other electrical characteristics remain the same. Indications are that the fabrication time for the memory will be substantially reduced, and the test time reduced by a factor of at least three. Reliability is expected to be significantly improved because of the generous use of integrated circuits (about 450), a major reduction in the number of connections, about 10,000 as opposed to about 30,000 in the present memory, and reduced damage in handling during fabriction and test.

The basic package design of the unit is unique in that it consists of nine subassemblies, each about 6 inches square, and all tied together by flat printed-circuit flexible cables. Five of these boards are ministick, and contain most of the integrated circuits; two are standard printed circuit boards that accommodate the necessary components not available in IC form, and the remaining one is the storage core mat consisting of 25,000 ferrite cores plus associated circuitry.

The boards are fabricated, assembled, and tested individually, then interconnected by the flexible cables "in the flat". In this form it is given its first complete system tests. The open format makes identification and repair of any faults relatively fast and easy. The final operation consists of folding the assembly much like a road map, in which form it assumes the shape of a rectangular solid as seen in Fig. 8. Finally, a cast magnesium case encloses the entire assembly which forms the flight configuration.

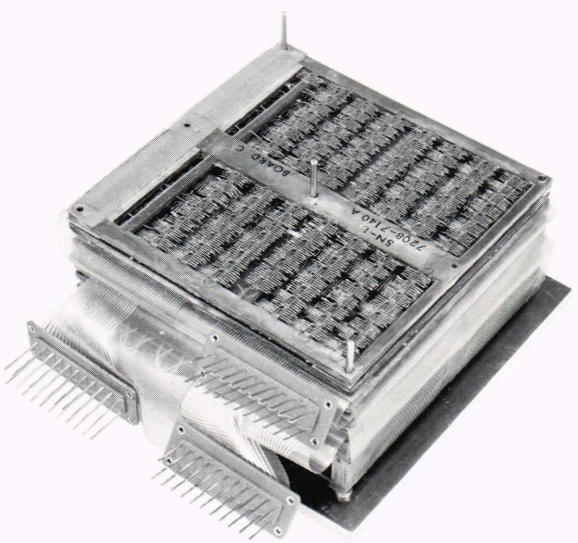

Fig. 8—Packaged ministick assembly.

The author wishes to acknowledge the significant contributions made by R. C. Evans, R. E. Hicks, and G. A. F. Winckler, during the development of the ministick process.