

Nanofabrication at APL: Novel Techniques to Deliver Innovative Devices

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ABSTRACT

The Johns Hopkins University Applied Physics Laboratory (APL) is working to realize a variety of nanostructured designs via top-down nanofabrication techniques. We leverage electron beam lithography, nanoimprint lithography, and focused ion beam deposition to pattern nanoscale features on semiconductor and optical material substrates. We combine these with other traditional microfabrication techniques as well as a few unique ones, including an atomic layer deposition–enabled nanomolding process to create high-aspect-ratio nanopillars from materials such as titanium dioxide (TiO₂). We apply these techniques on a wide variety of nontraditional substrate and film materials, including optical, phase-change, and superconducting materials, to create novel optical and electronic devices.

INTRODUCTION

Nanofabrication is the discipline of building physical structures with feature sizes significantly below 1 μm . At this scale, structures cannot be seen with the naked eye, or even with conventional optical microscopes. Nevertheless, when designed and produced correctly, nanoscale structures can produce dramatic macroscale effects. Nanofabrication can enable optical devices over a wide wavelength ranging from the infrared to visible and covering a broad spectrum of applications. Some example applications include communications, sensing, imaging, and thermal management;¹ quantum computing devices;² implantable high-density neural recorders;³ single-molecule DNA imaging devices;⁴ and ultra-sharp tips for atomic scale imaging.⁵

Nanofabrication is often divided into bottom-up versus top-down schema.⁶ Bottom-up nanofabrication refers to molecule- or particle-based assembly into

a desired structure, sometimes called self-assembly or directed assembly.^{7,8} These molecules or particles may be assembled based on binding forces that occur between them when in close proximity (e.g., chemical bonding). Bottom-up nanofabrication can also encompass energy minimization based on physical or electrostatic properties that define a preferred orientation during material deposition. While the bottom-up approach certainly has its applications, it is also somewhat limited with regard to direct control over final nanostructure and geometry, and the resulting devices are limited by this. Top-down nanofabrication involves the direct and precise control of the geometry, typically through lithographic means, that allows any arbitrary shape to be created within the resolution limits of the lithographic system. After lithography is used to create a desired pattern in a resist layer on top of the substrate, various deposition and etching

processes are commonly used to transfer that pattern from the top surface down into the material below.

APL scientists have been leveraging a variety of materials, nanopatterning methods, and pattern transfer techniques to make a diverse set of nanostructured devices, such as flat infrared photonic elements that replace bulky conventional optics and novel qubit design to enable more versatile quantum computing devices. To achieve this, we have focused primarily on the top-down nanofabrication approach.

BACKGROUND

The current processes used in state-of-the-art complementary metal-oxide-semiconductor (CMOS) fabrication can be considered nanofabrication, given the feature sizes of individual transistors and lower-level metal interconnects. Billions of dollars invested in research and development (R&D) have made this possible through strict process controls and numerous advancements in extreme-ultraviolet (EUV) photolithography, transistor structures, and self-alignment schemes. However, a commercial foundry with all the equipment required to fabricate these devices now runs upward of \$10 billion per plant,⁹ and so is only viable for the high-volume CMOS industry with its massive revenue and manufacturing scales. Chip manufacturers project that 20,000 wafers per month is the minimum efficient scale for a new state-of-the-art plant.⁶ For lower-volume applications with specialized material or processing needs that cannot be met in a traditional semiconductor chip foundry, this approach to nanofabrication is clearly out of reach.

For custom, unique, research-grade nanofabricated devices, the options for nanofabrication hinge primarily on more cost-effective low-volume nanopatterning techniques. APL leverages several different patterning

techniques to enable APL staff members to realize their nanoscale concepts, including electron beam lithography (EBL), nanoimprint lithography (NIL), and direct-write focused ion beam (FIB) deposition. We combine these tools with some traditional and some more novel pattern transfer techniques, including metallization and liftoff, reactive ion etching (RIE), ion milling, and nanomolding. In nanofabricated devices, however, process parameters must be carefully tuned at each step to yield the desired nanostructures.

NANOPATTERNING TECHNIQUES USED AT APL

Electron Beam Lithography

EBL is the most widely used and flexible approach to nanoscale patterning within an R&D environment. This technique relies on a tightly focused beam of electrons that is moved across a sample coated with an electron-sensitive photoresist, exposing the resist as it goes. Upon exposure, interactions with the electrons induce chemical changes in the resist, making the area exposed either more or less soluble in a developer (depending on whether the resist is positive tone or negative tone). A beam blanker and high-speed vector-addressable beam deflection system enable “writing” arbitrary shapes and paths in the resist layer. These written features result in openings in the photoresist coating after immersion in the developer solution. A high-quality electron beam tool can resolve features less than 10 nm in dimension with careful tuning; in our case, we typically use EBL to pattern feature sizes from 50 to 500 nm.

APL currently leverages a Raith EBPG5000+ EBL system at the US Army Research Laboratory (ARL), made available through a cooperative R&D agreement (CRADA). This tool can write on substrates from a few

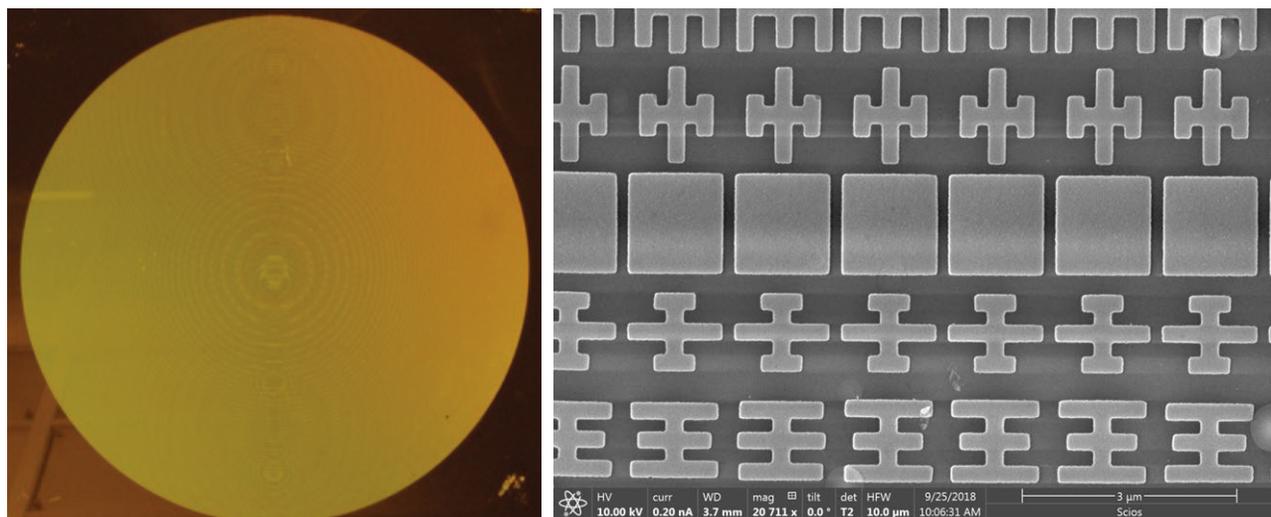


Figure 1. Complex features patterned over a large area using EBL. Left, 1-cm pattern area; right, nanostructured detail in one local spot.

millimeters in size up to 6 in. in diameter. This system can align and register between layers with a precision of ~ 30 nm. This is the workhorse of our nanopatterning techniques, and we have used it to make a wide variety of plasmonic structures designed for use in the infrared regime, as well as novel voltage-tunable superconducting junctions. As an example, Figure 1 shows a flat metasurface lens, 1 cm in diameter, patterned with EBL.¹⁰

Nanoimprint Lithography

NIL is a pattern replication technique that uses a nanopatterned master stamp to duplicate the same pattern more quickly and at a much lower cost than using solely EBL. First, the master stamp is typically fabricated on a silicon substrate. A thin layer of electron beam photoresist is spun and then baked. The resist is exposed in an EBL system, and then silicon is etched to create a rigid pattern to be replicated in a deep reactive ion etching (DRIE) system (Figure 2a). The master mold is then used to create a soft stamp on a specially surface-treated flexible polymer sheet. On the master stamp, a layer of UV-sensitive resin layer is spun, the polymer sheet is laid on the top (Figure 2b), the assembly is pressed with a roller to remove air bubbles, and then the resin is cured with UV light in a conventional contact lithography tool (Figure 2c). The UV-cured resin binds it to the polymer sheet. When the polymer sheet is peeled from the master stamp, the soft stamp is complete and retains a negative copy of the master stamp pattern (Figure 2d).

The negative-image soft stamp is then replicated onto a final target substrate using another heat- or UV-sensitive NIL resist layer in much the same way (Figure 2, e–h). We typically use a roller laminator to laminate this soft stamp onto a target substrate coated with NIL resist. This assembly is then put into a NIL system, which pulls vacuum to ensure there are no air bubbles at the interface and then applies pressure through a flexible bladder to the back of the soft stamp to ensure that the resist fully penetrates the nanostructured surface of the stamp mold and squeezes out as much excess resist as possible. While the assembly is pressed, heat is also applied to cure the NIL resist. The resulting pattern on the target substrate matches the master mold after these two image reversals. A short oxygen plasma clean is required to remove a few nanometers of NIL resist that cannot be squeezed out on the bottom of the pattern before subsequent processing (Figure 2g).

One advantage of NIL over EBL is that the processing time is the same (~ 30 min total) regardless of the sample size or pattern density. In contrast, EBL can take many hours or even days to write, depending on write area, pattern density, and critical dimension size. In these cases, fabricating a master mold using EBL once and then replicating that pattern with NIL is an effective way to reduce the process time, even when producing

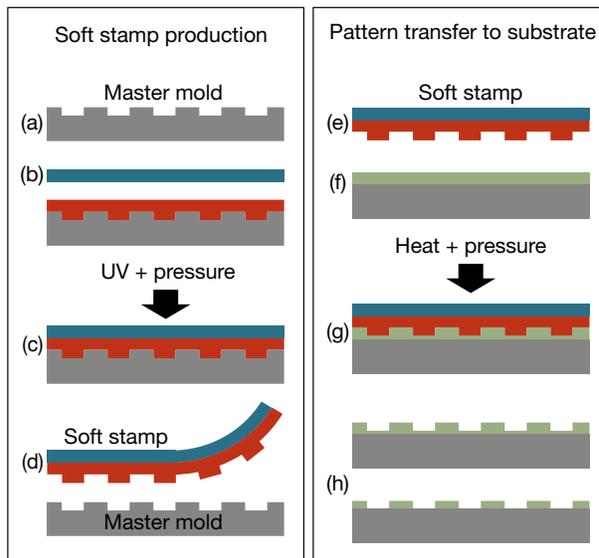


Figure 2. An illustration of the NIL process for duplicating nanostructures. (a) A silicon master mold etch. (b) A layer of UV resin is spun on the master mold. (c) A flexible polymer sheet is pressed to the master mold and then exposed with UV. (d) The soft stamp is peeled from the master mold. (e) The soft stamp is ready for NIL. (f) NIL resist is spun on a substrate. (g) The soft stamp is pressed onto the substrate with heat. (h) The NIL resist has the same pattern as the master mold. (g) A short oxygen plasma etch cleans the NIL resist residue on the bottom of the nanopattern.

a relatively small quantity. The silicon master mold can be used to make dozens of working stamps with no degradation in quality,¹¹ and each working stamp can in turn be used to make dozens of imprints. Lastly, NIL can accommodate patterning on curved surfaces, whereas EBL requires a very flat planar substrate. Given this advantage, NIL may be a good choice for patterning nanostructures on a curved lens.

APL has two NIL tools in our on-campus micro- and nanofabrication cleanroom. These include a NIL Technology (NILT) compact tool and a SÜSS MicroTec imprint lithography equipment (SMILE) system. The NILT tool is capable of patterning wafers with up to 4 in. in diameter, with no alignment capability. The SMILE tool is capable of patterning wafers up to 6 in. in diameter with alignment accuracy within 1 μm . Figure 3 shows some nanoimprinted structures patterned at APL.

Focused Ion Beam Writing

A FIB system can be used for either etching or depositing material on a sample in a localized area. The FIB system introduces a precursor gas into a vacuum chamber, which then chemisorbs onto the sample surface. The ion beam traces the desired pattern on the substrate, which breaks apart the precursor molecule into a volatile and a nonvolatile molecule. The nonvolatile part remains on the sample, while the volatile part is pumped away by the

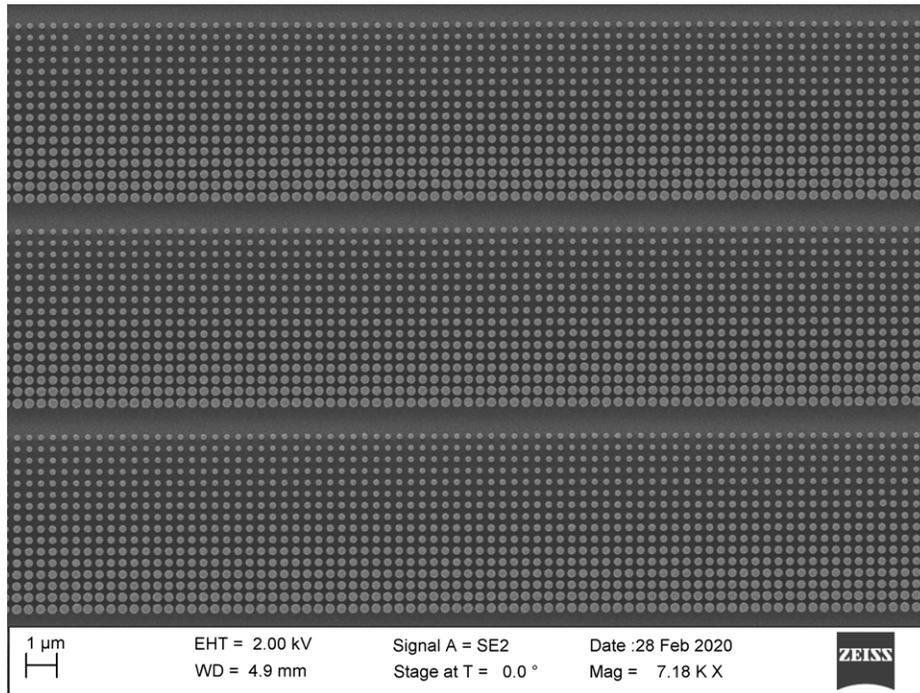


Figure 3. A scanning electron microscope (SEM) image of nanoimprinted structures fabricated at APL.

vacuum system. In this way, a gas such as tungsten hexacarbonyl [$W(CO)_6$] can be used to “direct write” tungsten wires or pads of arbitrary shape with dimensions on the order of 100 nm. However, the ion beam is not 100% effective at breaking the bonds, so some amount of organic contaminant remains in the deposited wire. Because of this, the effective resistivity for FIB-deposited metals is significantly higher (10–100 times) than metals deposited using more conventional thin-film physical vapor deposition techniques such as electron beam evaporation

or sputtering. However, in some cases, an anneal of the FIB-deposited traces after deposition can improve conductivity, presumably by removing some of the trapped contaminants.¹² APL has a dual-beam FEI Helios FIB/SEM with tungsten and platinum deposition sources and a gallium beam. Figure 4 shows a FIB-deposited platinum wire connecting to a preexisting gold pad. As deposited, tungsten generally features lower resistivity than platinum in a FIB process. However, platinum shows improvement with annealing, whereas tungsten does not. Both of these are likely because the platinum precursor has a higher ratio of carbon atoms to metal atoms than the tungsten precursor, so the tungsten material deposits with less organic contamination. We found that long anneals at low temperature are preferred for nanostructures rather than short anneals at higher temperature, which tend to cause defects that break electrical connections. Our preferred anneal process for platinum FIB wires is 150°C for 24 h in an oxygen environment, followed by an argon/hydrogen mixture (95:5 ratio by volume) at 150°C for 1 h and then at 200°C for a second hour. This results in a reduction in resistivity of 50–90% in our experiments.

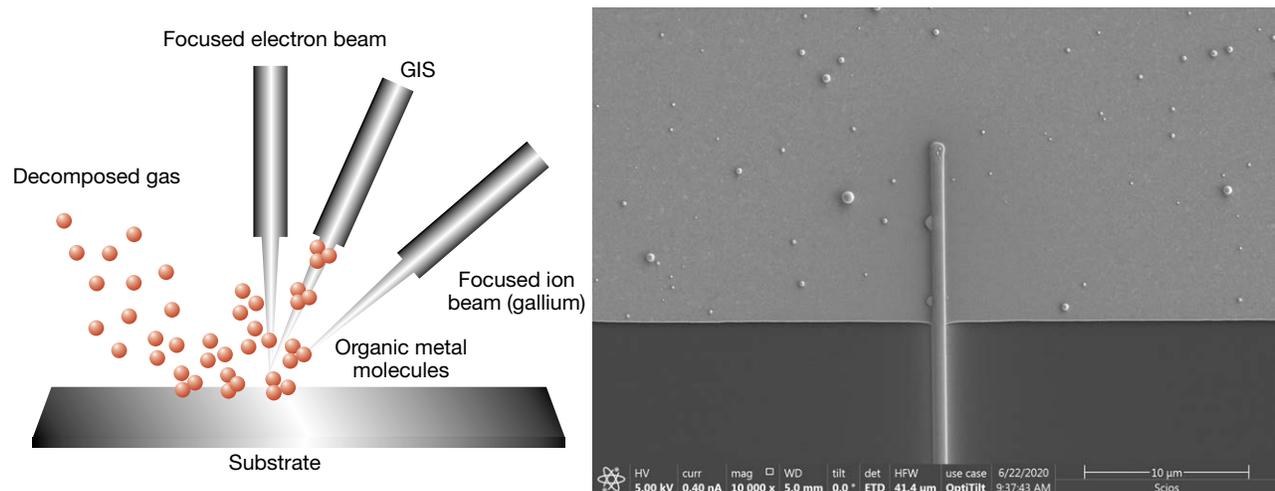


Figure 4. FIB direct-write material deposition. Left, Conceptual diagram of FIB deposition system and working principle. Right, FIB-deposited platinum wire connecting to preexisting gold pad.

PATTERN TRANSFER TO DESIRED MATERIAL

After the nanopatterning techniques described above are used to “write” a pattern of the desired geometry, the next step to fabricating a nanostructured device is to transfer that pattern into a desired material. Nanostructured devices at APL have been fabricated using a combination of traditional and novel pattern transfer techniques, such as metallization and liftoff, RIE, ion milling, and nanomolding.

Metallization and Liftoff

For thin-film nanostructures, transferring the pattern to the desired material is often straightforward. If the desired material is deposited by electron beam evaporation or ion beam sputtering, we can generally deposit directly on top of the patterned photoresist layer, then dissolve the resist away with a solvent to lift off the areas that were protected with resist. This results in a reverse image of the photoresist pattern in the new material on the surface of the wafer, as shown in Figure 5. This is most commonly used for metals, which are typically easy to evaporate, but can also be used for some dielectrics and semiconductors, such as alumina (Al_2O_3), silicon dioxide (SiO_2), silicon, and germanium. Materials deposited in this manner are typically amorphous or polycrystalline, which can affect the mechanical, optical, and electronic properties of the film, so care must be taken to ensure the film properties obtained meet the device requirements. An example of liftoff patterned nanostructures is shown in Figure 5, as well as the structures in Figure 1.

There are some common situations for which liftoff is not a viable option, namely when the desired materials require high-temperature deposition processes, or when

thick films are required. For higher-temperature material deposition processes, including materials deposited via chemical vapor deposition (CVD) or atomic layer deposition (ALD), the resist pattern often will not survive the deposition process as it begins to “reflow” or lose shape at temperatures greater than $\sim 100^\circ\text{C}$. Liftoff also does not work well for deposited films thicker than ~ 200 nm because as the desired material film thickness approaches the thickness of the electron beam resist, the material within the gaps of the resist begins to connect with the material on top of the resist, such that no gaps remain and the resist is unable to lift off when submerged in solvent. In these situations, our typical approach is to consider another pattern transfer technique, usually deposition of a complete film followed by patterning and etching.

Etching of Nanoscale Pillars

Rather than starting with patterning of a resist layer followed by material deposition and liftoff, etching typically begins with deposition of a blanket layer of the desired material, then patterning on top of this layer. RIE is then used to transfer the pattern from the top down into the material. RIE uses a radio frequency (RF) plasma to generate ions that can then be accelerated at the substrate through an electric field between the plasma and substrate (Figure 6). With the right choice of gas source, both physical and chemical etching occur at the substrate. The physical etching is due to ion bombardment, which increases the etch rate and enables vertical sidewalls with faithful reproduction of the mask geometry throughout the full etch. In contrast, most purely chemical etches would undercut the mask and erode the material underneath.

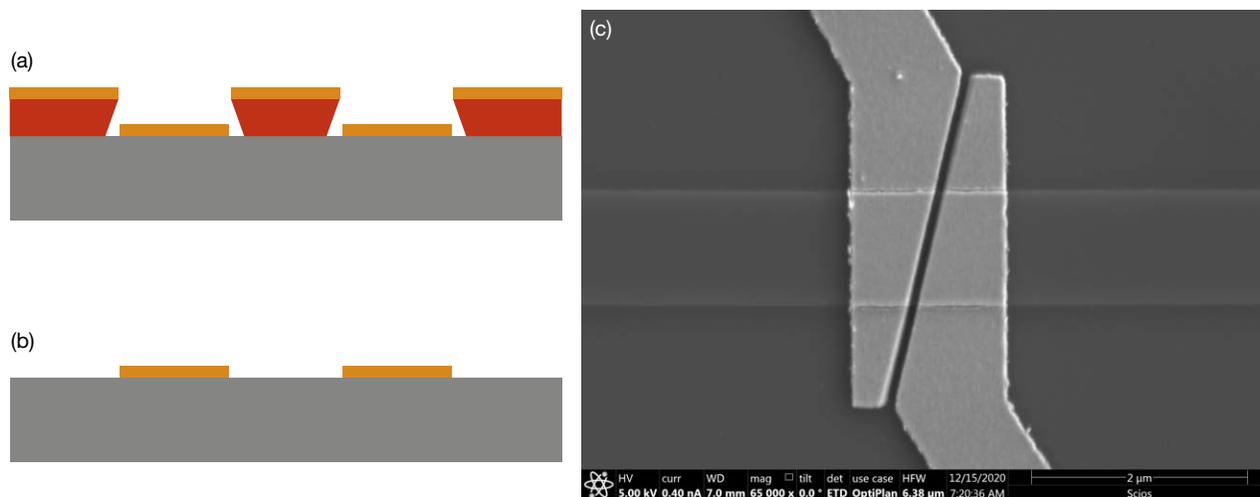


Figure 5. Conceptual depiction of liftoff process. (a) Patterned photoresist with undercut or sloping sidewalls is coated with the desired thin film. (b) When the photoresist is dissolved away with a solvent, the film sticks to the exposed features and lifts off with the photoresist in any photoresist-covered areas. (c) The resulting structure can have very high resolution and tightly controlled nanoscale dimensions. This example shows a 60-nm gap patterned between two platinum electrodes via EBL patterning, evaporation, and liftoff.

For RIE processes, the patterning is either through EBL or NIL. Because these resists do not typically have great resistance to RIE etch processes, when etching layers thicker than ~ 300 nm we often use an intermediate hard mask (typically 30–100 nm thick) as the actual etch mask. This requires writing the negative of the desired etch pattern, then using a deposition/liftoff step to transfer the pattern into a suitable hard mask material such as Al_2O_3 or chromium.

APL has access to a variety of reactive ion etchers, both in our micro- and nanofabrication cleanroom and through our CRADA with ARL. Taken together, these include chemistries that can etch an extensive variety of materials. The etch processes must be carefully tuned to achieve straight sidewalls and high-aspect-ratio structures (i.e., feature height much greater than feature width). This is most easily achieved for silicon and amorphous silicon, but we have developed processes for other materials as well. One example of a high-aspect-ratio etched nanostructure in amorphous silicon is shown in Figure 6.

Nanomolding through ALD

Finally, for materials that are difficult to etch but have established conformal deposition processes via ALD, we use a more novel nanomolding process developed at APL over the last couple years (Figure 7). After patterning a layer of electron beam photoresist, a layer of ALD titanium dioxide (TiO_2) is deposited conformally to fill the patterns in the photoresist. The ALD TiO_2 layer is planarized using an ion milling system. After removing the electron beam photoresist ALD, TiO_2 pillars are left standing on a substrate. This leaves the desired pattern intact in the ALD-deposited material.

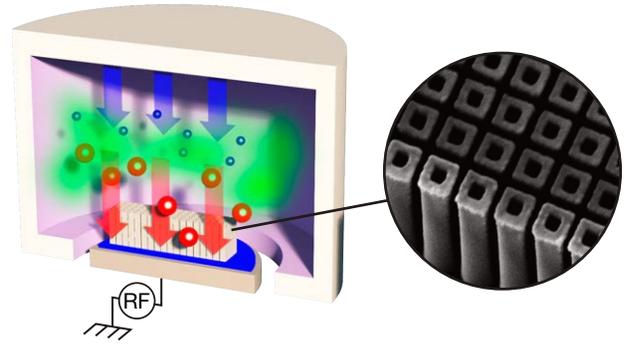


Figure 6. Conceptual drawing of RIE principle and resulting high-aspect-ratio nanostructures achieved in this process (inset).

APL has access to two Kurt Lesker ALD systems through our CRADA with ARL and a Beneq ALD system at the University of Maryland on a fee-per-usage agreement. Because ALD precursor sources are not changed routinely, each system is generally limited to two to four materials in regular usage, so access to multiple systems is useful in expanding the material set available. An example of some TiO_2 nanopillars formed using this process is shown in Figure 7b.

CONCLUSION

APL has leveraged a variety of tools, techniques, and materials to realize nanofabricated devices. We use EBL, NIL, and FIB to pattern nanoscale shapes. Transferring the pattern to the desired material often uses common microfabrication processes such as liftoff and RIE; however, we have also developed a nanomolding process based on etching the mold in a sacrificial material and

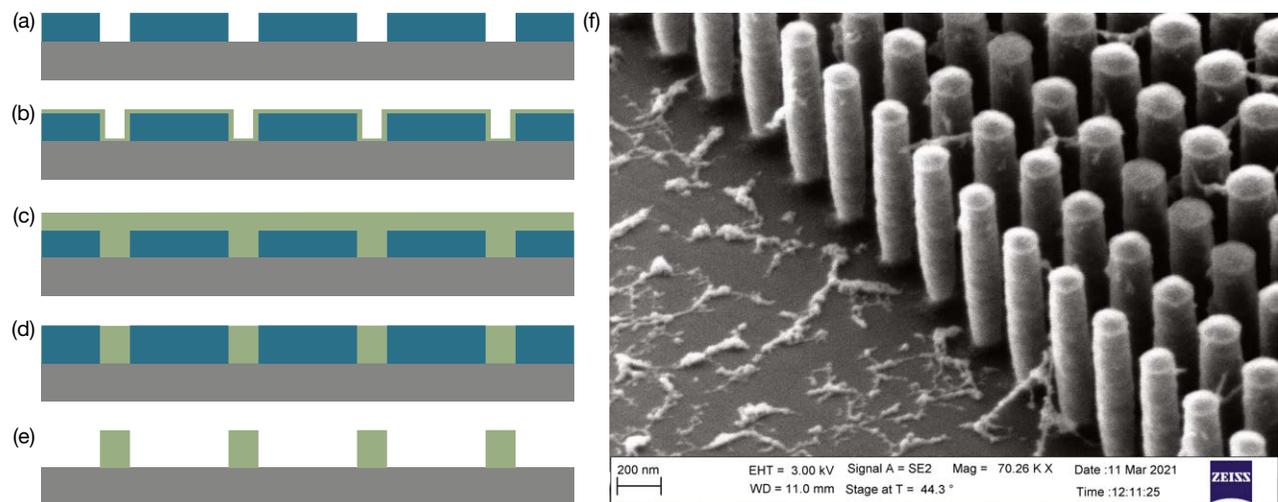


Figure 7. Nanomolding process developed at APL. (a) Electron-beam patterning of deep trenches or holes in a thick ebeam resist. (b) ALD coating begins and conformally coats from the bottom and sidewalls of the holes. (c) ALD continues until the holes are completely filled from the sides inward. (d) The ALD film built up on top of the resist is etched away, and (e) the photoresist is removed with oxygen plasma, (f) resulting high-aspect-ratio TiO_2 nanostructures patterned with this technique.

filling the mold using a conformal coating process such as ALD, then removing the mold material to leave the desired structure. We regularly work with exotic substrates and less-common thin-film materials. APL has the expertise and capability to develop custom deposition, etching, and processing for each of these unique materials, taking into account the specific sensitivities of each. We have brought all these capabilities to bear in fabricating challenging infrared optical devices, novel superconducting qubit structures, sensors, and more.

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