APL's Packaging Future: The Next Few Years

Harry K. Charles, Jr.

Next to chip technology, electronic packaging is the key to the implementation of high-performance systems, now and in the future. This article takes a systematic look at the new trends and paradigm shifts in electronic packaging that will dominate the field for the next few years. APL's current status in modern electronic packaging is presented, along with indications of how APL is responding to the rapidly changing packaging environment.
(Keywords: Advanced packaging, Electronic packaging, Future packaging.)

INTRODUCTION

In the previous articles in this issue of the *Technical Digest*, you have learned about APL's electronic packaging technology, both past and current. Now let's talk about the future. Where is electronic packaging headed in the next few years, and how will APL embrace this rapidly changing area of technology? To lay the groundwork to answer these questions, we must examine where integrated circuits and electronic products and systems are headed. Semiconductor (integrated circuit) technology continues to evolve rapidly from its beginnings in 1958.[1] The predictions of Moore's law[2,3] continue to hold, with the number of components (active devices) on chips doubling every 18 months. Today, we already have integrated circuits with over 10^8 active devices per single piece of silicon (not much bigger than an average fingernail). By 2009, we should see this number reach 10^{11} devices (transistors) on a similar-sized silicon slice.

Similarly, other things will also happen to the integrated circuit besides an increase in density. The current aluminum-silicon metal alloy system, which becomes more resistive as on-chip interconnection dimensions shrink, will be replaced by a metal with higher electrical conductivity, such as copper, probably with chromium or titanium adhesion layers.[4] Inorganic dielectric layers will also be changed to organic materials with lower dielectric constants, such as polyimide, benzocyclobutene, or Teflon-based materials.

The ultimate goal, if interconnect topologies can be worked out, would be to use air as the dielectric. As device geometries shrink, the number of electrons per device is also being reduced. With 10^8 circuit elements and a total chip power of 1 W, we have approximately 1000 electrons per device. If we project that same power limitation to the 10^{11} device level, we are down at the single electron per device level, forcing new device structures and current-control techniques. Reaching such device densities also challenges lithography techniques and the thickness of critical device layers such as gate oxides. Similarly, charge storage features (for example, trench capacitors) will require new dielectrics and the processing of nonconventional

semiconductor materials. Aspects of the chip revolution taking place over the next few years can be found in an article by Alles.[5]

While chip (integrated circuit) technology seems to be growing without bounds, what is happening to its packaging? Packaging is defined as the methodology for connecting and interfacing the integrated circuit or circuits with a system and, ultimately, the physical world. Figure 1 presents a microelectronic product time line. Important events in both the semiconductor (transistor/integrated circuit) and packaging worlds are indicated. As we move along the time line, we see events that reflect major shifts in the way packaging is done and in the drivers for the world's electronic products.

The major shift in the world's electronic products is toward portability. Along with portability go several other system-level requirement factors, including small size, low weight, low cost, ease of use, and, of course, functionality and connectivity. These system-level drivers pervade all types of electronic products—from personal computers and cellular or wireless telephone products to military field hardware, biomedical instrumentation, and spaceflight hardware. Small, lightweight, low-cost, and highly functional hardware is the key to all modern electronic system applications. Such hardware and its associated system-level evolution (revolution?) have forced major paradigm shifts in the world of electronic packaging. These paradigm shifts are captured in Fig. 2 for some of the most important processes or concepts in the packaging arena.

Other allied semiconductor-based technologies, such as integrated optics[6] and microelectromechanical systems,[7] will also play an important role in the electronic products world. Each of these will exert its influence on electronic packaging activities, bringing with it a new set of issues and a shift in packaging philosophy from individual components to integrated systems. Unfortunately, the complexity and natural differences between the optical and microminiature electromechanical worlds make a thorough discussion of their packaging beyond the scope of this work. As "electronic" packaging evolves, it can be envisioned that the development of integrated packages containing optical, electrical, and mechanical devices and systems, all operating in complete synergy, will be routine.

INTERCONNECT

In Fig. 2, we see a shift in the form of first-level interconnect from wire bonding to flip chipping. Although not new,[8] flip-chip technology is starting to make major inroads into the wire bond–dominated interconnection world (over 10^{12} wire bonds are made each year[9]). Although flip chipping is a more costly process than wire bonding, the switch is necessary to increase chip performance. Wire bonds are limited in their ability to provide low-loss interconnects at frequencies much above 10 GHz, while the short, robust pillar of the flip-chip joint provides low electrical signal loss at frequencies in excess of 100 GHz. Your digital circuits are not operating at microwave frequencies? Remember that square wave pulses have rise times. Current rise times are 100 ns or less, thus necessitating low-loss bandwidths greater than 35 GHz.[10] Figure 3 illustrates typical wire bond and flip-chip interconnect geometries.

Where is interconnect going, and how is APL postured for the future? Wire bonding will still be the

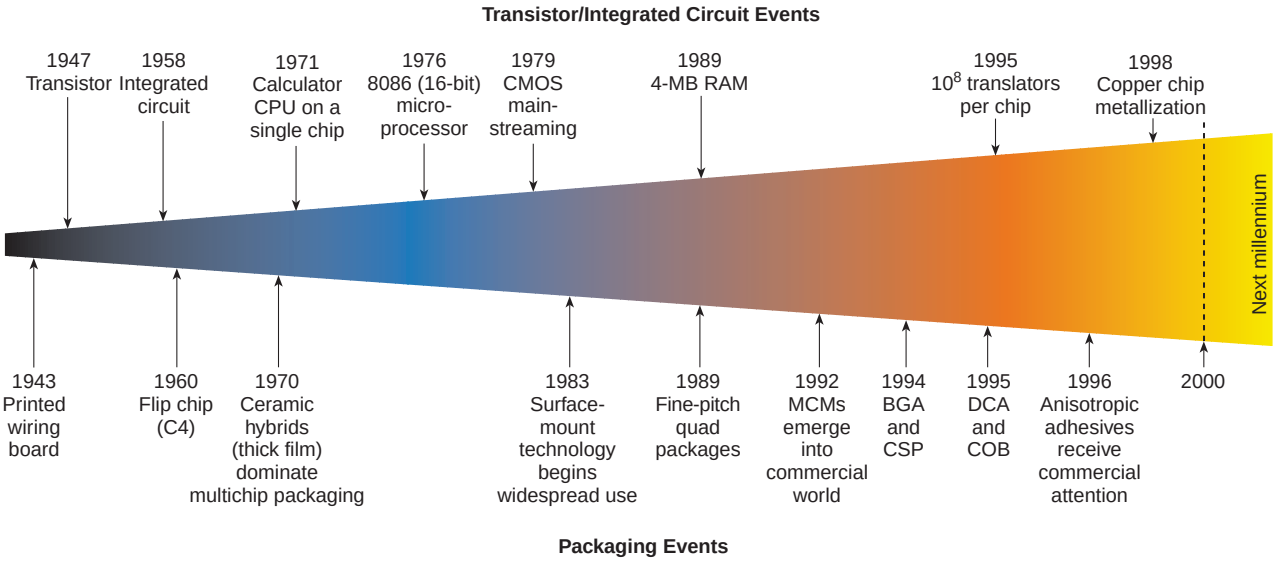


Figure 1. Microelectronic product time line. (C4 = controlled-collapse chip connection, CPU = central processing unit, CMOS = complementary metal-oxide semiconductor, RAM = random access memory. Other acronyms are defined in the text.)

Chip interconnection
Wire bonding ⇒ Flip chipping

Package (to board) interconnection
Pin-in-hole → Surface-mount technology (SMT)
→ Fine-pitch SMT ⇒ Ball-grid array (BGA)
→ Direct chip attach (DCA—packageless)

Single-chip packages
Dual-inline package (DIP) → Quad-flat package (QFP)
→ μQFP → BGA ⇒ μBGA and chip-scale packages
→ DCA ⇒ Packaging on wafer

Multichip packages
Hybrid (chip and wire) ⇒ Multichip module (MCM)
→ Composite MCM → Wafer-scale integration (WSI)
Discreted passives (R, L, C) ⇒ Integrated R and C
⇒ Integrated R, C, and L

Package hermeticity
Hermetic (ceramic, metal, glass) ⇒ Nonhermetic (plastic) encapsulants or overcoats

Figure 2. Electronic packaging paradigm shifts.

mainstay interconnect for some time to come. Two major types of wire bonding are used today: thermosonic and ultrasonic. These techniques were detailed in a previous issue of the *Technical Digest*.[11] Today, APL has both automatic and semiautomatic thermosonic and ultrasonic wire bonders capable of handling a wide variety of electronic interconnection needs. Upgrades to the equipment, such as higher-frequency ultrasonic generators, new vision systems, and software controls, will keep our systems competitive into the next millennium. A major issue is bonding to nonrigid substrates found in today's and tomorrow's multilayer organic board systems. APL has undertaken extensive studies[12] to understand the influence of soft and flexible substrate structures on the wire bonding process. Such studies and their resultant change in machine parameters and bonding practices will allow APL to produce high-quality, reliable wire bonds well into the next century.

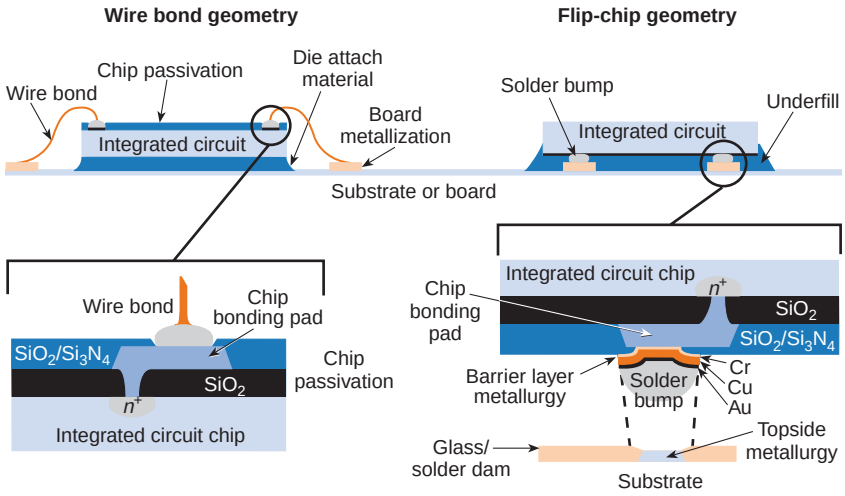
APL is currently installing a flip-chip capability in our Electronic Services Group. Our intention is to develop both a low-temperature reflow process using indium tin alloy (melting point ≈120°C) and the more traditional high-temperature process with the solders of high lead content (e.g., Sn5 or Sn10 with melting points near 300°C). Work on both these processes is well under way. In the future, alternate forms of flip-chip technology will be pursued, including such exotic sounding techniques as "stud bump and glue" and the use of anisotropic conductive adhesives. Examples of both these techniques are illustrated in Figs. 4 and 5, respectively.

In the stud bump and glue technique, single-ended, thermosonic wire bonds are placed on the chip bonding pads by means of an automatic wire bonder. The balls are then coined or tamped to a uniform height using a special tool placed in the wire bonder. This stud-bumped chip is then pressed on a plate containing a thin layer of conductive adhesive. As the chip is lifted from the plate, a small amount of the conductive adhesive adheres to each bump. The chip is then placed on the corresponding substrate pads and the adhesive is cured, resulting in the geometry illustrated in Fig. 3. In another technique, the epoxy can be pre-applied to the substrate by screen printing.

An anisotropic adhesive is an adhesive that has small conductive particles embedded in its nonconducting organic matrix. A bumped chip (see Fig. 4) is then pushed down into the adhesive, capturing a few conducting particles between the bump and the mating bonding pad on the package or substrate. When the adhesive is cured, an electrical interconnect is made. In addition, the region between the chip and the board becomes rigid, mechanically holding the chip down (underfill[13]). Such techniques offer promise over the next few years, provided issues concerning repairability, reliability, and long-term survivability can be resolved to the satisfaction of the broad-based electronics community. APL, in particular, will have to investigate the issues associated with spaceflight, such as outgassing, ability to withstand launch, and joint resistivity (with aging).

SINGLE-CHIP PACKAGING

In looking at the other paradigm shifts in Fig. 2, two major trends are evolving for the "packaging" of



Figures 3. Wire bond and flip-chip geometries.

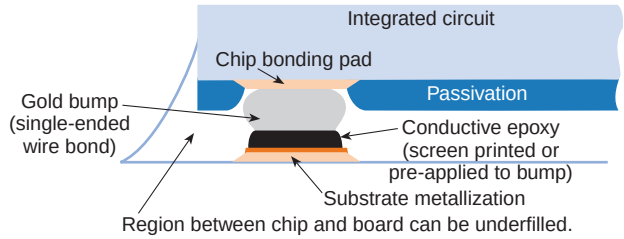


Figure 4. Schematic diagram of flip-chip technology using wire bonding (single-ended) for making a gold bump on standard chip metallurgy. The chip is then attached to the substrate by using conductive epoxy followed by an underfill as necessary.

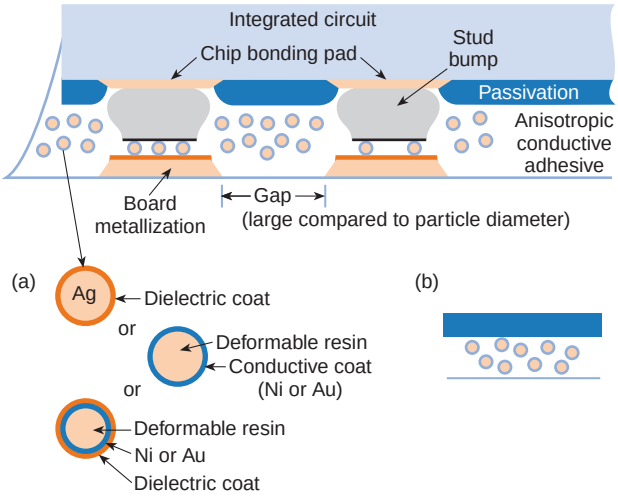


Figure 5. Anisotropic adhesive flip-chip technology. Again, stud bumps (single-ended wire bonds) are used with anisotropic adhesive layers. Insets: (a) Particle details. (b) Double-layer anisotropic conductive adhesives or films exist; only put conductive particles in the vicinity of the bump–board metallization interface (saves cost since conducting particles are expensive).

individual integrated circuits: (1) replacing the current high-density surface-mount packages, such as quad-flat packages, with ball-grid array (BGA) packages[14] as shown in Fig. 6 or (2) directly mounting the individual die on the circuit board. This direct mounting is usually described in the literature as direct chip attach (DCA). APL has its own version of DCA that we call chip-on-board (COB). Details of the current status of APL's COB are presented in this issue of the *Technical Digest* in the article by Le et al. Future evolution of APL's COB efforts will be presented later when we talk about multichip packaging.

APL is currently developing a BGA surface-mount capability, which extends our current board assembly techniques for packaged parts well into the next century. BGA will continue to evolve as the dominant packaging technique. Compared to the old dual-inline package that most of us have used in our computers, the BGA offers significant advantages, including constant input/output (I/O) density. Because the I/Os are spaced on an area array, the I/O density can remain constant even though the size of the package or required number of I/Os increases.

The importance of the BGA is illustrated by its rapid evolution to high-density versions such as the micro-BGA and to a whole series of miniaturized, high-density area (and few perimeter-type) interconnect packages called chip-scale packages (CSP). CSPs are defined as package structures with footprint areas not much larger than the chip itself. Typical definitions[15] suggest that the total area of a CSP must be less than 1.5 times the area of the chip. Figure 7 illustrates the relative size of several package types.

It will be important for APL to develop CSP handling techniques as well as to continue the evolution of DCA. Assembly of packaged parts has some distinct advantages over the handling of bare dies, as illustrated in Table 1. These advantages of CSP may have significant impact at APL because of our low-volume applications.

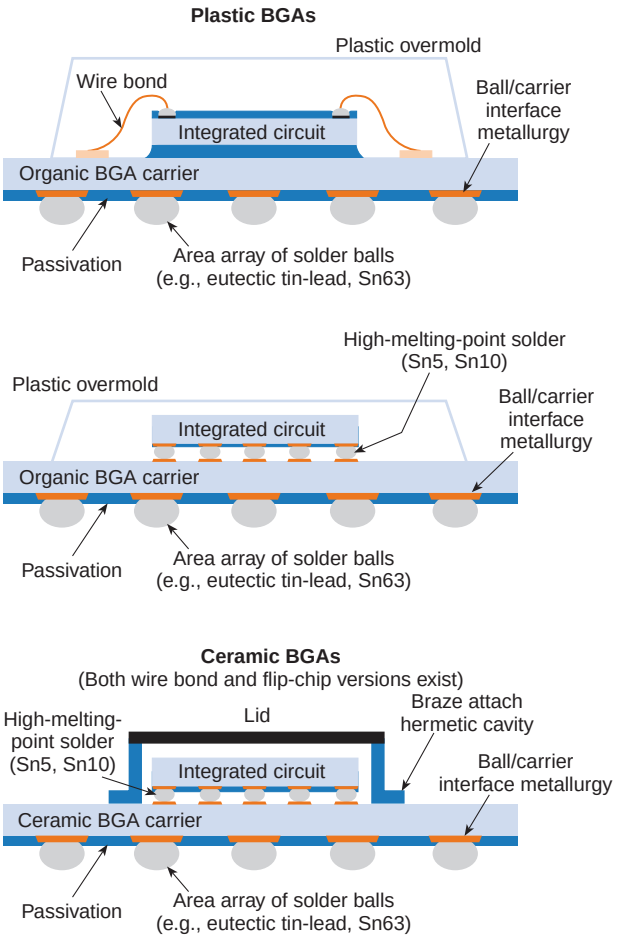
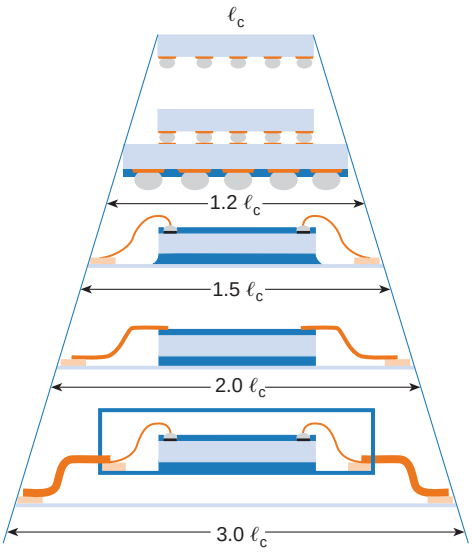


Figure 6. Ball-grid array (BGA) configurations. Chips are attached to the BGA carrier (organic or ceramic) by either wire bonding or flip chipping.



Technology	Area ratio: package/chip
Flip chip	1:1
Chip-scale package	1.5:1
Chip-on-board	2.25:1
Tape automated bonding	4.0:1
Quad-flat package	9.0:1

Figure 7. Size comparisons of flip chip (DCA) with alternate packaging styles (ℓ_c = length of chip side). For small chips, the package-to-chip area ratios may be even larger for chip-on-board, tape automated bonding, and quad-flat packages.

Table 1. Comparison of the advantages of chip-scale packages with those of direct chip attach.

Chip-scale packages	Direct chip attach
Test at speed (known good die)	Smaller footprint (and height)
Burn-in at part level	Low cost for basic unit
Die protection	Lower weight
Packaged part procurement infrastructure	Smaller circuits and systems
	Improved electrical performance
Ease of handling and rework	Improved thermal performance
Solder reflow assembly, extends surface-mount technology	More reliable (fewer interconnects)
Package standardization	
Can accommodate die shrinks or expansion	

MULTICHIP PACKAGING

The comment in the previous paragraph is not meant to downplay the importance of DCA as we build multichip chip structures. The multichip module (MCM)[16] has become a shining new star of high-density, high-performance packaging in the electronics industry worldwide and here at APL (see the article by Blum et al., this issue). MCMs exist in three primary forms based on the type of substrate interconnect structure between the chips:

1. MCM-D: deposited and photolithographically patterned thin film layers on a silicon carrier
2. MCM-C: composed of screen-printed conductors on either printed ceramic dielectric layers or thin ceramic sheets
3. MCM-L: laminate board technology similar to that used for printed wiring boards but with finer traces and a different method for producing the interlayer connections, or vias

Chips are mounted and interconnected to these high-density substrates by using either die attach followed by a wire bonding operation or by flip chipping.

MCMs are an evolution of the traditional hybrid microcircuit technology used so successfully here at APL for many years,[17] but with two distinct differences. The major difference is the density of chips on the substrate. MCMs typically cover more than 50% of the substrate area with active chips. The "old" hybrid typically had as many chips,[17] but most were passives (resistors and capacitors) rather than very-large-scale integrated circuits. The second difference is the density of the interconnect lines on the substrate. Today's MCMs' trace densities approach values of 500 in./in^2 (200 cm/cm^2) (or greater) compared to 50 in./in^2 (20 cm/cm^2) for conventional printed wiring boards and 100 in./in^2 (40 cm/cm^2) for the hybrid of old. Figure 8 is a plot of trace density versus number of board interconnect layers for various substrate technologies, both old and new.

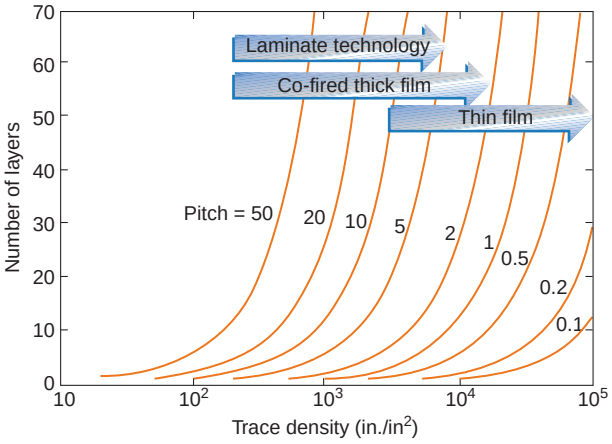


Figure 8. Number of layers versus effective board-level trace density for various multichip module circuit board technologies (and pitches [in mils]). The via penalty factor is assumed to be less than 10%.

Each of the three major MCM technologies (C, D, and L) has its advantages for certain applications (Table 2). The article by Blum et al. (this issue) shows current APL products built with each of the technologies. A major question is, "How will this technology evolve with time?" Some experts[18] predict that as MCM technology develops, only two technologies will survive: MCM-D and MCM-L. MCM-D will survive because it has the required performance or density of interconnect; however, its disadvantage is the complexity of processing and, hence, higher cost. MCM-L will survive because it is the lowest-cost option, despite its current lack of density.

Yield is a key factor as the number of chips in the module increases. Module yield (Y) as a function of the number of chips (n) for a given known good die (KGD) probability (p) is given by $Y = p^n$. Most future efforts in MCM-D technology will be aimed at cost reduction, including lower-cost materials, elimination of processing steps (e.g., using photodefinable dielectrics and conductors), yield enhancement designs, built-in testability, and the ability to repair. In some of our recent work at APL,[19] we have shown that the ability to repair is a key item in reducing the costs of MCMs. A typical yield enhancement improvement histogram as a result of the number of repairs is shown in Fig. 9. Cost analysis of most MCM structures results in curves, such as those in Fig. 10, where total module cost with and without repair is plotted against KGD probability of the included chips. Results of such analyses indicate that if repair costs are low, it is better to repair chips than to spend money for KGD. On the other hand, if repair costs are high, it pays to invest in the better chips (i.e., chips that have been screened to some level of fault coverage).

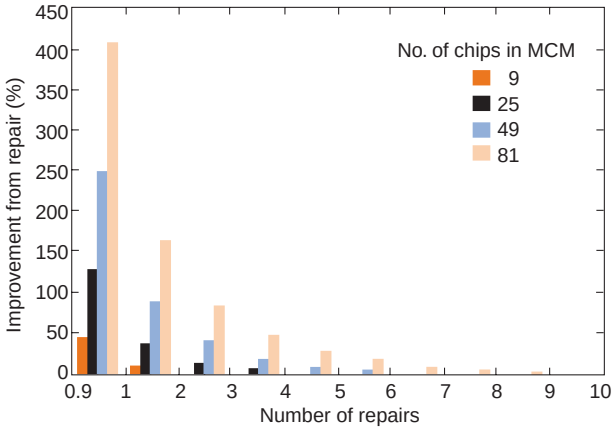


Figure 9. The percentage of improvement in fractional module yield as a function of the number of repairs for multichip modules containing 9, 25, 49, and 81 chips. Each chip has a known good die probability of 0.95.

In MCM-L technology, the thrust of technological efforts will be to increase density while maintaining the low cost associated with printed wiring board laminate technology. MCM-L technology forms the backbone of our COB efforts. Shrinking organic board feature size coupled with autocatalytic plating of bondable gold[20] has been the key to APL's success in the COB arena.

Future efforts will be aimed at replacing the drilled via structure[10] by vias produced on each layer as needed during the build-up of the board structure. These vias will be punched, etched, and/or laser drilled rather than mechanically drilled as done in the current process. Similarly, the via structures will be filled with solid metal rather than plated on the edges of drilled holes. Vias will be completely contained within one line width rather than the current[10] area-consuming plated-through-hole vias with their concomitant annular rings.

Table 2. Advantages and disadvantages of the different MCM substrate technologies.

Issue	Comments
Cost	MCM-L has lowest cost for most modules MCM-D has lowest cost for extremely high volumes and very complex modules
Density/size	MCM-D provides the densest wiring, followed by -C, then -L MCM-D for a given amount of circuitry yields the smallest size with fewest layers
Electrical performance	MCM-D has the lowest dielectric constant MCM-D has the shortest signal paths MCM-C has the best decoupling capacitors
Integrated passives (R, C, and L)	MCM-C with MCM-D (on silicon) offers significant potential; recent research indicates that organic-based passives are possible on MCM-L
Hermeticity	MCM-C and MCM-D (on ceramic or silicon with inorganic dielectric layers) are hermetic without additional coatings
Thermal performance	MCM-L is the poorest without thermal vias MCM-D (on silicon) with thermal vias is potentially the best
Coefficient of thermal expansion (CTE) mismatch problems	MCM-L with DCA or BGA-style packaging is the most prone to CTE mismatch failure

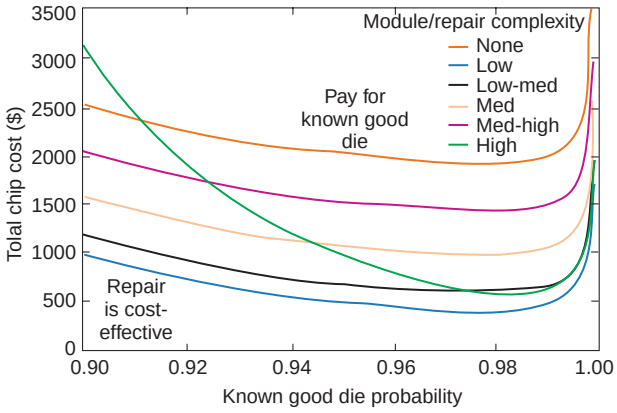


Figure 10. Normalized total chip cost of a 25-chip multichip module with and without repair for various levels of module and repair complexity.

Although these via improvements will lead to additional processing costs, we hope the increased density will reduce the number of circuit board layers as compensation. New resins, other than epoxy and polyimide, will help reduce costs and increase performance. In addition, many of the new high-density MCM-L structures will be fabricated with nonreinforced resins, making them flexible and in many ways analogous to today's flexible circuits. The trace density curves in Fig. 8 show what may be expected of MCM-L technology in the future. APL is starting work on evolving its current COB substrate structures into the MCM-L of the future.

MCM-C technology has not received as much attention in the packaging literature as it probably deserves. It is a middle-ground technology, offering densities greater than those of MCM-L (today) but less than those of MCM-D. Similarly, ceramic technology typically costs more than organic-based laminate technology but much less than MCM-Ds. APL's work on such cost versus technology trade-offs has been reported.[21]

Ceramic-based technology has been a workhorse of multichip packaging at APL for some time.[17] Ceramic-based hybrids have been used successfully in myriad applications, ranging from the Transit spacecraft to implantable medication systems. Our current low-temperature, co-fired ceramic technology has produced several important products for recent APL programs, including the Midcourse Space Experiment, Advanced Composition Explorer, and the soon-to-be-launched Thermosphere-Ionosphere-Mesosphere Energetics and Dynamics spacecraft. Low-temperature, co-fired ceramic technology will evolve into the MCM future by providing a host substrate (containing power and ground planes, plus buried passive components) for thin film organic dielectric, multilayer technology. These MCM-D/-C units, or composite MCMs, will take maximum advantage of the strength of each type of MCM. The low-dielectric-constant organic/metal signal layers will provide high-speed operation, while the high dielectric constant of the ceramic will provide excellent decoupling and power and ground insulation resistance. APL has started work with this composite substrate technology, including efforts to develop buried, passive device structures.

The integration of passive devices (R, C, and L) into the substrate structure is a hot topic in the electronic packaging world, especially in extending the technology to MCM-Ds and MCM-Ls. Integrated passives are well proven in MCM-C technology and are in limited production in MCM-D–type modules, while organic-based resistive and dielectric layers compatible with MCM-Ls are at the university and research laboratory development level.

Two other techniques are worthy of mention in the multichip packaging world. The first is the three-dimensional (3-D) stacking of chips as shown in Fig. 11. The 3-D stacking of chips is designed to reduce the board area for a given high-density component by sacrificing vertical height. Because of the stacked nature of the multiple devices and the difficulty in connecting each device to separate pads at the board level, 3-D tends to be most popular with parallel, low-I/O chip architectures such as memory. APL has experimented with the use of 3-D stacked memories in its COB applications. More 3-D stacked components will appear as the technology for "vertical" interconnect matures and the yield of the stacked components improves (see Fig. 10).

Also shown in Fig. 11 is a schematic 3-D packaging scheme in which complex MCM-like boards are stacked vertically using prepatterned compliant interposer boards. The interposer has through-board conductive channels, allowing the I/O of one circuit board to be connected to the next. This vertical stacking scheme would be clamped together mechanically to ensure good electrical contact. Unlike the 3-D stacked chip schemes where a malfunctioning chip would be cause for throwing the device away (or for using it in a less stringent application), the 3-D compression package stack can be repaired. This would allow one board to be removed and replaced without discarding the extremely expensive stack.

The many variations of 3-D–stackable packaging are beyond the scope of this article. Needless to say, APL must keep abreast of changes in this important area and be prepared to implement one or more of these 3-D schemes. Initial work has begun in developing a flexible interposer and its associated compression contacts.

The second technology of potential future interest is an MCM technology where the chips are embedded in a carrier substrate flush with the substrate's surface, as shown in Fig. 12. The space around the chips is then filled so that the chip and carrier appear as a smooth,

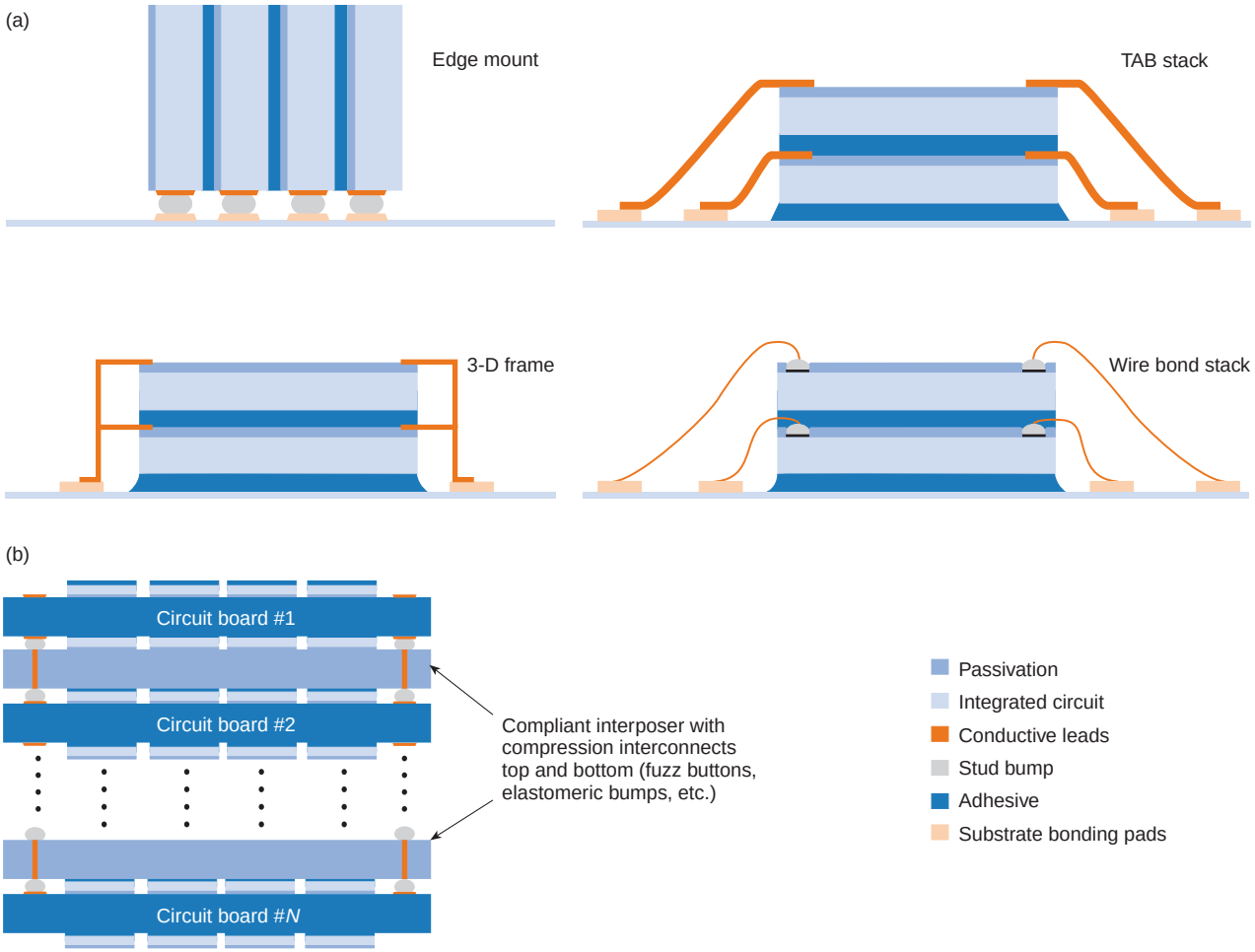


Figure 11. Three-dimensional (3-D) (a) stacked chips (TAB = tape automated bonding) and (b) stacked packaging schemes.

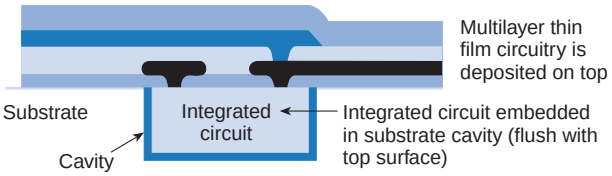


Figure 12. Chip first: high-density interconnect.

single unit. Multilayer thin film interconnects using MCM-D technology are then deposited on the planar chip/carrier surface. The result is a monolithic module of extreme density and potentially very high performance, both electrically and thermally. This so-called "chip first" technology has one major drawback—it cannot be repaired. Once encapsulated and overlayered with interconnect, the chip cannot be removed; thus the complex module is a throwaway. Many researchers are working on possible repair schemes such as dissolvable substrates. If such techniques work, the chip first MCM may become a reality.

PACKAGE HERMETICITY

The last major paradigm shift is toward nonhermetic packaging. For packaged parts, this means plastic. Plastic-encapsulated microcircuits have completely dominated the electronics world. In fact, it is difficult or impossible to get many of today's microcircuits packaged in anything but plastic. The article by Moor et al. (this issue) describes this problem in detail and how APL is gearing up to use plastic parts in many high-reliability applications, including those for space.

In the multichip world, with products such as MCMs and COB, the drive away from metal and ceramic sealed enclosures (hermetic packages) is forcing a new look at the entire issue of packages and sealed enclosures. It has been shown that tightly adhered organic layers (silicon rubber, epoxy, Parylene, etc.) can prevent corrosion of electronic systems even though moisture can readily permeate these materials (permeability coefficients are orders of magnitude lower for organic-based materials than for the traditional metal or ceramic-based packaging materials). The concept relies on the premise that

liquid water causes corrosion and, hence, electronic failure.[22]

A tightly adhered coating allows only molecular water to reach the surface. Once adhesion is lost or a crack develops, a pocket can form, resulting in the accumulation of liquid water; hence, corrosion can begin. Integrated circuit dies are now sealed (except at the bonding pads) with high-quality oxide and nitride layers. Thus, if an effective seal around the bonding pads can be made, the chips would be totally protected. Such seals are made by barrier layer metallurgy used in a flip-chip bumping process or by the application of a chip coating material ("glob top") if wire bonding is used for chip interconnect. Examples of APL glob tops are shown in the article by Le et al. (this issue). Flip-chip assemblies are underfilled (with organic pottants) in many MCM and COB applications to mitigate the strain on the solder joints in situations where the coefficient of thermal expansion of the chip and the board are far apart. This underfill can also help protect the pads in the case of stud bumping described previously.

In either case, the chip is protected and the hermeticity requirement gets pushed from the chip to the substrate. Ceramic-based substrates are, for the most part, hermetic, assuming the top-layer metals are noble enough to prevent corrosion. Printed wiring boards have been overcoated for years to reduce surface leakage and trace edge corrosion.

Today we are overcoating our COB applications with Parylene. The insulating properties of Parylene are excellent for electronic applications and have been reported recently for films produced by our Parylene deposition system at APL.[10] MCM-D substrates have typically been packaged in hermetic enclosures. There are, however, many reports[21] of nonhermetically sealed MCM-Ds being reliable (gold top-surface metallization) under 85°C, 85% relative humidity testing.

Although such test results are promising, long-term reliability may require additional overcoats or a switch from the traditional polyimide-based dielectric to one that has less moisture absorption, such as benzocyclobutene.[23] APL is currently studying the organic overcoating of MCM-Ds as well as exploring alternate dielectrics, including low-moisture-absorbing benzocyclobutene and a chromofore-doped polyimide,[24] which offer promise in the testability of complex substrate structures such as MCMs.

DISCUSSION

Modern electronic packaging is a rapidly changing field with many nuances and a myriad of technologies. Many key drivers and shifts in thinking are taking place as the electronic products business becomes almost completely dominated by commercial products. The portable/wireless revolution is driving us to small, lightweight, high-performance systems that are wirelessly connected to the world, all at costs far below those associated with historic electronic products and markets. These trends have produced major paradigm shifts for the electronic packaging world. As we have seen, words such as flip-chip, direct chip attach, ball-grid array, chip-scale package, and multichip module will become just as familiar in our electronics packaging vocabulary as the dual-inline package and the chip and wire hybrid are today.

Figure 13 summarizes many of the packaging concepts described in this article and places them in a family tree–like form with some of their more familiar ancestors. It also shows how the minimal package and

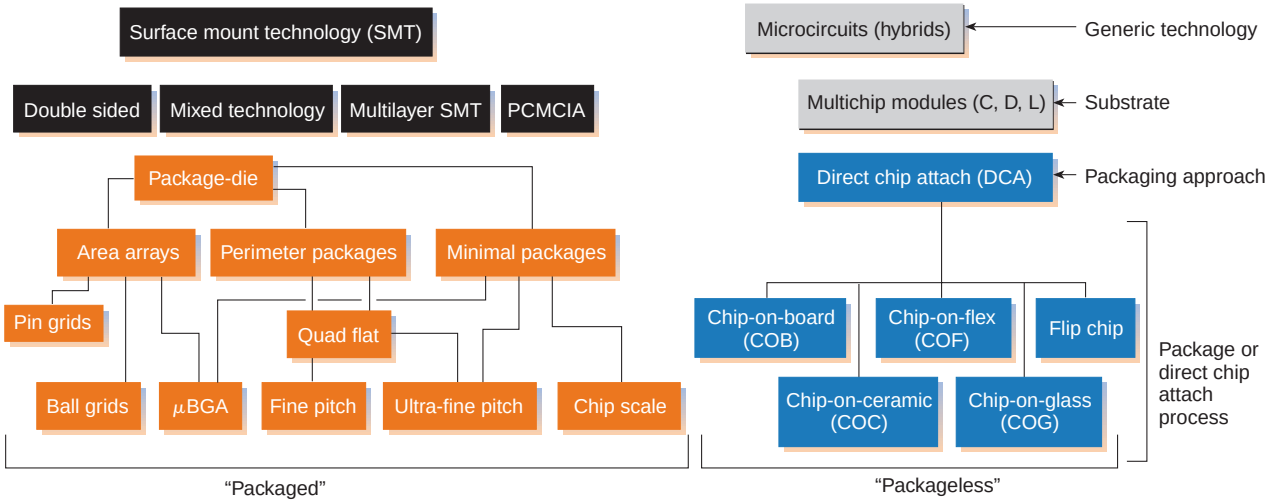


Figure 13. Packaging hierarchy: substrate and package types.

packageless parts have evolved from more traditional products.

SUMMARY

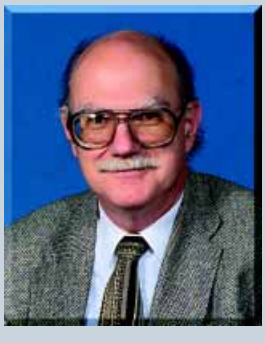
Electronic packaging is rapidly changing to meet the demands of the commercial world. High-reliability systems (military, space, biomedical, etc.) are being driven to use these commercial technologies at a rapid pace owing to the unavailability of more traditional, hermetic products and the promise of lower cost. APL's electronic packaging efforts have kept pace with the commercial world and are offering products and services that meet the needs of our in-house packaging clients. Future needs are being addressed through selective enhancement of today's activities, along with the introduction of new technology. This work should ensure that APL continues to have appropriate electronic packaging solutions for its systems customers.

REFERENCES

[1] Kilby, J. S., "Invention of the Integrated Circuit," *IEEE Trans. Electron. Devices* ED-23, 648–654 (1976).
[2] Moore, G. E., "VLSI: Some Fundamental Challenges," *IEEE Spectrum* 16(4), 30–37 (1979).
[3] Schaller, R. R., "Moore's Law: Past, Present, and Future," *IEEE Spectrum* 34(6), 53–59 (1997).
[4] Geppert, L., "Solid State," *IEEE Spectrum* 35(1), 23–28 (1998).
[5] Alles, M. L., "Thin Film SOI Emerges," *IEEE Spectrum* 34(6), 37–45 (1997).
[6] Agullò-Lòpez, F., Cabrera, J. M., and Agullò-Eueda, F., *Electro-optics: Phenomena, Materials and Applications*, Academic Press, London (1994).
[7] Murphy, J. C., Benson, R. C., and Charles, Jr., H. K., "Miniature Sensors Based on Micromechanical Systems," *Johns Hopkins APL Tech. Dig.* 16(3), 311–318 (1995).
[8] Miller, L. F., "Controlled Collapse Reflow Chip Joining," *IBM J. Res. Dev.* 13, 239–250 (1969).
[9] Harman, G., *Wirebonding in Microelectronics: Materials, Processes, Reliability, and Yield*, McGraw Hill, New York (1997).
[10] Bakoglu, H. B., "Interconnection Resistance," Chap. 5 in *Circuits, Interconnections, and Packaging for VLSI*, Addison-Wesley, Reading, MA, pp. 194–225 (1990).
[11] Charles, Jr., H. K., "Materials in Electronic Packaging at APL," *Johns Hopkins APL Tech. Dig.* 14(1), 51–67 (1993).
[12] Charles, Jr., H. K., Mach, K. J., Edwards, R. L., and Lehtonen, S. J., "Wirebonding for Multichip Modules," in *Proc. Int. Microelectron. Symp.*, Minneapolis, MN, pp. 420–425 (1996).
[13] Ito, S., Kuwamura, M., Akizuki, S., Ikemura, K., Fukushima, T., and Sudo, S., "Solid Type Cavity Fill and Underfill Materials for New IC Packaging Applications," in *Proc. 45th Electronic Components and Technol. Conf.*, Las Vegas, NV, pp. 1217–1222 (1995).
[14] Lau, J. H., and Pao, Y-H., *Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies*, McGraw-Hill, New York (1997).
[15] Aday, J. G., Koehler, C., Tessier T., Carpenter, B., Matsuda, Y., and Esteo, C., "Flip Chip Scale Packaging: Transferring the Flip Chip Density Requirements from the Mother Board to the Chip Carrier," in *Proc. Int. Conf. and Exhibition on Multichip Modules and High Density Packaging*, Denver, CO, pp. 229–235 (1998).
[16] Charles, Jr., H. K., "Electronic Materials and Structures for Multichip Modules," *ASME J. Electronic Packaging* 114, 226–233 (1992).
[17] Charles, Jr., H. K., and Wagner, G. D., "Microelectronics at APL: The First Quarter Century," *Johns Hopkins APL Tech. Dig.* 6(2), 130 (1985).
[18] Carpenter, Jr., J. A., Evans, J., Hakim, E. B., Naclerio, N., Lyle, J., et al., "Overview of US Government Advanced Packaging Programs," in *Proc. Int. Conf. on Multichip Modules*, Denver, CO, pp. 495–500 (1993).
[19] Petek, J. M., and Charles, Jr., H. K., "Known Good Die, Die Replacement (Rework), and Their Influences on Multichip Module Costs," in *Proc. 48th IEEE Electronic Components and Technol. Conf.*, Seattle, WA, pp. 909–915 (1998).
[20] Charles, Jr., H. K., Mach, K. J., Edwards, R. L., Lehtonen, S. J., and Lee, D. M., "Wirebonding on Various Multichip Module Substrates and Metallurgies," in *Proc. 47th IEEE Electronic Components and Technol. Conf.*, San Jose, CA, pp. 670–675 (1997).
[21] Charles, Jr., H. K., "Cost Versus Technology Trade-Offs for Multichip Modules," *ISHM J. Microelectron. Electronic Packaging* 19(3), 295–300 (1996).
[22] Sinnadurai, F. N. (ed.), *Handbook of Microelectronics Packaging and Interconnection Technologies*, Electrochemical Publications, Ayr, Scotland, pp. 7–10 (1985).
[23] Takahashi, T., Rutter, Jr., E. W., Moyer, E. S., Harris, R. F., Frye, D. C., et al., "A Photo-definable Benzocyclobutene Resin for Thin-Film Microelectronic Applications," in *Proc. Int. Microelectronics Conf.*, Yokohama, Japan, pp. 64–70 (1992).
[24] Mechtel, D. M., Charles, Jr., H. K., and Francomacaro, A. S., "Electro-optic Probing: A Laser-Based Solution for Noninvasive High Speed Testing of Multichip Modules," in *Proc. Int. Microelectron. Symp.*, Philadelphia, PA, pp. 125–130 (1997).

ACKNOWLEDGMENTS: I gratefully acknowledge the efforts of both the Electronic and Mechanical Services Groups, without whose support the APL accomplishments mentioned in this article could not have been achieved and whose continuing support will be necessary to achieve the future packaging vision for APL. I extend a special thank you to S. Lynn Hoff for manuscript preparation.

THE AUTHOR



HARRY K. CHARLES, JR., received his B.S. in 1967 from Drexel University and his Ph.D. in 1972 from The Johns Hopkins University, both in electrical engineering. He joined APL in 1972 as a Postdoctoral Research Associate. He is currently Assistant Department Head for Engineering in the Technical Services Department and a member of the Principal Professional Staff. Dr. Charles has worked for 25 years in the microelectronics arena, authored over 150 articles, and is an internationally recognized specialist in electronic devices, systems, packaging, and reliability. His latest interests include multichip module design, fabrication, and testing; advanced interconnect; biomedical instrumentation; and novel sensors based on MEMS technology. He is a Fellow and former President of IMAPS (The International Microelectronics and Packaging Society), a Fellow of the IEEE, and a member of the Board of Governors of the IEEE's Components Packaging and Manufacturing Technology (CPMT) Society. His e-mail address is harry.charles@jhuapl.edu.