



## The Impact of Electronic Packaging at APL: Guest Editor's Introduction

Harry K. Charles, Jr.

Imagine a gold or aluminum wire several times finer than a human hair, sized, shaped, and positioned with much greater precision than by a surgeon's hand, all within a fraction of a second. Interconnects such as these are repeated hundreds to thousands of times for each electronic product produced. Then further imagine that such operations are done over 10-billion times daily around the world! These are examples of just a few of the myriad activities that must be performed to package an electronic device, assembly, or system.

The world of electronic packaging is a complex, highly interdisciplinary one that is facing significant technological challenges. Levels of integration are doubling on an almost annual basis. Chips dissipate more power, require more inputs and outputs, and operate at ever-increasing speeds. The 450-MHz personal computer is available today for the desktop, and 1-GHz models are in the laboratory. Electronics are getting smaller and smaller, but with ever-expanding functionality. Harnessing the available functionality in a manner compatible with the application and at a reasonable cost is the modern electronic packaging challenge.

Where does APL fit into this modern electronic packaging world, and is it prepared for future challenges? This issue of the *Technical Digest* attempts to answer these questions by capturing our electronic packaging history, extensively exploring our current packaging capabilities, and providing a glimpse into the packaging "future world."

In the article by Wagner, our packaging history from the VT fuze to some of our latest Earth satellites and spacecraft is captured. Remember, the VT fuze owed its success to the extremely innovative packaging of vacuum tube circuits. The next article by Bevan and Romenesko summarizes modern packaging technology and provides a discussion of the full range of the latest packaging applications in place at APL.

Clatterbaugh, Vichot, and Charles provide insight into the key issues that must be addressed to successfully package today's high-performance integrated circuits. Packaging solutions developed by APL for several important Laboratory programs are shown as examples of how critical performance issues are resolved. In the article by Le et al., APL's growing chip-on-board (COB) program for the miniaturization of space

electronics is described. A sampling of material and process qualification studies is presented along with the long-term reliability implications for COB technology.

Blum, Charles, and Francomacaro describe in detail the fabrication of substrates for multichip modules (MCMs). These substrates are the key to any current and future multichip applications. Such substrates can contain over a mile of routed track length, all within a few square inches of space.

Kopp, Moore, and Coffman tackle the subsystem-level packaging of high-frequency components. They describe our efforts in the development of miniature transmit/receive modules for phased-array radar systems. For high-frequency design, the package is a major factor in achieving overall subsystem performance.

System-level packaging is explored by Mehoke, Feldmesser, and Grimm. Their article focuses on the system design process and how the packaging engineer makes all the elements (design, fabrication, testing, components) come together successfully. Components are addressed in the article by Moor, Casanovas, and Purwin. They examine the use of plastic-encapsulated microcircuits (PEMs) in high-reliability flight applications. APL's PEMs program is described, along with our standardized plastic part handling procedure.

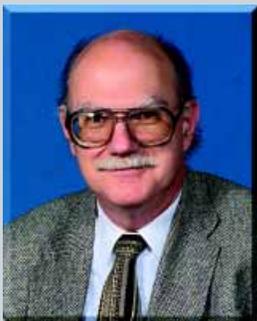
Charles takes a look at the future of electronic packaging and relates APL's current efforts and

planned activities to the future packaging challenge. As important as packaging has been to the Laboratory's electronic systems in the past, it will be even more critical in the future. Portability (small size, weight, and power), connectivity (global electronic access), and low cost will be the keys to all electronic products; even low-volume and one-of-a-kind development systems such as those produced at APL will be impacted significantly.

Recognizing the importance of electronic packaging now and in the future as well as the complex interdisciplinary aspects of the field, many packaging leaders have demanded that universities provide the packaging engineers of the future. Several universities have risen to the challenge. Our special feature article is written by Rao Tummala of Georgia Institute of Technology. He describes his National Science Foundation-funded engineering research center and the education model for packaging in the 21st century.

In summary, I hope this issue of the *Technical Digest* will clearly demonstrate to the reader that (1) electronic packaging is key to the development of all current and future electronic systems—just as it has been in the past, (2) electronic packaging faces many important technological challenges over the next few years, (3) APL is ready to meet those challenges head-on, and (4) electronic packaging engineering is an important, necessary, and extremely interesting discipline.

#### THE AUTHOR



HARRY K. CHARLES, JR., received his B.S. in 1967 from Drexel University and his Ph.D. in 1972 from The Johns Hopkins University, both in electrical engineering. He joined APL in 1972 as a Postdoctoral Research Associate. He is currently Assistant Department Head for Engineering in the Technical Services Department and a member of the Principal Professional Staff. Dr. Charles has worked for 25 years in the microelectronics arena, authored over 150 articles, and is an internationally recognized specialist in electronic devices, systems, packaging, and reliability. His latest interests include multichip module design, fabrication, and testing; advanced interconnect; biomedical instrumentation; and novel sensors based on MEMS technology. He is a Fellow and former President of IMAPS (The International Microelectronics and Packaging Society), a Fellow of the IEEE, and a member of the Board of Governors of the IEEE's Components Packaging and Manufacturing Technology (CPMT) Society. His e-mail address is [harry.charles@jhuapl.edu](mailto:harry.charles@jhuapl.edu).